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Conception et test de cellules de gestion d'énergie à commande numérique en technologies CMOS avancées

Design and Test of Digitally-Controlled Power Management IPs in Advanced CMOS Technologies

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Jury :

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MEGA	**MECANIQUE, ENERGETIQUE, GENIE CIVIL, ACOUSTIQUE** Secrétariat : M. LABOUNE PM : 71.70 –Fax : 87.12 Bat. Saint Exupéry mega@insa-lyon.fr	M. Philippe BOISSE INSA de Lyon Laboratoire LAMCOS Bâtiment Jacquard 25 bis avenue Jean Capelle 69621 VILLEURBANNE Cedex Tél :04.72.43.71.70 Fax : 04 72 43 72 37 Philippe.boisse@insa-lyon.fr
ScSo	**ScSo*** M. OBADIA Lionel Sec : Viviane POLSINELLI Insa : J.Y. TOUSSAINT	M. OBADIA Lionel Université Lyon 2 86 rue Pasteur 69365 LYON Cedex 07 Tél : 04.78.69.72.76 Fax : 04.37.28.04.48 Lionel.Obadia@univ-lyon2.fr

*ScSo : Histoire, Geographie, Aménagement, Urbanisme, Archéologie, Science politique, Sociologie, Anthropologie

Abstract

Owing to the development of modern semiconductor technology, it is possible to implement a digital controller for low-power high switching frequency DC-DC power converter in FPGA and ASIC. This thesis is intended to propose digital controllers with high performance, low power consumption and simple implementation architecture.

Besides existing digital control-laws, such as PID, RST, tri-mode and sliding-mode (SM), a novel digital control-law, direct control with dual-state-variable prediction (DDP control), for the buck converter is proposed based on the principle of predictive control. Compared to traditional current-mode predictive control, the predictions of the inductor current and the output voltage are performed at the same time by adding a control variable to the DPWM signal. DDP control exhibits very high dynamic transient performances under both load variations and reference changes. Experimental results in FPGA verify the performances at switching frequency up to 4MHz. Considering the implementation complexity and performances, DDP control is therefore a better candidate compared to PID, RST and SM controls.

For the boost converter exhibiting more serious nonlinearity, linear PID and nonlinear SM controllers are designed and implemented in FPGA to verify the performances.

A digital control requires a DPWM. Σ-Δ DPWM is therefore a good candidate regarding the implementation complexity and performances. An idle-tone free condition for Σ-Δ DPWM is considered to reduce the inherent tone-noise under DC-excitation compared to the classic approach. A guideline for Σ-Δ DPWM helps to satisfy proposed condition. In addition, an 1-1 MASH Σ-Δ DPWM with a feasible dither generation module is proposed to further restrain the idle-tone effect without deteriorating the closed-loop stability as well as to preserve a reasonable cost in hardware resources. The FPGA-based experimental results verify the performances of proposed DPWM in steady-state and transient-state.

Two ASICs in $0.35\mu m$ CMOS process are implemented including the tri-mode controller for buck converter and the PID and SM controllers for the buck and boost converters respectively.

The lab-scale tests are designed to lead to a power assessment model suggesting feasible applications. For the tri-mode controller, the measured power consumption is only 24.56mW/MHz when the time ratio of stand-by operation mode is 0.7. As specific power optimization strategies in RTL and system-level are applied to the latter chip, the measured power consumptions of the SM controllers for buck converter and boost converter are 4.46mW/MHz and 4.79mW/MHz respectively. The power consumption is foreseen as less than 1mW/MHz when the process scales down to nanometer technologies based on the power-scaling model. Compared to the state-of-the-art analog counterpart, the prototype ICs are proven to achieve comparable or even higher power efficiency for low-to-medium power applications with the benefit of better accuracy and better flexibility.

Résumé

Les technologies avancées de semi-conducteur permettent de mettre en œuvre un contrôleur numérique dédié aux convertisseurs à découpage, de faible puissance et de fréquence de découpage élevée sur FPGA et ASIC. Cette thèse vise à proposer des contrôleurs numériques des performances élevées, de faible consommation énergétique et qui peuvent être implémentés facilement.

En plus des contrôleurs numériques existants comme PID, RST, tri-mode et par mode de glissement, un nouveau contrôleur numérique (DDP) pour le convertisseur abaisseur de tension est proposé sur le principe de la commande prédictive: il introduit une nouvelle variable de contrôle qui est la position de la largeur d'impulsion permettant de contrôler de façon simultanée le courant dans l'inductance et la tension de sortie. La solution permet une dynamique très rapide en transitoire, aussi bien pour la variation de la charge que pour les changements de tension de référence. Les résultats expérimentaux sur FPGA vérifient les performances de ce contrôleur jusqu'à la fréquence de découpage de 4MHz. Les comparaisons avec les commandes PID, RST et par mode de glissement montrent que le contrôleur DDP présente un meilleur compromis entre la complexité algorithmique et les performances.

Pour le convertisseur élévateur de tension où la présence de non linéarité est importante, un contrôleur PID linéaire et un contrôleur par mode de glissement non linéaire sont conçus et mis en œuvre sur FPGA afin de vérifier leur performance.

Un contrôleur numérique nécessite une modulation numérique de largeur d'impulsion (DPWM). L'approche Σ-Δ de la DPWM est un bon candidat en ce qui concerne le compromis entre la complexité et les performances. Un guide de conception d'étage Σ-Δ pour le DPWM est présenté. Une architecture améliorée de architectures traditionnelles 1-1 MASH Σ-Δ DPWM est synthétisée sans détérioration de la stabilité en boucle fermée ainsi qu'en préservant un coût raisonnable en ressources matérielles. Les résultats expérimentaux sur FPGA vérifient les performances des DPWM proposées en régimes stationnaire et transitoire.

Deux ASICs sont portés en CMOS 0,35μm: le contrôleur en tri-mode pour le convertisseur

abaisseur de tension et la commande par mode de glissement pour les convertisseurs abaisseur et élévateur de tension. Les bancs de test sont conçus pour conduire à un modèle d'évaluation de consommation énergétique. Pour le contrôleur en tri-mode, la consommation de puissance mesurée est seulement de 24,56mW/MHz lorsque le ratio de temps en régime de repos (stand-by) est 0,7. Les consommations de puissance de commande par mode de glissement pour les convertisseurs abaisseur et élévateur de tension sont respectivement de 4,46mW/MHz et 4,79mW/MHz. En utilisant le modèle de puissance, une consommation de la puissance estimée inférieure à 1mW/MHz est envisageable dans des technologies CMOS plus avancées. Comparé aux contrôlés homologues analogiques de l'état de l'art, les prototypes ASICs illustrent la possibilité d'atteindre un rendement comparable pour les applications de faible et de moyen puissance mais avec l'avantage d'une meilleure précision et une meilleure flexibilité.

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Bo

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Abbreviation

ADC	Analog-to-digital converter
ALU	Arithmetic logic unit
ASIC	Application-specific integrated circuit
CCM	Continuous conduction mode
CMOS	Complementary metal-oxide-semiconductor
DAC	Digital-to-analog converter
DCM	Discontinuous conduction Mode
DLL	Delay-locked loop
DMASH	Dithered multistage noise shaping
DNL	Differential nonlinearity
DPWM	Digital pulse-width modulation (modulator)
DRC	Design rule check
DSP	Digital signal processor
EDA	Electronic design automation
ESR	Equivalent series resistance
FPGA	Field-programmable gate array
HDL	Hardware description language
IC	Integrated circuit
INL	Integral nonlinearity
IP	Intellectual property
LCO	Limit-cycle oscillation
LDO	Low-dropout regulator

LP	Loop filter
LSB	Least significant bit
LUT	Look-up table
LVS	Layout versus schematic
MASH	MultistAge-noise-SHaping
MLS	Maximum length sequence
MOSFET	Metal-oxide-semiconductor field-effect transistor
MSB	Most significant bit
NTF	Noise transfer function
PD	Phase detector
PLL	Phase-locked loop
PN	Pseudo-noise
PSD	Power spectral density
PVT	Process-voltage-temperature
PwrSoC	Power supply-on-chip
RTL	Register-transfer level
SAR	Successive approximation register
SDF	Standard delay format
SM	Sliding-mode
SMPS	Switched-mode power supply
STF	Signal transfer function
TTM	Time to market
VCO	Voltage-controlled oscillator
VLSI	Very-large-scale integration
VSS	Variable structure system
ZOH	Zero order hold

French Part

Chapitre 1 Etat de L'art

Afin de bénéficier de la technologie avancée CMOS, beaucoup d'idées sont proposées vis-à-vis de la commande numérique des convertisseurs de puissance. Contrairement au contrôleur analogique, l'implémentation du contrôleur numérique requiert un convertisseur analogique numérique (CAN) et une modulation de largeur d'impulsion (MLI) pour laquelle une attention particulière doit être accordée (pour éviter les cycles limites par exemple). La question cruciale du CAN est de parvenir à une résolution suffisante tout en maintenant la consommation d'énergie la plus faible possible. La ligne à retard ou les architectures hybrides sont des solutions possibles. Tous les CAN proposés ne mesurent que le voisinage de la tension de référence (notion de structure à fenêtres). La conception de CAN ne tombe pas dans le cadre de cette thèse.

Grâce à l'approche basée sur des "look-up tables", l'implémentation du régulateur linéaire, notamment le régulateur PID en mode tension, bénéficie d'avantage en termes de coût de ressources matérielles. Cependant, leurs performances dépendent généralement du point de fonctionnement, tel que la présence d'éléments parasites, la variation de la charge en fonction du temps ou la variation de la tension d'alimentation peuvent détériorer le comportement de la régulation. La commande non linéaire par mode de glissement offre de bonnes performances de régulation et présente des algorithmes relativement simples. Elle fera l'objet du Chapitre 2. Avec la connaissance du courant dans l'inductance, une structure de commande multi-boucles peut être adaptée : une boucle interne en courant et une boucle externe en tension. Cette méthode augmente l'efficacité du régulateur avec les avantages inhérents comme la protection contre les surintensités. La commande dite *dead-beat* et le contrôle en courant programmable sont largement utilisés pour la boucle de

courant interne. Cet algorithme de contrôle calcule, à chaque période d'échantillonnage, le rapport cyclique à l'aide d'un modèle discret du convertisseur, pour s'assurer que le courant dans l'inductance atteint la référence à la période suivante.

Une modulation numérique à largeur d'impulsion (MNLI) à haute résolution est une condition nécessaire pour éviter les oscillations de cycles limites (OCL). Les lignes-à-retard ou les compteurs associés à des comparateurs font parties des architectures classiques mais nécessitent des fréquences d'horloge d'autant plus élevée que la fréquence de découpage du convertisseur augmente. Différentes solutions sont proposées dans la littérature : les méthodes basée sur les cellules de retard, les méthodes utilisant le moyennage multi-cycle ou les méthodes assistées par des ressources matérielles. Nous nous focalisons sur la modulation Σ-Δ qui sera analysée du point de vue temporelle et fréquentielle dans le Chapitre 4.

A la fin de ce chapitre, les produits les plus importants reflétant l'état de l'art de la conception de régulateurs sont présentés comme références.

Chapitre 2 Commandes pour des Convertisseurs Abaisseur et Elévateur de Tension

Ce chapitre se concentre sur la conception des commandes à haute efficacité énergétique, consacrée aux convertisseurs abaisseur et élévateur de tension. Les performances de la commande dédiée est critique pour l'efficacité de conversion. La commande adoptée doit fonctionner correctement dans l'état dynamique et l'état statique. L'implémentation physique doit être relativement simple. Par ailleurs les fréquences de découpage élevées (>100MHz) présentent un verrou fort pour la commande numérique.

Ce chapitre commence par une revue des commandes existantes pour un convertisseur abaisseur de tension comme les PID, RST et la commande par mode de glissement.

Une commande numérique dite tri-mode contenant un PID, un PID sous échantillonné et un RST a été étudiée. Une amélioration au niveau des transitions des états du contrôleur tri-mode est apportée en s'accordant avec les conditions des opérations du convertisseur abaisseur durant l'état stable, l'état repos (stand-by) et l'état transitoire.

Pour un convertisseur élévateur de tension où la non linéarité est plus importante, une commande linéaire PID et une commande non linéaire par mode de glissement sont synthétisées.

Une partie importante de notre travail s'intéresse à la consommation énergétique du contrôleur. L'objectif est de lier cette consommation aux performances de la commande. Toutes les commandes présentées dans ce chapitre sont intégrée au sein d'un ASIC afin de vérifier l'éligibilité d'une commande numérique donnée dans le cadre d'un système de gestion d'énergie intégré ou Power System-on-Chip - PwrSoC (l'objet du Chapitre 6 et Chapitre 7).

Chapitre 3 Commande Directe avec Deux Etats de Prédiction

Un nouveau contrôleur numérique basé sur le principe de la commande prédictive est proposée pour le convertisseur abaisseur de tension à haute fréquence de découpage. Par rapport à la commande prédictive traditionnelle en mode courant, la prédiction du courant de l'inductance et de la tension de sortie ont effectuées en même temps, en ajoutant une variable de contrôle au signal MNLI (modulation numérique de largeur d'impulsion ou DPWM). Ceci accélère la vitesse de convergence pendant les états transitoires, tandis que la rejection des perturbations de la charge et le suivi de référence sont conservées avec d'excellentes performances.

Cette commande nécessite des informations sur la tension aux bornes de la capacité de sortie et la variation du courant de l'inductance en entrée. Un algorithme d'estimation est proposé afin de réaliser cette commande sans ajouter des capteurs physiques.

L'analyse du fonctionnement de ce contrôleur illustre des performances meilleurs comparant aux celles des contrôleurs PID, RST ou par mode de glissement.

Chapitre 4 Quantificateurs et des Blocs Périphériques

Pour la commande numérique, les deux quantificateurs, MNLI et CAN, sont utilisées comme les interfaces entre le contrôleur et l'étage de puissance. Des quantificateurs de résolution insuffisante peuvent provoquer des oscillations de cycles limites ou OCL. Le défi pour la conception d'une approche de MNLI dépend non seulement de l'exigence de sa résolution, mais aussi de la faisabilité de l'implémentation en termes de consommation acceptable d'énergie. Les deux techniques possibles comportent la génération de petits intervalles par les techniques dérivées des lignes à retard et les techniques de moyenne dans le domaine temporel par la modulation Σ-Δ ou la décimation. En effet, les méthodes ci-dessous peuvent être considérées respectivement comme deux approches de génération pour la haute fréquence dans les domaines temporel et fréquentiel.

Le modulateur Σ-Δ pour MNLI consomme moins d'énergie que les lignes à retard. Une analyse en boucle fermée est donnée afin de démontrer l'effet du modulateur Σ-Δ. Le modulateur introduit des ordres d'excitation continue dans le spectre de la tension de sortie du convertisseur DC-DC, qu'il faut rejeter.

La structure dite 1-1 MASH Σ-Δ de MNLI est considérée dans ce chapitre. Conformément à l'analyse, il n'y a pas d'amélioration de la réduction du bruit, comparée à une MNLI Σ-Δ de second-ordre, bien que la performance dynamique soit prévue pour être améliorée. Alors un bloc de décimation est ajouté à la structure 1-1 MASH Σ-Δ si bien qu'il puisse effectivement réduire l'effet des marques lentes sans trop de ressources matérielles supplémentaires. Toutes les analyses durant des états stationnaire et transitoire seront données avec les résultats expérimentaux.

Le détail qui concerne l'implémentation du CAN concerne l'architecture de la ligne en retard et la fenêtre de capture. Comme le CAN n'est pas l'objet principal de ce travail, il ne sera pas élaboré dans ce chapitre. La boucle à verrouillage de phase (PLL: Phase Locked Loop) est un autre bloc nécessaire pour implémenter un ASIC. Ce chapitre donne une approche synthétique, adoptant la cellule à retard qui est insérée dans un oscillateur contrôlé en tension assisté par un convertisseur à pompe de charge comme détecteur de phase.

Chapitre 5 Résultats Expérimentaux sur FPGA

Ce chapitre présente les résultats expérimentaux des contrôleurs et MNLI discutés dans les chapitres précédents. Tout d'abord, les platesformes expérimentales pour les convertisseurs abaisseurs et élévateurs de tension sont introduites. Ensuite, les résultats expérimentaux vérifient les améliorations de la MNLI proposé. Les résultats expérimentaux de la commande directe avec deux états de prédiction pour le fonctionnement convertisseur abaisseur de tension à la fréquence de découpage de 1MHz, sont donnés en comparaison avec des PID, RST et par mode de glissement. Les essais avec une fréquence de découpage de 4MHz sont également réalisés pour montrer les meilleures performances du contrôleur proposé. Enfin, les performances du convertisseur élévateur de tension sous les contrôleurs PID et par mode de glissement sont fournies. La fréquence de découpage de 4MHz n'est limitée que par les éléments discrets du convertisseur DC-DC. Les simulations de l'ASIC montreront un fonctionnement correct vis-à-vis de fréquence de découpage supérieur à 50 MHz.

Chapitre 6 Intégration sur ASIC

Ce chapitre reprend d'abord le flot de conception *top-down* des circuits intégrés numériques et mixtes analogiques-numériques. Basé sur ce flot, deux ASICs ont été élaborés pour permettre une évaluation de la performance et l'efficacité des contrôleurs numériques, plus poussée que sur FPGA. Nous avons implémenté trois commandes dans une première puce (contrôleurs PID, RST et par mode de glissement). Certains circuits périphériques nécessaires sont aussi intégrés comme les MNLI, BVP (boucle à verrouillage de phase) et une interface série-parallèle.

Le langage VHDL-AMS est utilisé pour construire le système de signaux mixtes. Il est possible d'évaluer les performances dynamiques et statiques durant la phase de conception de ASIC. C'est aussi la meilleure méthode pour estimer la performance des commandes avant l'implémentation actuelle sur FPGA ou ASIC.

Le premier ASIC est la puce de test qui implémente des stratégies de contrôle numérique pour le convertisseur abaisseur de tension. Sont également portés les machines d'état de haut-niveau de gestion des commandes ainsi que la gestion du contrôleur tri-mode. En l'absence du bloc DCM sur FPGA, un bloc MNLI, basé sur le modulateur de second-ordre Σ-Δ, est implémenté. Le test de cette première puce requière une carte mère (Xilinx XC3S500E) pour fournir les signaux manquants nécessaires pour compléter les blocs et construire le contrôleur tri-mode. Les résultats expérimentaux vérifient les fonctionnements de la boucle fermée à la fréquence de découpage jusqu'à 2MHz. Le convertisseur est régulé sur une large plage de sortie avec des performances dynamiques acceptables.

Le second ASIC embarque des stratégies de contrôle non seulement pour le convertisseur abaisseur de tension mais aussi pour le convertisseur élévateur de tension. Les commandes PID et par mode de glissement sont programmées pour ces deux convertisseurs. Le modulateur 1-1 MASH Σ-Δ proposé, est intégré dans tous les contrôleurs implémentés, pour alléger l'exigence en fréquence de l'horloge. Nous avons aussi intégré une BVP pour fournir une horloge haute fréquence avec quatre changements de phase, comme proposé par un module DCM sur FPGA. Afin d'implémenter les paramètres programmables qui permettent d'ajuster la fonction de transfert des contrôleurs, un récepteur de données série-parallèle, avec une interface de type périphérique UART de micro-contrôleur, est adapté. La lecture des paramètres dans ce module possède aussi sa propre horloge synchrone et la possibilité de réinitialiser les signaux. Chaque paramètre est adressé et l'écriture de l'ensemble des registres s'effectue à travers un registre à décalage en tampon sur la réception. La comparaison des performances et l'analyse de chaque contrôleur sont données à la fin de ce chapitre.

Chapitre 7 Evaluation de la Consommation Energétique

Comme nous nous approchons d'un prototype de type PwrSoC, la mise à l'échelle dans la technologie de semiconducteur permet de mieux apprécier la consommation énergétique des contrôleurs numériques. Le but est de définir les cas d'utilisation rationnelle des contrôleurs numériques comparés aux contrôleurs analogiques. Il y a d'un côté un effort pour abaisser la consommation. Il convient alors de savoir quel convertisseur DC-DC pourrait bénéficier des avantages d'un contrôleur numérique à rendement énergétique égal (par rapport à un contrôleur analogique). On considère ici la puissance de sortie du convertisseur et sa fréquence de découpage.

La puissance qui est consommée par le contrôleur numérique prend de 4,5% à 9,5% du total des pertes des convertisseurs DC-DC testés. Basé sur les résultats expérimentaux d'après le test des puce (CMOS 0,35μm), la consommation d'énergie du contrôleur en tri-mode avec la MNLI est donc analysée pour bâtir un modèle de consommation d'énergie effective du contrôleur numérique. Ce modèle aide ensuite à estimer la consommation du contrôleur numérique dans divers cas, et suggère l'impact sur l'efficacité énergétique globale du convertisseur DC-DC. Des résultats sont commentés en fonction d'une puissance de sortie donnée et de la fréquence de découpage.

Selon les résultats, l'adaptation du contrôleur tri-mode et du contrôleur par mode de glissement offre des performances dynamique et statique acceptables, avec une consommation réduite, comparable à celle de contrôleurs analogiques. Par conséquent, le contrôleur numérique peut permettre d'atteindre dans certains cas de convertisseurs, une efficacité énergétique comparable à celle de leurs homologues analogiques mais avec un gain important en fonctionnalité et en performances.

Conclusion et Perspectives

Conclusion

Le premier objectif de la thèse est la proposition de structures de contrôleurs numériques compatibles avec des convertisseurs à haute fréquence de découpage. Pour des questions pratiques, le prototypage discret limite l'ambition à 4MHz. Avec quelques efforts, il doit être possible d'atteindre des tests à 10MHz en circuits discrets pour le convertisseur, mais ceci ne changera pas fondamentalement les performances des contrôleurs.

Visant la vérification sur ASIC pour les PwrSoC, la question centrale est le prix à payer en consommation énergétique pour bénéficier des performances accrues de contrôle (par rapport à un contrôleur analogique). Un effort doit viser l'implémentation numérique des contrôleurs dans un souci de minimisation de la consommation énergétique.

Les contributions peuvent être résumées ainsi:

- une amélioration de la consommation est proposée à travers un contrôleur tri-mode destiné à réaliser un compromis entre la réponse dynamique et les pertes. Un contrôleur RST robuste anticipe les hautes performances dynamiques et est adopté en l'état transitoire; le contrôleur PID est appliqué en l'état stable; le même contrôleur PID est cadencé avec les paramètres appropriés en basse fréquence en l'état repos;
- les contrôleurs PID et par mode de glissement sont successivement conçus et implémentés pour le convertisseur élévateur de tension. Ils sont testés sur la plateforme FPGA;
- le contrôleur prédictif de courant et de tension est proposé pour un SMPS à haute fréquence de découpage. La prédiction du courant de l'inductance et de tension de sortie est effectuée en ajoutant un paramètre de commande supplémentaire dans le signal MNLI. La commande directe avec deux états de prédiction préserve les mérites du contrôleur prédictif de courant standard et permet l'amélioration des performances dynamiques en maintenant une rejection excellente des perturbations de la charge et un bon suivi de référence;
- une fonction MNLI hybride est construite à partir des limitations rencontrées dans la mise en œuvre de la correction par Σ-Δ. La marque basse-fréquence dans le signal de sortie est expliquée;
- une architecture améliorée par rapport aux architectures traditionnelles (dit 1-1 MASH Σ-Δ DPWM) est synthétisée sans détérioration de la stabilité en boucle fermée ainsi qu'en préservant un coût raisonnable en ressources matérielles;
- une BVP est proposé pour offrir des sources d'horloge déphasées;
- un banc d'essai en VHDL-AMS est construit pour évaluer les performances de chaque contrôleur numérique;
- les paramètres des contrôleurs ont été rendus ajustables dans les ASICs. Ceci garantit un réglage minutieux pour offrir une immunisation vis-à-vis des perturbations du bruit, ou le réglage des paramètres important en fréquence de découpage élevée;

- deux circuits intégrés numériques ont été conçus pour porter une implémentation améliorée du contrôleur tri-mode vis-à-vis de la faible puissance et la haute fréquence de découpage du convertisseur abaisseur de tension (CMOS 0,35μm);
- les performances des contrôleurs implémentés sont comparés avec celles d'homologues analogiques;
- basé sur les résultats expérimentaux, les consommations énergétiques des contrôleurs implémentés sont évalués pour construire un modèle de consommation. Ce modèle permet d'estimer l'impact d'un contrôleur numérique sur l'efficacité énergétique d'un convertisseur DC-DC et vis-à-vis d'homologues analogiques pour des conditions d'exploitation similaires;
- les résultats expérimentaux ont confirmé ceux obtenus en simulation. L'implémentation sur ASIC s'est révélée fonctionnelle et a permis de confirmer les résultats sur la plateforme FPGA. Le modèle énergétique confirme la possibilité de concevoir des contrôleurs numériques peu énergivores pour une grande gamme de convertisseurs, même de faible puissance et de fréquence de découpage élevée.

Perspectives

La technologie CMOS 0,35μm n'est pas la plus appropriée pour vérifier des résultats vis-à-vis de PwrSoC qui s'implantent jusqu'en CMOS 32nm. Pour autant les puces disponibles vont permettre d'affiner certains résultats.

Plusieurs perspectives peuvent être données:

- l'estimation ou l'observation de courant;
- l'étude de saturation du courant de l'inductance pour la commande directe avec deux états de prédiction;
- l'étude de robustesse et de stabilité;
- l'extension de l'étude aux convertisseurs pour le mode de conduction discontinue;
- l'implémentation de la commande directe avec deux états de prédiction sur ASIC et l'extension à d'autres convertisseurs;
- la vérification du modèle énergétique en présence d'un CAN dédié à contrôleur numérique;
- l'implémentation des algorithmes en CMOS avancé;
- la réalisation d'un PwrSoC à commande numérique.

Introduction

Research Background

The booming demand for mobile electronic devices raises the concern of the stability and accuracy for the power supply with high efficiency. Meanwhile, very large-scale integrated circuits (VLSI) suffers from inexistent or inefficient power management inside the chip so far. Low power electronic requirements are pushing for local and global solution to optimize energy consumption (generally from an external battery). Current industrial practice is to place a power management chip on the same board as the system-on-chip (SoC) and the power chip manages the battery energy to create the necessary voltages for the SoC operation. Inside the SoC, only local techniques are implemented to limit energy leakage. A global optimization requires that power management is integrated inside the SoC. A processor will be dedicated to operate a power management algorithm by sensing adequate quantities all over the chip and acting the power supply of each block. Power management is then built upon several blocks including analog blocks (sensors), digital blocks (digital signal processor-DSP) and power blocks (class-D voltage regulators or at least low-dropout regulator-LDO).

Although the pervasive power management approach is analog, it cannot benefit from the progress in advance complementary metal-oxide-semiconductor (CMOS) technologies. Digital control for low-power switched-mode power supply (SMPS) opens up the possibility of the integration of high switching frequency power conversion system [Liu 09, Martin 95, Patella 03, Lukic 07, Ahmad 10, Soenen 10]. Compared with the analog counterpart, the digital approach allows the development of digital controller which cannot be realized in the analog domain. For example, specific nonlinear controller can boost the dynamic response to the perturbation of power train [Yousefzadeh 08, Hu 06, Babazadeh 09, Feng 09], the PMBus power management protocol enables the communication-level and system-level integration [White 06], the active efficiency monitoring [Saggini 08] and the digital autotuning [Zhao 07, Lukic 09, Stefanutti 07] can improve

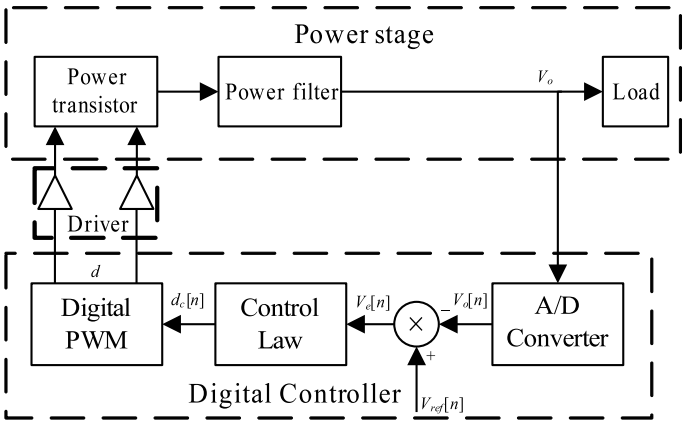


Figure 1: Block diagram of a digitally controlled buck converter

the control performance. Moreover, digital control exhibits inherent advantages of digital integrated circuit, for instance, insensitivity to the process-voltage-temperature (PVT) variations, design reuse and reprogrammability that greatly accelerate the time-to-market (TTM). Digital controller is therefore regarded as an attractive candidate to achieve better performances.

Even though digital controller can be used to obtained aforementioned advantages, there are some issues that prevent it becoming pervasive in applications such as power converter and motor driver. Most of the disadvantages for a digitally controlled buck converter come from the building blocks of the digital controller itself as shown in Fig. 1. The digitization of the control-law, also known as compensator, requires the aid of two quantizers including analog-to-digital converter (ADC) and digital pulse-width-modulator (DPWM). ADC plays an important role in digital controller with respect to steady-state error, output ripple value and limit cycle oscillation (LCO). Compared to analog approach, this extra module should be designed to minimize the power consumption that prohibits the use of traditional ADCs such as flash ADC, pipeline ADC and Σ-Δ ADC. So the delay-cell-based ADCs are the trade-off to reduce power consumption to some extent, although the resolution and precision require further tuning [Patella 03, Lukic 07]. Therefore, the appropriate method to implement an ADC devoted to power controller is still a focus of study. In this thesis, the quantized digital output is compared to a digital reference after the ADC to generate the digital error signal for control-law. If the reference value is provided in analog form, the comparison can be performed before the ADC so that ADC only quantizes the error signal. DPWM is another necessary building block in digital controller. Apart from the analog approach, DPWM should be designed only with digital standard cells. Generic hardware-description-language (HDL) can be synthesized to achieve such function by a combination of counter and comparator with the aid of a system clock that seems unachievable for mainstream CMOS process. Even if possible, we cannot afford the large power consumption brought by an ultra-fast system clock. Delay-cell and dither are regarded as two of the most important approaches to alleviate the high frequency requirement. If an anti-LCO condition [Peng 04] cannot be satisfied, the LCO will occur. Such phenomenon also brings about some limitations on the feedback loop with respect to the resolution of two quantizers, the integral gain of the control-law and so

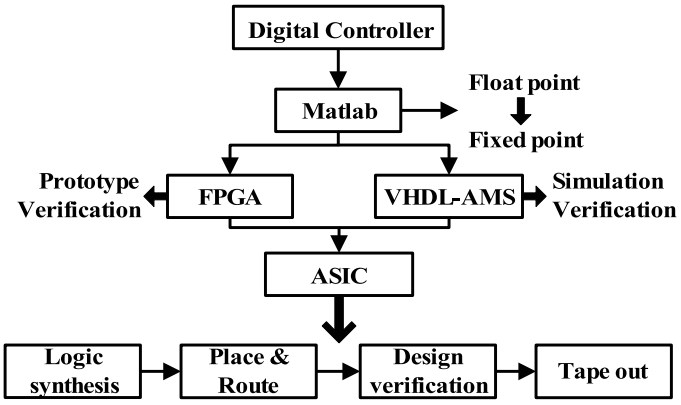


Figure 2: General design flow for the digital controller

on. Due to the nonlinear characteristics of the ADC and DPWM, it is normally difficult to predict the closed-loop behavior. Simulation relies on a reliable software to estimate the actual operation.

[Wei 96a] firstly investigates the power dissipation of each part in digitally controlled power converter under different regulated voltages. Building blocks including driver, buck converter, controller and load are taken into consideration. The implemented digital PID controller consumes from 4.55% to 9.44% of the total power. It is about the sum of the other components regardless of the load consumption. According to the analysis result, the way to reduce the power consumption of a digital controller becomes a critical issue to increase the total efficiency of the power conversion function. Meanwhile, it is not wise to realize power reduction by limiting the control performances at the risk of losing more power in other components. Such a trade-off requires a lot of experiments to estimate the performance of candidate controllers so as to achieve a relative optimal choice.

In order to better employ the advantage of digital controller and alleviate the aforementioned design pressure, this dissertation is involved in some issues that will be analyzed in general in the next section.

Design Methodology

As shown in Fig. 2, FPGA and ASIC are two main platforms to implement the digital controller and verify the performance. Based on a current or proposed control algorithm, the float-point simulation has to be re-modeled to the fixed-point simulation due to its better interpretation of the experimental results in FPGA and ASIC. With the aid of some external circuits, FPGA performs the prototype verification. On the other hand, FPGA is regarded as a feasible verification approach before ASIC implementation. Provided that it is impossible to build up an FPGA prototype, the VHDL-AMS based simulation becomes a feasible verification approach to interpret the ASIC behavior. The mixed-signal part can be modeled by VHDL-AMS. The netlist of the pure digital part can be updated according to different ASIC design steps. If all the verification results satisfy the design specifications, we can start to design the ASIC.

To perform the logic synthesis, that is, to transfer the RTL VHDL code to gate-level netlist, is the first issue. Such a synthesis must satisfy the timing, area and power constrains. According to the gate-level netlist, the layout can be generated by placing and routing standard cells. Before taping out the chip, layout verification must be performed including DRC, LVS, parasitic parameter extraction and post-layout simulation. Fig. 2 shows the general design flow of digital IC. Detail can be found in Section 6.1.

Focus of This Research

The research concentrates on two issues of digitally controlled power converter in terms of building-block-level and system-level. The optimization of existing building blocks with respect to the performances is based on the closed-loop analysis. The main task in the building-block-level is to maintain a good control performance without introducing extra perturbation with the aid of improved compensator and quantizers. At system-level, the integration of the improved digital controller provides the experimental prototype so as to evaluate the feasibility in terms of performance and power consumption. Moreover, the high switching frequency makes the passive components smaller. It is also important for the further chip integration of the whole power conversion system. Firstly, a brief introduction of the improvements in the building-block-level is introduced as

- Most popular digital controllers are developed to make a comparison in terms of cost and performances. This thesis refers to the following controllers: PID, RST, sliding-mode (SM) and dead-beat controllers.
- With respect to the dynamic performances and power consumption of the PID and RST controllers, an improved power-aware tri-mode control is proposed to achieve a better trade-off between the two factors.
- In order to enrich the target DC-DC converters, especially to some non-minimum phase systems exhibiting more serious nonlinearity, PID and SM controllers are implemented in a boost converter operating at high switching frequency. This approach illustrates the performances, and anticipate a more common design approach of implemented controllers.
- Controller is a critical part to achieve better steady-state and transient-state performances. The thesis proposes a direct control with dual-state-variable prediction (DDP control) devoted to high switching frequency buck converter. Unlike the double closed-loop control method, the predictions of the inductor current and the capacitor voltage are performed at the same time. The DDP controller preserves the merits of the predictive current control, allows to further enhance the dynamic performances and maintains an excellent rejection of the power supply perturbation.
- To design a high effective DPWM, delay-cells and dither are main orientations with emphasis on the generation of tiny interval by process-based delay and hardware algorithm respectively. Dither approach does not need extra high density series of delay-cells, and can be implemented with less hardware resources. Our research will focus on one of the controlled dither generation approaches called Σ-Δ. A dithered MultistAge-noise-SHaping

(DMASH) architecture is proposed to reduce the idle-tone effect to some extent while maintaining the noise-shaping effect and closed-loop stability.

– A prototype of the global clock generator is also taken into consideration to provide an on-chip system clock intellectual property (IP) for the system integration in the future.

Then the system-level tasks focus on the following issues as

– The construction of the system-level model makes it easy to verify the performances of the proposed building blocks. VHDL-AMS is adopted here to simulate the digital parts (register-transfer level-RTL in VHDL) and analog parts (AMS) simultaneously. Beside behavioral simulation (Matlab for example), VHDL-AMS can better reflect the influence of each block.
– Referring to the simulation results, the design of isolated digital controller ICs is to accumulate feasible IPs for integration. Meanwhile, the information on the performances and power consumption can be obtained from the realized application-specific integrated circuit (ASICs).
– An estimation of power consumption obtained from the digital power analysis software can be used to compare to that from the experiment. So we can build a feasible power consumption model for each controller under different CMOS technologies. The power prediction can help designers to evaluate the efficiency of the implemented digital controller compared to its analog counterpart.

Thesis Outline

The dissertation is organized as follows

Chapter 1 reviews the existing solutions for the design and implementation of the digitally controlled power converter in terms of control-law and DPWM. Important progresses and corresponding limitations with respect to linear, nonlinear and dead-beat control-laws are reviewed. Then a section summarizes two main types of DPWM as well as their improved structures. This chapter ends with a summary of some available commercial products.

Chapter 2 firstly reviews the PID, RST and SM controllers for the buck converter. An improved power-aware tri-mode control using PID and RST control-law is proposed in order to pursue low power consumption under normal operation. PID and sliding-mode controllers are also implemented in the boost converter. It is also the foundation of the chip integration for the corresponding controllers.

As another major contribution of the thesis, the DDP controller is proposed in Chapter 3 to achieve better dynamic performances than the reviewed controllers. The PWM signal regulated by two variables assures such performances without any physical inductor current sensor.

Based on the existing closed-loop LCO analysis, Chapter 4 proposes a simulation platform to pre-evaluate the noise-shaping effect of adopted Σ-Δ DPWM under DC excitation. The behavior of the noise-sensitive DC input is also summarized in this section. Then an 1-1 DMASH Σ-Δ DPWM is proposed to further reduce the idle-tone effect. This chapter also discusses a feasible on-chip system clock generator by a four-phase shift phase-locked loop (PLL).

Experimental results in field-programmable gate array (FPGA) for DPWM and proposed controllers are given in Chapter 5.

Two ICs are fabricated in $AustriaMicrosystemS$ $0.35\mu m$ CMOS process. PID, RST and SM controllers are designed for the buck converter, while PID and sliding-mode controllers are integrated for the boost converter. The on-chip DPWM, system clock generator and a parameter read-in module are also included. Chapter 6 discusses the system-level simulation, design flow and the test platforms. Experimental results are also given in this chapter.

The analysis of the chip power consumption obtained from experiment and simulation provides a guideline to anticipate power consumption of the digital controller. It also reveals the efficiency of the digital controller compared to its analog counterpart. Chapter 7 tries to classify each type of power consumption and clarify their contributions to the total power consumption of the converter. A power consumption model is built to estimate the power consumption of each controller as the switching frequency increases and different technologies are considered.

The last chapter concludes the thesis and suggests possible new research directions.

Chapter 1

State of the Art

In order to benefit from the advanced CMOS technology and the inherent merits mentioned in the introduction part, a lot of ideas are proposed to promote digitally controlled synchronous power converters in which the buck converter and the boost converter are shown in Fig. 1.1. Located in the central position of the feedback loop, the control-law is designed to realize the advanced control algorithm in a digital manner. Two quantizers, ADC and DPWM, therefore become mandatory as an interface between analog and digital world. Away from the analog counterpart, the digital closed-loop operation calls for a serious observation on all the latter three parts along with the quantization effects and related LCO. The following sections will introduce a wide range of the latest articles about above issues.

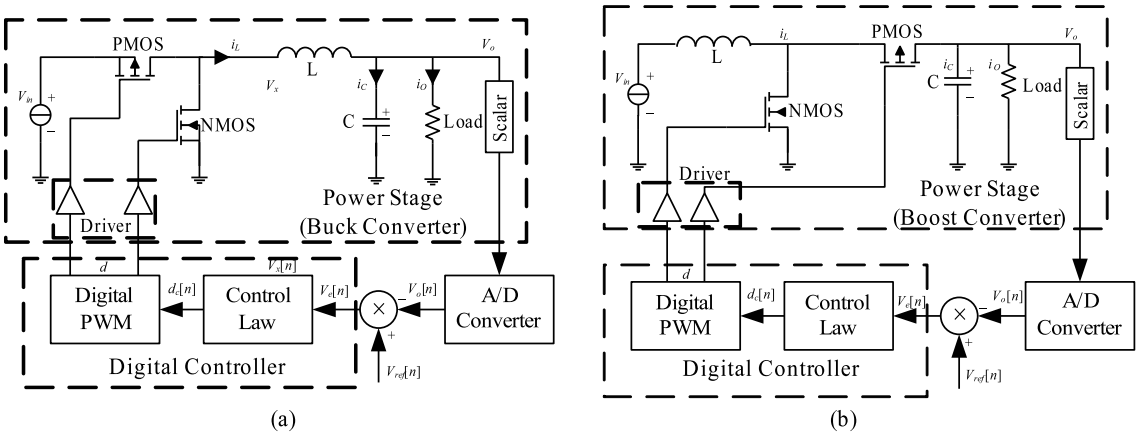


Figure 1.1: Digitally controlled synchronous buck converter (a) and boost converter (b) respectively

Table 1.1: Summary of important ADCs

Architecture	Power (μA/MHz)	Quantization step (mV)
Ring-oscillator [Xiao 04]	74	16.0
Nonlinear self-strobe [Lukic 07]	8	15.0
Programmable self-strobe [Parayandeh 08]	28	4.4
Optimum delay-based [Barai 10]	6	12.5
Frequency domain Σ-Δ [Ahmad 10]	14	7.8

Table 1.2: Summary of important ADCs (cont'd)

Architecture	Area (mm^2)	Process μm	Target converter
Ring-oscillator	0.150	0.25	0.5MHz buck
Nonlinear self-strobe	0.108	0.18	12.0MHz buck
Programmable self-strobe	0.011	0.18	1.5MHz buck
Optimum delay-based	0.080	0.50	1.0MHz buck
Frequency domain Σ-Δ	0.200 (estimated)	0.18	0.5MHz buck

The system integration of the discrete ADC component is not within our scope. Only a general introduction about the ADC applied to digital controller is given. Located in the front-end of the digital feedback loop, ADC is an additional module in digitally controlled SMPS compared to the analog counterpart. As the necessary interface between the analog variable in the power stage and the digital controller, ADC itself must maintains acceptable static and dynamic performances, while keeps power consumption as small as possible. A traditional classification of ADCs presents the achievable performances and the applications [Murmann 08]. Only from the issues of the effective resolution and the achievable conversion frequency, SAR and pipeline ADC are two feasible ADCs for power converter [Hariprasath 10, Gubbins 08]. However, both of these two ADCs require the aid of switch-capacitors array and are prone to an inherent conversion latency that possibly degrades the dynamic responses. The necessary analog components also prevent such ADCs because of its incompatibility with the digital design.

According to above discussion, the general purpose ADC is too expensive in terms of power consumption and chip area. Even the typical full range ADCs, such as pipeline ADC, are considered more complex than the analog controller. The proposals of windows ADC and delay-line implementation are proven to be feasible solutions. Several prototypes are proposed based on the two ideas. Table. 1.1 and 1.2 summarize the existing developments and their performances. It still arouses many discussions in order to further increase the power efficiency, reduce chip area as well as maintain acceptable performances.

In next sections, we will focus on important control-laws and feasible DPWMs dedicated to digitally controlled power converter.

1.1 Digital Control-law

The digital control-law permits the implementation of control algorithms with high efficiency that is unavailable for the analog control-law. Many papers discussed optimized solutions. Taking advantages of its simplicity and reasonable control effect, linear control has been used for high-frequency (MHz range) and low-power (several millwatt) SMPS [Lukic 07, Liu 09]. As typical examples, the voltage-mode PID control and derived digital control-laws can be implemented by mapping continuous s-domain to discrete z-domain or employing direct digital design approach utilizing the difference equation with reprogrammable coefficient [Al-Atrash 07, Patella 03]. As another method, SM control is an alternative to realize the control behavior which exploits the inherent variable structure system (VSS) of DC-DC converter. Classic HM-based SM control operates at a variable and high switching frequency [Nguyen 95]. That will lead to excessive power losses, electromagnetic-interference (EMI) generation and filter design complications. In order to keep a fixed switching frequency, a PWM-based SM control has been proposed [Chu 08, Tan 08a, Tan 08b]. Hybrid control consisting of both the linear and nonlinear control-laws is accommodated well to both the static-state and transient-state operations [Perry 07, Hu 08, Yousefzadeh 08]. With the knowledge of inductor current, a digital control technique based on a two-loop predictive deadbeat control concept is developed for DC-DC SMPS [Bibian 02]. This kind of control is classified as current-mode control that is proven to be effective with the inherent advantages including overcurrent protection and excellent audiosusceptibility [Chen 03, Chattopadhyay 06, Bibian 02]. In the following sections, a general review of popular digital control methods is presented.

1.1.1 Linear Control

Obvious advantages of digital controller mentioned in the introduction part as well as the lower price and higher density of IC compel the designer to take the digital implementation into consideration. Among the digital controllers, linear control is regarded as an easy implementation with low power consumption. Digital redesign (also known as digital via emulation) and direct digital design are two approaches to design digital linear control. Derived from the analog control in continuous s-domain, the digital redesign requires a minimal work in the discrete z-domain. In effect, based on the existing linear control-law in analog domain, a mapping from s-domain to z-domain requires one of the variety of discretization methods, such as backward Euler and bilinear methods. However it usually suffers from the discretization effects and disregards of acquisition delay and zero-order-hold (ZOH) delays [Liu 09]. Direct digital approach is designed in z-domain using step invariant model of a continuous time plant when ZOH is used. [Maksimovic 07] presents the small-signal discrete model for DPWM-based DC-DC converter in continuous conduction mode (CCM).

As a typical linear control, PID control is the first realized control-law for IC application [Prodic 02]. The transfer function of PID in s-domain, $G_c(s)$, is mapped into z-domain using pole-zero mapping method as the following form

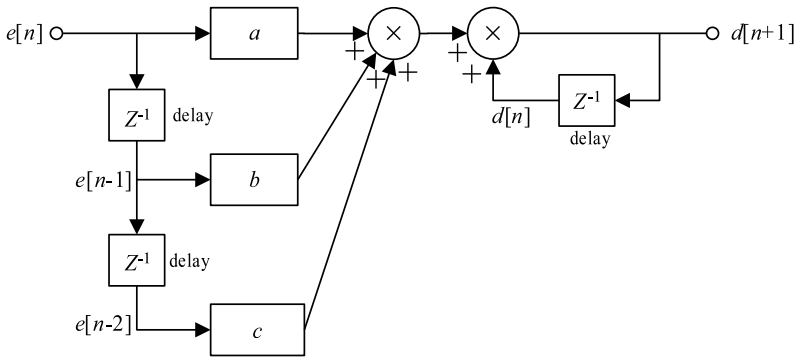


Figure 1.2: Block diagram of the digital PID control [Prodic 02]

$$G_c(z) = \frac{a + bz^{-1} + cz^{-2}}{1 - z^{-1}} \tag{1.1}$$

where coefficients a, b and c are determined by the pulsation ω_{cr} and the damping ratio ζ_{cr} of the desired closed-loop transfer function. The discrete-time equivalent of the PID control-law is of the following form

$$d[n] = d[n-1] + a \cdot e[n] + b \cdot e[n-1] + c \cdot e[n-2] \tag{1.2}$$

where $e[n]$, $e[n-1]$ and $e[n-2]$ are the error signals generated by an ADC and a digital reference. $d[n]$ and $d[n-1]$ are duty cycles in the current and previous period respectively. The corresponding implementation is shown in Fig. 1.2.

Coefficient multiplication is the intuitive design approach that requires large chip area and possibly introduces extra computation delay. In order to solve the problems, look-up tables (LUTs) are used here taking advantage of the binary computation [Prodic 02]. The LUTs-based PID control is of significantly low power consumption. This architecture is easy to implement in both FPGA and ASIC. Whereas this configuration is not compatible with the variable switching frequency architecture due to the dependency between the switching frequency and delay-cell update period.

As an important improvement of LUTs-based PID control, [Hu 08] proposes a LUTs-assisted discrete-time control-law based on nonuniform analog-to-digital quantization presented in Fig. 1.3. An interesting research is examined on how to choose the input bin value {a1, a2...} and the corresponding output quantization level {b1, b2...} as shown in Fig. 1.4 in order to avoid the zero-error bin that may affect the system stability margins. Describing functions and the circle criterion are used to analyze how to preserve acceptable stability margins. Based on the linear controller, a search procedure to determine the nonuniform quantizer parameters {a1, a2, b1, b2} is illustrated in a proposed flowchart. In each step, a transient simulation is performed to check the describing function bound, and to evaluate a figure of merit for the transient response. The nonuniform ADC-based controller results in a significantly smaller maximum voltage deviation and a significantly shorter response time along with low budget of hardware resource. According to the experimental results, the controller mimics a PI control during steady-state; however, when

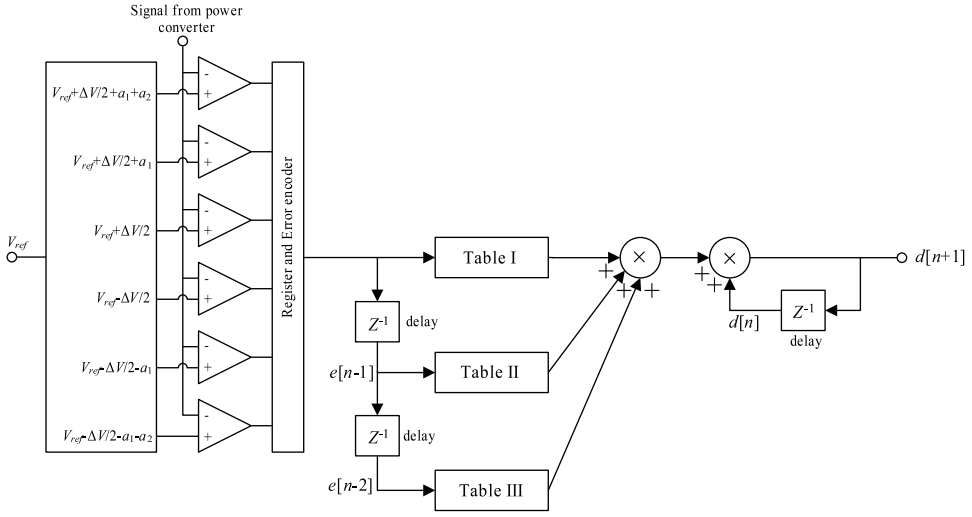


Figure 1.3: Block diagram of the nonuniform ADC-based nonlinear control [Hu 08]

either the output voltage error or the derivative of the output voltage is relatively high, the duty cycle varies at a faster nonlinear rate.

Some other improvements are made to enhance the performance of the digital PID control [Yousefzadeh 06b, Takayama 06, Lukic 07]. [Yousefzadeh 06b] proposed a third-order compensator with improved transient response and disturbance rejection performances compared to the classic second-order ones. [Lukic 05, Lukic 07] proposed a dual-mode PID control. Either steady-state mode or dynamic mode is activated according to the current operation state in order to achieve high control efficiency. A mode choice logic fulfilled this task that is capable of eliminating potential stability problem related to the dynamic switching between different modes.

Linear control is an easy and effective digital control approach with acceptable performances and low power losses as reviewed in this section. However, the nonlinear control can benefit the advantages from its validity in large regions of state-space as opposed to linear control that are only valid in the neighborhood of an operating point. In the next section, we will review nonlinear control-laws that can be compatible with digital design.

1.1.2 Nonlinear Control

One of the most important advantages to digital control is that it is very suitable to implement the complicated nonlinear control algorithm to further improve the dynamic performances compared to that of the linear ones because of the independence with operating point and wide dynamic operation range. However, many nonlinear control-laws are not compatible with digital design approach, especially can not operate in the fixed high switching frequency for integrated application. This section only cites some important feasible cases.

PWM-based SM control is an important type of nonlinear control for fixed switching frequency DC-DC power converters [Tan 05b, Tan 05a, Tan 08a]. The analog SM control can be mapped easily to the corresponding digital form [Ramos 03, Guo 10]. Section 2.3 and 2.4.2 will discuss the

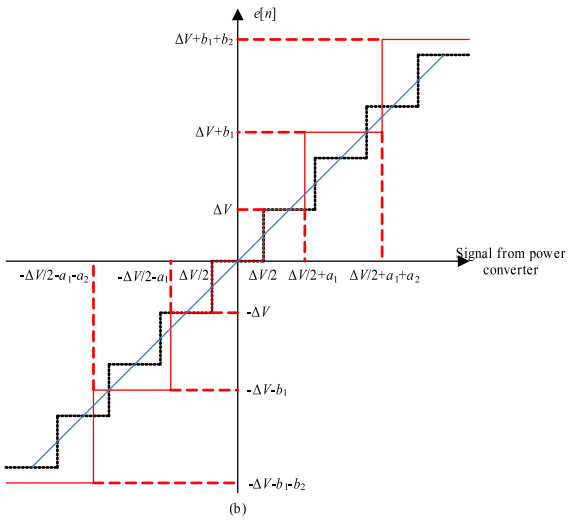


Figure 1.4: Quantizer characteristics of nonuniform ADC [Hu 08]

PWM-based SM control for digitally controlled buck and boost converters respectively. However, SM control still suffers from nonzero steady-state error. This problem can be alleviated to some extent by the double integral sliding surface proposed in [Tan 08b].

Compared to the stand-alone nonlinear control, a hybrid digital control is proposed as a combination of linear controller and nonlinear controller [Yousefzadeh 08]. A state machine based switching surface controller takes samples of the voltage error at the over-sampling rate so as to detect the state change while preserving a smooth transient between the two modes.

Most of the nonlinear controllers prefer benefiting from the fast response during transient-state while maintaining simple implementation as linear controller during steady-state. In the next section, the predictive current-mode control-laws are reviewed as another type of digital controller with good dynamic performances.

1.1.3 Predictive Dead-beat Control

Fig. 1.5 shows the block diagram of a traditional digital current-mode control. Inductor current prediction, or relevant quasi-prediction is widely used in dead-beat control [Bibian 02, Malesani 98] and current programmed control [Chen 03, Chattopadhyay 06, Trescases 07] in order to execute the control operation compared to the sensed inductor current I_L. This section will review one of the most important cases, dead-beat control.

Providing that the output voltage V_o is constant during the switching period as the topology shown in Fig. 1.5, the inductor current I_L at the end of one cycle can be expressed as

$$I_L\left(k+1\right)|_{d(k)} = I_L\left(k\right) + \frac{V_o}{L}\cdot T_e - \frac{V_{in}}{L}\cdot T_e\cdot\left(1-d\left(k\right)\right) \tag{1.3}$$

where $I_L\left(k+1\right)|_{d(k)}$ is the inductor current value at time $\left(k+1\right)\cdot T_e$ when apply the duty ratio $d\left(k\right)$. By setting $\Delta d\left(k\right) = d\left(k\right) - d\left(k-1\right)$, then the predictive inductor current variation can be obtained as

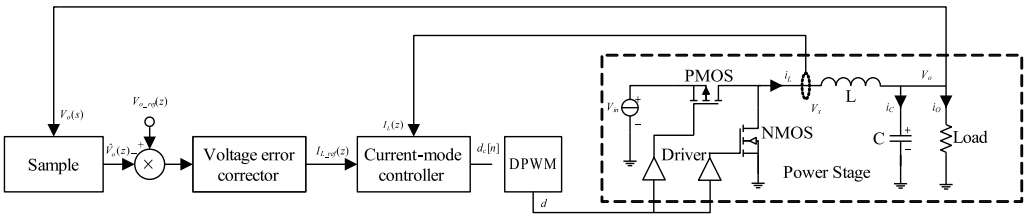


Figure 1.5: Block diagram of the digital current-mode control

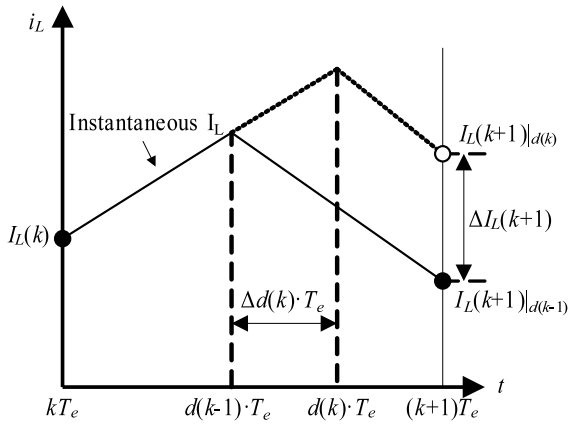


Figure 1.6: Inductor current during one switching period for dead-beat control

$$\Delta I_L\left(k+1\right)=\frac{V_{in}}{L}\cdot T_e\cdot\Delta d\left(k\right) \tag{1.4}$$

where $\Delta I_L\left(k+1\right)=I_L\left(k+1\right)|_{d(k)}-I_L\left(k+1\right)|_{d(k-1)}$. The result is represented in Fig. 1.6. Providing that $\Delta I_L\left(k+1\right)$ stands for the inductor current error that needs to be compensated, a duty cycle increment can be calculated based on (1.4). The following dead-beat control is therefore obtained as

$$d\left(k\right)=d\left(k-1\right)+\frac{1}{V_{in}}\cdot\frac{L}{T_e}\cdot\varepsilon\left(k+1\right) \tag{1.5}$$

where $\varepsilon\left(k+1\right)$ is the difference at $(k+1)\cdot T_e$ between the desired current reference $I_{L,ref}\left(k+1\right)$ and the value of current if the duty cycle were to be kept the same as in the previous switching period which is expressed as $I_L\left(k+1\right)|_{d(k-1)}$. The control concept can be expressed as follows: if the duty cycle $d\left(k\right)$ is calculated based on (1.5) and applied to the converter at kT_e, then the I_L will reach its reference value $I_{L,ref}\left(k+1\right)$ at $\left(k+1\right)T_e$. As a result, the current error at $\left(k+1\right)T_e$ will theoretically be zero. In other words, the control action is calculated such that the error is reduced to zero at the end of the switching period.

Due to its dependence on current sensor, it cannot support high switching frequency (200 kHz maximum). State observer is another approach to obtain current information, however, the dependence attribute by system architecture determines a complex architecture mapping to a large amount of hardware resources [Gensior 06]. From the perspective of modulation format, the con-

troller is versatile enough to implement valley, peak and average current-mode control just by adjustment of the sampling instant of I_L [Chen 03]. Although the three modulation architectures can optimize the control performance to some extent, the single control factor generated by the current-mode control can only lead to a symmetric or quasi-symmetric modulation pattern that restricts the dynamic performances.

1.1.4 Summary of Control-law

This section reviewed the state of the art control-laws in terms of linear, nonlinear and predictive dead-beat controls. The advantages and disadvantages of each reviewed control-law are illustrated. Some important control-laws reviewed in this section will be taken as building blocks or counterparts in Chapter 2 and 3 respectively.

1.2 Digital Pulse-width-modulator

Because of the inherent quantization effect, the closed-loop control architecture may operate with risk of LCO. It is introduced by the static and dynamic behaviors of the two quantizers [Peng 07]. Particularly an obvious case is that the quantization level of DPWM is larger than that of ADC [Peterchev 03b]. There is no adjacent DPWM level that maps into the ADC bin corresponding to the reference voltage. So an oscillation starts in the range of two adjacent levels.

The graphical interpretation of the limit-cycling phenomenon is shown in Fig. 1.7. The effective least significant bit (LSB) of ADC is q_{AD}. While the effective DPWM quantization voltage is expressed as q_{DPWM}. As shown in Fig. 1.7(a), if $q_{DPWM} > q_{AD}$, the output voltage V_{out} will generate the LCO. In steady-state, the controller always attempts to force the power converter output to reach the zero-error bin, however there is no corresponding DPWM level there, so a periodic oscillation behavior occurs in such a condition. In other words, there is no DPWM level that maps into the ADC bin, corresponding to the reference V_{ref}. That is the origin of LCO. On the contrary, if $q_{DPWM} < q_{AD}$, the converter is able to map to a DPWM level leading to a zero-error output voltage. In other words, it is a necessary condition that eliminates LCO. If we take the power stage into consideration, the control-to-output gain will put more strict constraint as [Peng 07]

$$G_0 \cdot q_{DPWM} < q_{AD} \tag{1.6}$$

where G_0 is the control-to-output gain of the converter under DC excitation. Assuming the control-law includes an integral term with a gain K_i, then we have $q_{DPWM} = K_i \cdot q_{AD}$, and (1.6) can be rewritten as

$$G_0 \cdot K_i < 1 \tag{1.7}$$

which offers the possibility to determine the range of feasible integral terms of a control-law. All the aforementioned steady-criteria must be satisfied so as to make further analysis in the dynamic condition.

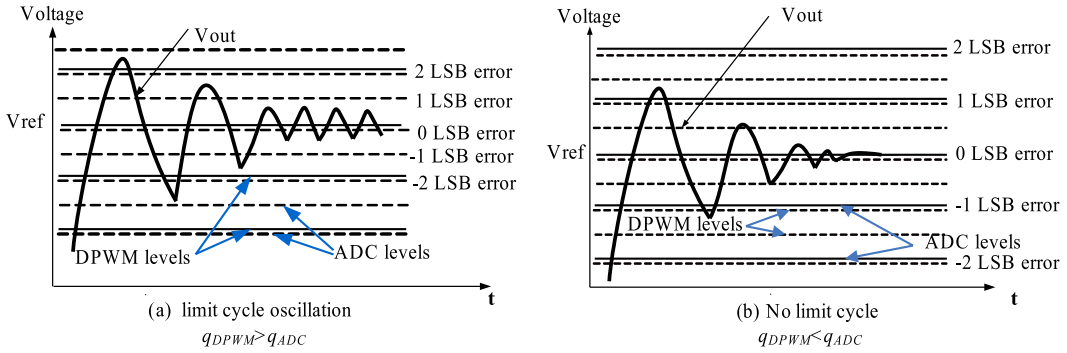


Figure 1.7: Behavior of the output tracking with (a) DPWM resolution lower than ADC resolution, (b) DPWM resolution higher than ADC resolution

Describing function is an effective approach to analyze the quantization effect of the quantizers. The approximate analysis method for the nonlinear system is used to interpret the dynamic behavior, and can exhibit the anti-LCO condition. [Peng 07] analyzed the anti-LCO condition under dynamic-state.

As a summary, the solution to solve LCO lays on two issues. Firstly, the resolution of DPWM must be relatively higher than that of ADC. A DPWM with high enough resolution is therefore mandatory requiring an achievable system clock frequency using the existing IC process. Furthermore, the closed-loop and dynamic impact must be taken into consideration including each building blocks of the digitally controlled power converter.

Relying on the excellent linearity, the advantage of counter-comparator DPWM is obvious in the time-domain. Nevertheless, for a n-bit DPWM devoted to a buck converter of which the switching frequency is f_s, an external clock must reach $2^n \cdot f_s$ theoretically. This is hardly achievable using the existing IC technology or at the risk of large power consumption as well as the necessity for an elaborate clock-tree. In order to solve these problems, several strategies are proposed. Three categories are given to better mark off each design motivation including delay-cell-based, hardware-assisted and dither-based methods. A review will be given in the next sections.

1.2.1 Delay-cell-based Methods

The delay-cell-based method generates time-slot that is smaller than the reference period taking advantage of the controllable delay from an inverter-based element. The CMOS inverter is a typical delay-cell that is a standard-cell in digital CMOS library. Other possible topologies, such as current-starved inverter, are easy to be instantiated and reused.

Dancy firstly introduces the delay-cell into the PWM [Dancy 97, Dancy 00]. The so-called delay-cell is commonly constructed by an improved current-starved delay-cell which is optimized to ensure that the negative edge of the outputs travel at the same speed as the positive edge. A series of delay-cells can make up a delay-line that is the main part to generate higher resolution. Fig. 1.8 shows the block diagram of the delay-line based DPWM.

A pulse from a reference clock starts a cycle, and sets the DPWM output high (after a delay designed to match the propagation delay through the multiplexer). The reference pulse propagates

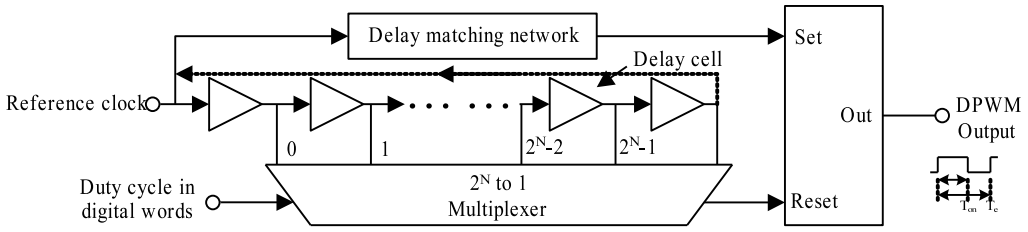


Figure 1.8: Delay-line DPWM [Dancy 97, Patella 03, Lukic 07]

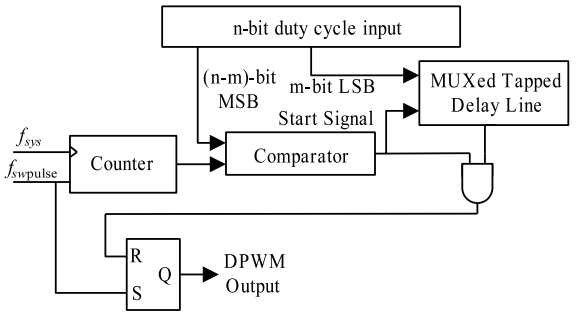


Figure 1.9: Block diagram of hybrid DPWM [Yousefzadeh 06a]

the delay-line, and when reaching the output selected by the multiplexer, it is used to set the DPWM output low. It therefore selects one of the time slots. Due to the PVT variations, the cell-delay t_d varies so that an open-loop delay-line cannot guarantee a well matching between the maximum delay and the switching frequency. Thus a closed-loop form (dotted part in Fig. 1.8) is adopted in order to improve the drift of the output duty-cycle to some extent.

In addition, several improvements such as the hybrid DPWM [Yousefzadeh 06a], the segment delay-line DPWM [Syed 04], the ring-oscillator DPWM [Peterchev 03b] are proposed with the purpose of a better linearity and better immunity to non-ideal process variations. Hybrid DPWM benefits from the cooperation of the counter-comparator and delay-line ADC, ensuring constant delays by the tapped delay-line regardless of external factors. The block diagram is shown in Fig. 1.9. Segmented delay-line DPWM separates the tapped delay-line into several stages in order to save the required amount of delay-cell. Ring-oscillator DPWM is based on symmetric structure. The full-differential delay-cell architecture can restrain the common-mode noise as well as support the multiphase DPWM since the different phases can be tapped out from symmetric positions across the ring. The delay-cell in the ring-oscillator is shown in Fig. 1.10.

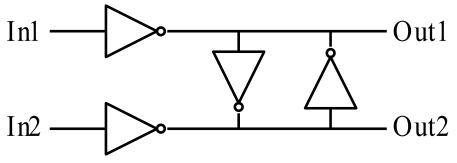


Figure 1.10: Ring oscillator delay-cell [Peterchev 03b]

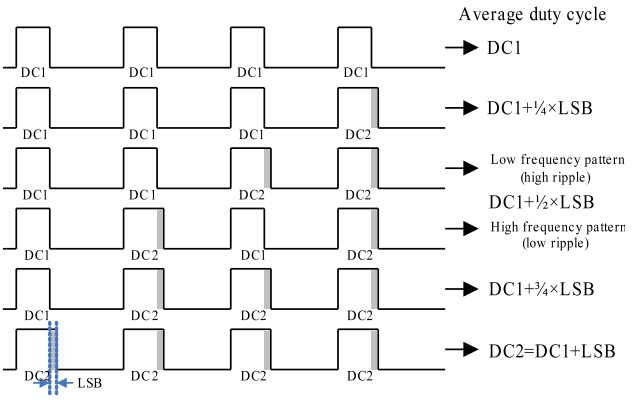


Figure 1.11: Dither pattern realizing 2-bit DPWM [Peterchev 03a]

The delay-cell-based methods absorb lower power consumption than the counter-comparator based ones. However they inherently suffer from PVT variations. Especially the DPWM with high resolution cannot assure an acceptable linearity as well as occupies large chip area (delay-cells and multiplexer). If a limited chip area and a harsh operating environment are the main concerns, such a solution is not a good candidate. The dither-based method reviewed in the next section can solve aforementioned drawbacks at the expense of dynamic performances.

1.2.2 Dither-based Methods

The dither-based methods involve a multi-cycle switch average algorithm generating an equivalent high-resolution DPWM. The averaging action is performed by an LC filter located in the power stage. Fig. 1.11 illustrates dithered patterns realizing 2-bit resolution. We can also observe that the minimum-ripple sequences (the fourth row) have an advantage over the rectangular-waveform (the third row) sequences with respect to the dither ripple size. LUT and Σ-Δ are two main approaches to generate the required dithers.

Several switching periods are required for an average of the dithered duty-cycles. So a common drawback of the dither-based DPWM is induced at the risk of the instability in terms of a slow tracking rate at specific input [Liu 09]. A potential closed-loop perturbation will also be introduced due to the slow convergence.

[Peterchev 03a] gives a LUT prototype to generate ripple-optimized dithers as shown in Fig. 1.12. A LUT stores 2^m dither sequences, each 2^m-b long, corresponding to the sub-bit levels implemented with m-bit dither. The dithered duty-cycle will be post-processed by a core DPWM in order to generate the output with anticipated resolution. A prediction of the dither ripple value with respect to the proposal to eliminate LCO is also given in [Peterchev 03a].

Another dither generation approach is to use a Σ-Δ modulator. The exact dither pattern during each averaging period is foreseeable and controllable. Meanwhile the mature noise-shaping analysis technique as well as the corresponding analysis tools are of a great benefit to anticipate the module behavior in time- and frequency-domain. We will discuss this issue in detail in Section 4.1.

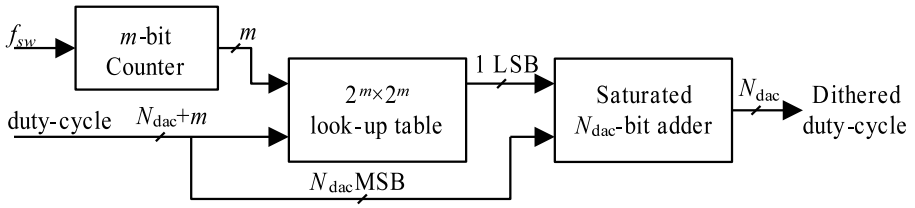


Figure 1.12: Block diagram of dithered duty-cycle generator [Peterchev 03a]

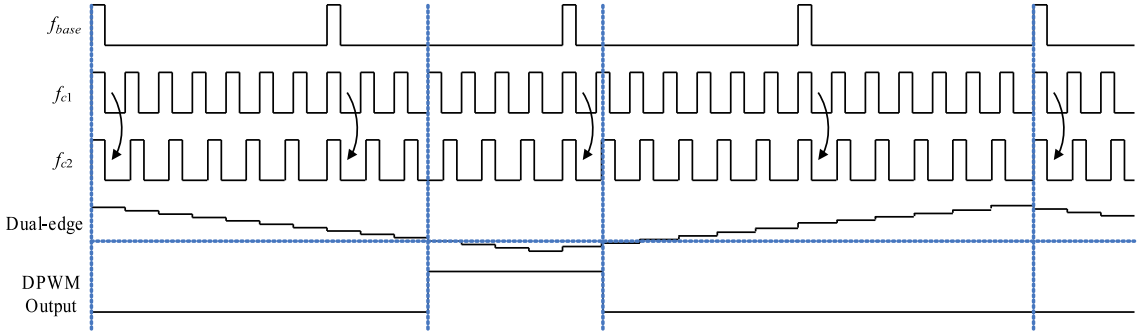


Figure 1.13: Timing sequence of dual-clock DPWM with division parameter M=7, N=6 [Qiu 07]

To sum up, dither-based methods can benefit the advance of digital IC much more. Compared to the delay-cell-based methods, such a solution can be programmed as a part embedded in the control-law with small additional hardware resources. This approach may cooperate with other methods, such as counter-comparator method, to provide a coarse quantization and to reduce the required system clock frequency.

With the aid of hardware, such as the digital-clock-manager in FPGA, alternatives are proven to be feasible as reviewed in the next section.

1.2.3 Hardware-assisted Methods

Based on possible Voltage-controlled oscillator (VCOs) in which delay-line is also an effective architecture, Fig. 1.13 shows an alternative also taking full use of PLL. [Qiu 07] gives the details. Two clocks $[f_{c1}; f_{c2}]$ generated by PLLs with similar frequencies are introduced with dual-edge modulation. The effective system clock frequency can be increased to

$$f_{sys} = \frac{f_{c1} f_{c2}}{f_{c1} - f_{c2}} \tag{1.8}$$

PLL is actually the critical component of which the characteristics determine the DPWM performances. In [Qiu 07], two PLLs with 100 and 101 MHz oscillation frequencies respectively are given to be compared. PLLs with such similar frequencies itself is a big challenge to a designer. Such specification requires an extra tuning or calibration modules.

As another feasible approach, phase-shifted DPWM is applicable to FPGA [Quintero 09] and is possibly implemented within ASIC. PLL/delay-locked loop (DLL) IPs can divide one cycle into

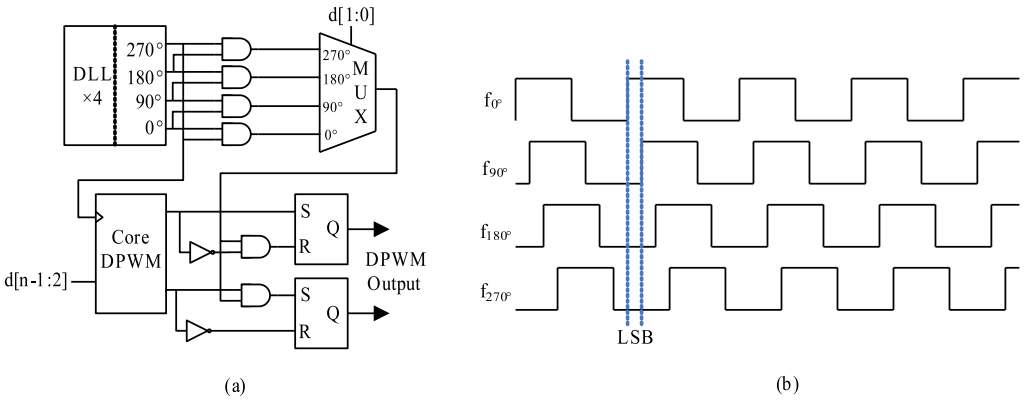


Figure 1.14: (a) Block diagram of the phase-shift DPWM, (b) its timing sequence [Huerta 08, Quintero 09]

Table 1.3: Summary of important DPWMs

Architecture	Complexity
Counter-comparator [Wei 96b]	Require fast clock
Delay-line [Dancy 98]	Require large silicon area
Segment delay-line [Syed 04]	Require MUX and thermometer coding
Hybrid delay-line [Patella 03]	Tradeoff between delay-line and counter-comparator
Ring-oscillator [Peterchev 03b]	Differential form of delay-line
Dual-edge dual-clock [Qiu 07]	Require two PLL with similar frequency
LUT-based dither [Peterchev 03b]	Require LUTs
Σ-Δ [Lukic 05, Lukic 07]	Require Σ-Δ modulator

N parts using the phase-shift signal. It effectively increases the resolution of DPWM by a factor of N. Fig. 1.14 presents an example of 90° phase-shift DPWM and the corresponding timing sequence. [Huerta 08] discusses the possible solution to avoid non-monotonic behavior when the two LSBs of the duty cycle are "11".

The aforementioned hardware-assisted methods are ready to use for circuit-level designers taking advantage of hardware resources such as FPGA and PLL. However, such a solution can not fully compatible with IC design.

1.2.4 Summary of DPWM

In the development of the digitally controlled DC-DC converter, DPWM plays a more and more important role across the feedback loop. Table. 1.3 and Table. 1.4 compare the aforementioned DPWMs where the Σ-Δ approaches will be detailed in Section 4.1. DPWMs with high resolution will continue to be a topic of interest on purpose of pursuing higher power efficiency. So an 1-1 DMASH Σ-Δ approach to achieve high resolution will be proposed in Section 4.2.

Table 1.4: Summary of important DPWMs (cont'd)

Architecture	Linearity	Power	Area	Process
Counter-comparator	Best	High	Unavailable	1.2μm
Delay-line	Poor	Moderate	$0.8mm \times 1.2mm$ (estimated)	0.6μm
Segment delay-line	Poor	Moderate	$0.0675mm^2$	0.5μm
Hybrid delay-line	Moderate	Moderate	$1mm^2$ (whole chip)	0.5μm
Ring-oscillator	Moderate	Moderate	$0.5mm \times 0.35mm$ (estimated)	0.25μm
Dual-edge dual-clock	Good	Unavailable	Unavailable	Unavailable
LUT-based dither	Good	Low	Unavailable	Unavailable
Σ-Δ	Moderate	Low	$0.057mm^2$	0.35μm

Table 1.5: Important products of digital dc-dc controller

Model	MFTR	Switching frequency	I^{2}C /SMBus^{TM}	PMbus^{TM}*	Control law	Accuracy
ZL2105	Zilker Lab	0.2-2MHz	$\surd$	$\surd$	Unavailable	$\pm$1%
LTC7510	Linear	0.15-2MHz	$\times$	$\surd$	PID	$\pm$2%
MAX8688	MAXIM	Up to 1MHz	$\surd$	$\surd$	Unavailable	$\pm$0.2%
UCD9240	TI	Up to 2MHz	$\surd$	$\surd$	hybrid	$\pm$0.1%

1.3 Available Products and Performances

Most of the portable electronic devices require a series of power converters that construct the system-level power converter network. Although digital control offers a better compatibility at the system-level, the use in industry has still encountered with reluctance from power electronic engineers. So there are not so many available products widely applied into industry nowadays. Table. 1.5 shows the most important products reflecting the top industrial design level.

**The Power Management Bus (PMBus) is an open standard power-management protocol with a fully defined command language that facilitates communication with power converters and other devices in a power system. The protocol is implemented over the industry-standard SMBus serial interface and enables programming, control and real-time monitoring of compliant power conversion products with details on http://pmbus.org/.*

1.4 Summary

The state of the art reviewed in this chapter opens two main directions to improve the digital control: performances and power losses. As two of the most important building blocks across the feedback loop, control-laws and DPWM will be investigated in depth in the following chapters. Some improved controllers with high dynamic performances will be proposed with a comparison to some of the reviewed controllers. In the mean time, the approach to reduce the idle-tone noise will be introduced to the Σ-Δ DPWM along with a dither module to further reduce this phenomenon. According to the author's knowledge, the power consumption of a digital controller has

not been regarded as a critical issue, although it will increase with the switching frequency that is distinct from the analog controller. This thesis will offer a plan to show the feasibility with respect to the power losses for digital controller according to the experimental results from dedicated digital controller ICs. Important peripherals, such as the on-chip clock generator, the parameter read-in module, will also be discussed to bridge the gap to the industry.

Chapter 2

Control-laws for the Buck and Boost Converters

Based on the survey on the state of the art papers in the previous chapter, this chapter will focus on the design of highly efficient control-laws devoted to the buck and boost converters. The performance of the digital controller is critical to the conversion efficiency. The adopted control-laws are anticipated to operate well in both the steady-state and dynamic-state as well as be of a relatively simple physical implementation. This chapter starts from a review of the existing control-laws including PID, RST, tri-mode and SM controls for the buck converter. The tri-mode controller proposed in [Guo 09a] will be improved in terms of compatibility with ASIC design and stable mode change. In order to enrich the target DC-DC converters, especially to some non-minimum phase systems exhibiting more serious nonlinearity (referring Appendix A.2.2), PID and SM controllers are implemented in a boost converter operating at high switching frequency. The existing theories for the buck converter must be reconsidered so as to better accommodate the boost converter. In the work of this thesis, we have implemented all these control-laws into ASIC. The integration issue and relevant tests will be discussed in Chapter 6.

2.1 Review of PID and RST Controls for the Buck Converter

As a background, this section will give a brief review of the earlier achievements in [Guo 09a]. Consisting of two off-line control-laws including PID and RST, a so-called tri-mode control has been improved which is adapted automatically among transient-state, steady-state and stand-by-state operations. The main concern is to achieve excellent performances in both the steady-state

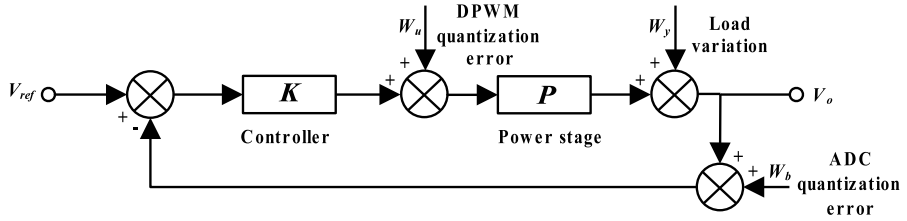


Figure 2.1: Block diagram of a typical SMPS with disturbances

and transient-state. According to the implementing results, the robust RST control achieves better performances than PID but at a cost of more multipliers probably resulting in a larger ASIC area. In order to better derive the control-laws, the relevant concepts must be clarified in advance.

For DC-DC switching converters, three types of disturbances are considered during modelling: the output disturbance W_y (e.g. load variation), measurement noise W_b (e.g. A/D converter noise) and control noise W_u (e.g. PWM noise). Fig. 2.1 represents the power stage of a SMPS (represented by P) and the controller (represented by K) with the three referred disturbances. So the output voltage of the target SMPS is given by

$$V_{out} = \Gamma \cdot V_{ref} + S_{yy} \cdot W_y + S_{yb} \cdot W_b + S_{yu} \cdot W_u \tag{2.1}$$

where Γ is the closed-loop transfer function. Given the definition of the open-loop transfer function $L_{yy} = K \cdot P$, Γ can be expressed as

$$\Gamma = \frac{K \cdot P}{1 + K \cdot P} = \frac{L_{yy}}{1 + L_{yy}} \tag{2.2}$$

S_{yy}, S_{yb} and S_{yu} are respectively the output-to-output, measure-to-output and control-to-output sensitivity function. They are given by

$$\begin{cases} S_{yy} = \dfrac{1}{1 + K \cdot P} = \dfrac{1}{1 + L_{yy}} \\ S_{yb} = \dfrac{-K \cdot P}{1 + K \cdot P} = \dfrac{-L_{yy}}{1 + L_{yy}} = -\Gamma \\ S_{yu} = \dfrac{P}{1 + K \cdot P} = \dfrac{P}{1 + L_{yy}} \end{cases} \tag{2.3}$$

S_{yy} at low frequency determines the steady-state properties of the target system. The bandwidth of S_{yb} defines the influence of measurement noise on the output voltage and the closed-loop bandwidth. The gain of S_{yu} verifies the rejection of control perturbations such as the PWM-related noises. The three sensitivity functions perform as graphical interpretation of the rejection to each disturbance and the stability of closed-loop system.

The discontinuous conduction mode (DCM) is avoided owing to an appropriate parameter selection for the buck converter. The CCM operation can facilitate the analyses for the proposed controllers. Since all operations are assured to operate under CCM, the transfer function of the buck converter in continuous-time (s-domain) is given by (details referring Appendix A)

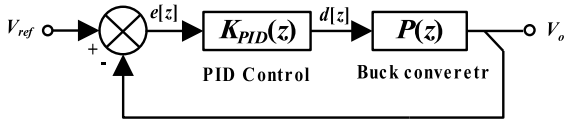


Figure 2.2: Block diagram of a PID-controlled buck converter

$$P(s) = \frac{\hat{V}_{out}(s)}{\hat{d}(s)} = \frac{(sr_C C + 1) V_{in}}{s^2 \left(1 + \frac{r_c}{R}\right) LC + s\left((r_C + r_L) C + \frac{r_L r_C C}{R} + \frac{L}{R}\right) + \frac{R_L}{R} + 1} \tag{2.4}$$

The corresponding discrete-time transfer function (z-domain) can be written as a second-order system [R.W.Ericksonand 00]

$$P(z) = \frac{b_1 z + b_2}{z^2 + a_1 z + a_2} \tag{2.5}$$

2.1.1 PID Control for the Buck Converter

PID control is one of the most frequently used control-laws in high frequency digitally controlled SMPS [Prodic 02, Patella 03, Yousefzadeh 06b, Takayama 06, Lukic 07]. The closed-loop buck converter with PID controller is illustrated in Fig. 2.2. $e[z]$ and $d[z]$ denotes the voltage error and PWM duty ratio respectively. In Fig. 2.2, the discrete-time PID control law can be modelled as

$$K_{PID}(z) = \frac{r_0 z^2 + r_1 z + r_2}{(z-1)(z+s_1)} = \frac{r_0\left(z^2 + \frac{r_1}{r_0} z + \frac{r_2}{r_0}\right)}{(z-1)(z+s_1)} \tag{2.6}$$

where r_0, r_1, r_2 and s_1 are the control parameters to be determined by the pole placement method. From Fig. 2.2 and (2.6), the discrete-time duty cycle is derived as

$$d(k) = r_0 e(k) + r_1 e(k-1) + r_2 e(k-2) - (s_1 - 1) d(k-1) + s_1 d(k-2) \tag{2.7}$$

where $d(k)$ is the discrete value of the PWM output, $e(k)$ is the discrete value of the error signal between the reference voltage V_{ref} and the regulated output V_o, $d(k-i)$ and $e(k-i)$ are respectively the output and the error values at the ith-cycles prior to the current cycle. Setting $\frac{r_1}{r_0} = a_1$ and $\frac{r_2}{r_0} = a_2$ to cancel the poles of $P(z)$ with the zeros of $K_{PID}(z)$, the closed-loop function in (2.2) can be rewritten as

$$\Gamma = \frac{r_0 b_1 z + r_0 b_2}{z^2 + (s_1 - 1 + r_0 b_1) z + (r_0 b_2 - s_1)} = \frac{r_0 b_1 z + r_0 b_2}{z^2 + p_1 z + p_2} \tag{2.8}$$

where p_1 and p_2 can be determined according to the desired closed-loop dynamics which corre-

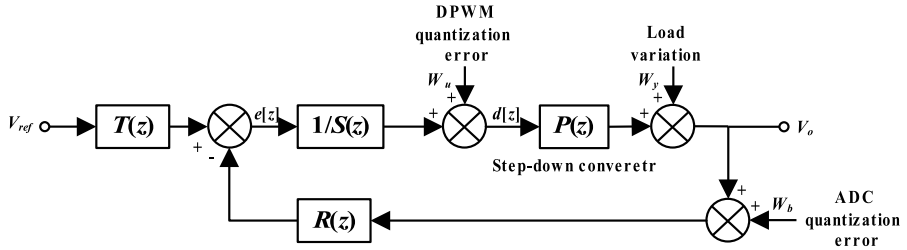


Figure 2.3: Block diagram of the RST controlled buck converter

spond to the second-order dynamics with a pulsation ω_{cr} and a damping ratio ζ_{cr}. Finally the parameters are determined as

$$\begin{cases} r_0 = (1 + p_1 + p_2)/(b_1 + b_2) \\ r_1 = a_1 r_0 \\ r_2 = a_2 r_0 \\ s_1 = r_0 b_2 - p_2 \end{cases} \tag{2.9}$$

Benefiting from Matlab simulations, control parameters can be obtained to achieve optimal control effect with respect to the graphical interaction of sensitivity functions.

2.1.2 Robust RST Control for the Buck Converter

Compared to the PID control, the robust RST allows to take into account different dynamics for the reference tracking and the rejection of disturbances [Lin-Shi 07, Guo 09a, Landau 94]. A RST controller is considered here in order to obtain a better output disturbance rejection while keeping a good robustness. The structure of a RST-controlled buck converter system is presented in Fig. 2.3. The design issue are detailed in [Lin-Shi 07].

If the discrete time SMPS model is described by the transfer function $P(z) = \dfrac{B(z)}{A(z)}$, where $B(z)$ and $A(z)$ are polynomials, the sensitivity functions can be expressed as

$$\begin{cases} S_{yy} = \dfrac{A(z)S(z)}{A(z)S(z) + B(z)R(z)} \\ S_{yb} = \dfrac{-B(z)R(z)}{A(z)S(z) + B(z)R(z)} \\ S_{yu} = \dfrac{B(z)S(z)}{A(z)S(z) + B(z)R(z)} \end{cases} \tag{2.10}$$

The same denominator in (2.10) can be used to determine the closed-loop poles. The knowledge of acceptable disturbances leads to design the RST control in terms of pole and zero assignments. Some fixed parts can be specified for the polynomials $S(z)$ and $R(z)$. For example, to ensure the output accuracy, a pole for $z = 1$ in $S(z)$ is necessary for static error elimination. The closed-loop poles are chosen either for filtering effects in certain frequency regions or for improving the robustness of the closed-loop system. For an output disturbance at pulsation ω_c (output filter corner frequency), the lower the gain of S_{yy}, the better the attenuation of the output distur-

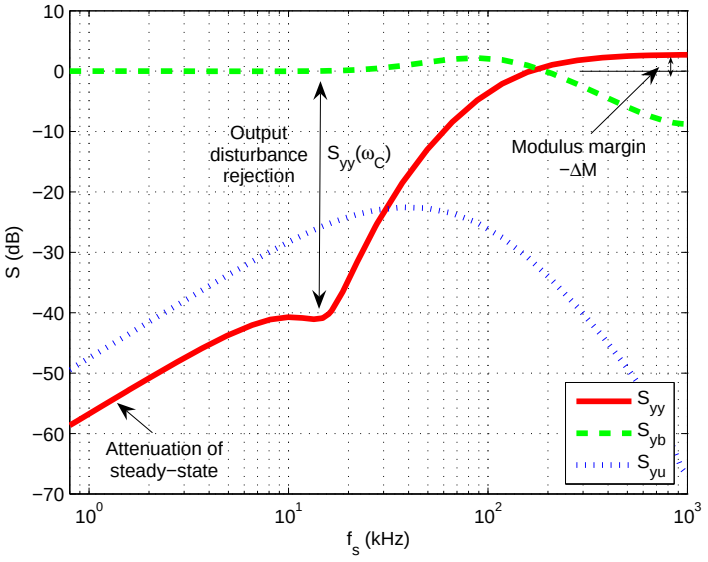


Figure 2.4: Sensitivity functions for a robust RST controller

bance. However it shows that the larger the attenuation of S_{yy} at ω_c, the larger the area of S_{yy} over zero value [Landau 90, Landau 96, Landau 98]. It can induce an increase in the maximum value of S_{yy}. As the maximum value of S_{yy} is inversely proportional to the modulus margin ΔM, a larger output noise rejection leads to a worse robustness. Fig. 2.4 demonstrates an example to describe aforementioned sensitivity functions for a robust RST controller. In this example, the gain of S_{yy} at ω_c (15kHz) is -41dB. To offer a trade-off between the robustness and a good rejection of disturbance, an off-line approach is proposed in [Lin-Shi 07] by using fuzzy logic and a genetic algorithm. This approach is summarized in Fig. 2.5. Detailed derivation procedure can be found in [Lin-Shi 07, Guo 09a].

Based on above discussion, a robust RST control can be written as

$$\begin{aligned} d(k) &= t_0 w(k) + t_1 w(k-1) + t_2 w(k-2) + t_3 w(k-3) \\ &\quad - r_0 y(k) - r_1 y(k-1) - r_2 y(k-2) - s_1 d(k-1) - s_2 d(k-2) \end{aligned} \tag{2.11}$$

where $d(k)$, $w(k)$ and $y(k)$ are respectively the discrete value of the PWM output, the reference voltage V_{ref} and the regulated output V_o, $d(k-i)$, $w(k-i)$ and $y(k-i)$ are the corresponding values at the ith-cycles prior to the current cycle, t_0, t_1, t_2, t_3, r_0, r_1, r_2, s_1 and s_2 are optimized control parameters.

2.1.3 Comparative Study of PID and RST Control-laws

A closed-loop simulation based on the buck converter written in S-function is performed to compare the performances of the two control-laws. As a necessary step before FPGA/ASIC implementation, the simulation is set to the fixed-point mode to anticipate the behavior in the further

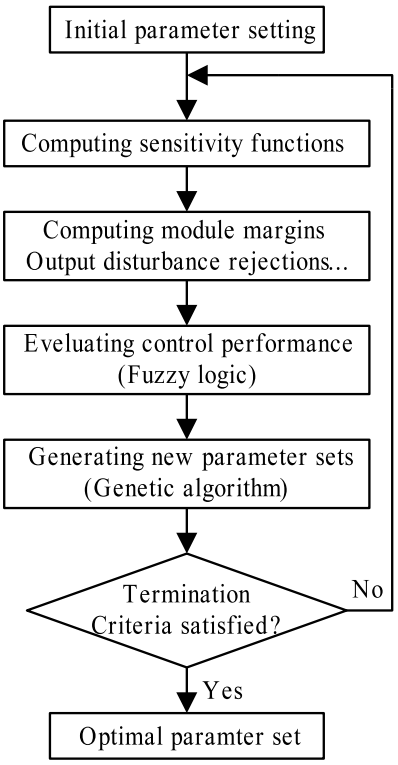


Figure 2.5: Offline approach to determine the control parameters

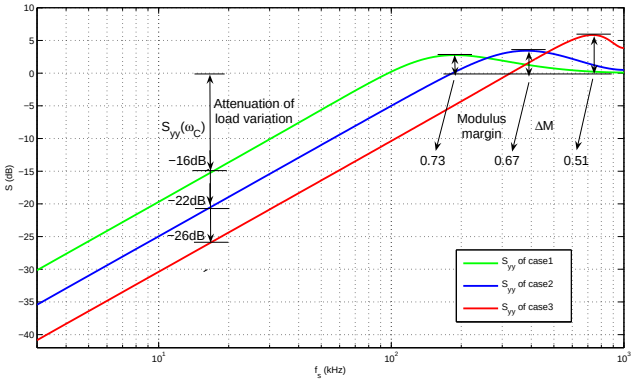
FPGA and ASIC. All the circuit parameters are of the same values as the ones on the test board. The default switching frequency f_s=2MHz, filter inductor L=4.7μH, filter capacitor C=22μF and the nominal load R_L=5Ω.

There is a trade-off between the robustness and the output noise (load variation) rejection property. For PID controller, a simulation is performed to obtain a better PID regarding the two factors. As shown in Fig. 2.6(a), the gain of S_{yy} at 15kHz corner frequency is -16dB, -22dB and -26dB respectively. The simulation results in time-domain also satisfy the analysis as shown in Fig. 2.6(b). However, the better the attenuation of load variation, the worse the modulus margin. That is to say, a better load variation rejection leads to a worse robustness as shown in Fig. 2.6(a). In this design, the case 2 is applied to the tri-mode controller..

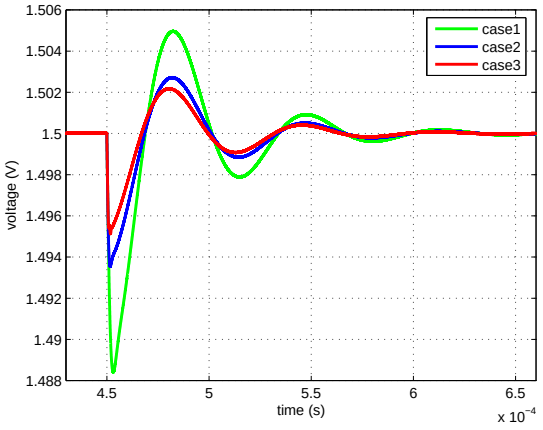
In order to quantify the control dynamics, robustness and output noise (load variation) rejection properties, the output-to-output sensitivity function S_{yy} is also presented in frequency-domain as shown in Fig. 2.7(a) for the PID and RST controls respectively. The parameters of PID and RST are both adjusted to obtain best dynamic rejections.

As aforementioned in Section 2.1.2, the gain of S_{yy} at 15kHz corner frequency is -43dB for RST control against -22dB for the PID control as shown in Fig. 2.7(a), whereas their robustness are similar ($\Delta M_{RST} = 0.73,\ \Delta M_{PID} = 0.67$).

Fig. 2.7(b) shows the simulation results of PID and RST control performances under load change from 0.3A to 0.45A to ensure CCM operation. The load transient response of RST control is superior to the PID control because it offers shorter settling time and produces smaller negative

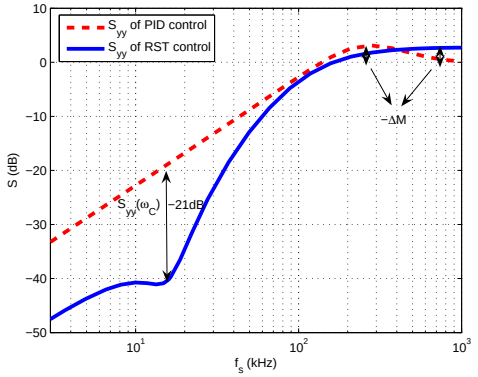


(a)

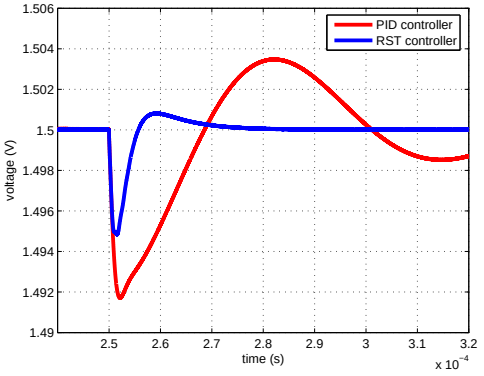


(b)

Figure 2.6: (a)S_{yy} sensitivity function for three PID controllers with different parameters, (b) simulation of three PID controllers with different parameters under load change from 0.3A to 0.45A



(a)



(b)

Figure 2.7: (a)S_{yy} sensitivity function for PID and RST controls, (b) simulation of PID and RST controls under load change from 0.3A to 0.45A

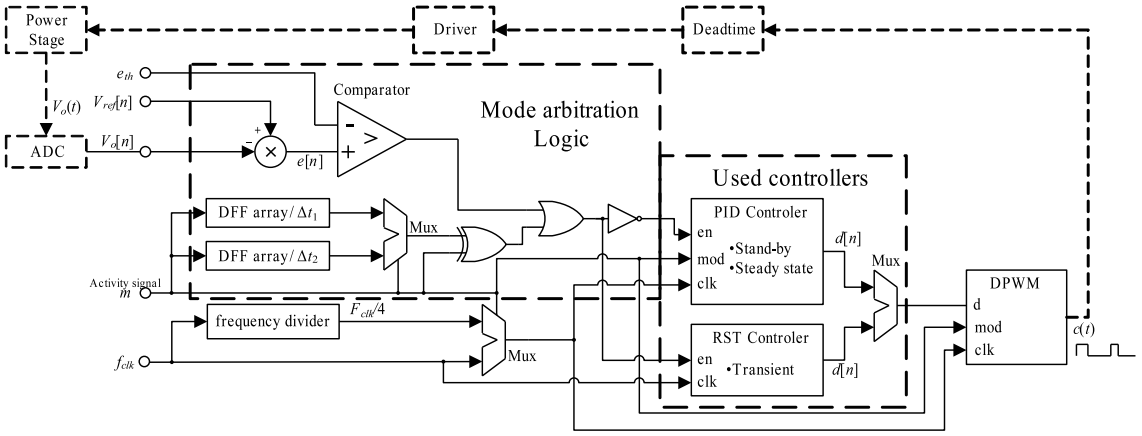


Figure 2.8: Improved tri-mode controller dedicated to ASIC

overshoot voltage.

2.2 Improved Power-aware Tri-mode Control

2.2.1 Review of Tri-mode Control for the Buck Converter

Aforementioned comparative study between PID and RST control-laws shows that for similar robustness with respect to the modeling uncertainties, the RST control exhibits a better dynamic behavior against the load variation than the PID control. However, the RST control requires a more complex implementation with respect to the extra combinational cells across the datapath according to (2.7) and (2.11). In fact, when the buck converter operates in steady-state, i.e. the external load is stable, the primary task of a control-law is to maintain the output voltage stable within an acceptable error range. Thus a simple control-law such as PID is preferable in steady-state. Moreover using the PID control during steady-state can not only satisfy the performance specification but also relax the tight requirement of algorithm computation so as to reduce the power consumption to some extent.

Many portable devices spend much time in the idle-state, i.e. in stand-by mode. The quarter PID control is therefore proposed. It has the same structure as the PID controller applied in normal operation but clocked at a quarter the switching frequency. That is to say the PID control updates its computation every four periods. Quarter PID control will help to further reduce the power consumption with respect to digital control.

The tri-mode control is then proposed in [Guo 09a] as shown in Fig. 2.8. It consists of a *mode arbitration logic* which switches among the three modes: robust RST control for the transient mode, PID control for the steady-state mode and quarter PID control for the stand-by mode. The operation of the tri-mode control is designed as shown in Fig. 2.9, and the mode changes procedure are detailed in Fig. 2.10.

The tri-mode control depends on an external activity signal m normally obtained by a sensor to select an appropriate mode. The digital functions inside any low-power systems are able to issue such a signal. For instance in the operation of a mobile phone, the activity signal is set to

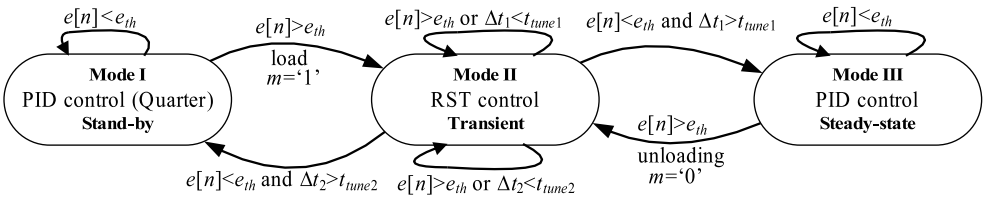


Figure 2.9: State-switch diagram of mode arbitration block

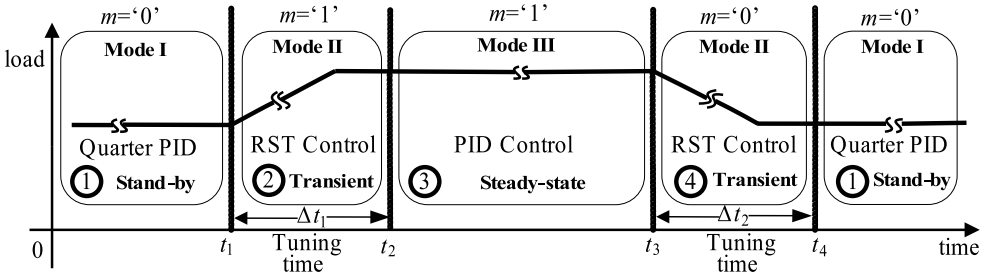


Figure 2.10: Mode change procedure of tri-mode controller

$m = 0$ when it is in the stand-by mode; and $m = 1$ when it is in normal operation. The tuning time Δt_1 and Δt_2 of RST control for the transient tuning can be adjusted to satisfy the practical application. Such two tuning times can be implemented by two ladders of D-flip-flops arbitrated by the activity signal m. For example the constant tuning time t_{tune1} is set to Δt_1 and t_{tune2} to Δt_2 here. The voltage error $e[n]$ obtained from the reference voltage $V_{ref}\,[n]$ and the regulated output $V_o\,[n]$ is normalized in the discrete-time format and the maximum tolerant voltage error is set as the threshold e_{th}. It is a user-defined voltage such as a unit value of 15mV for example. As shown in Fig. 2.8, e_{th} is compared to the actual error signal $e\,[n]$. The logic-glue assures a correct functions and timing sequence to enable the three controls. A frequency divider is used to provide a quart system clock to PID control in stand-by mode. Detailed operation of the tri-mode control is described as follows

1. After the initialization of a buck converter, it is assumed that the controller is in stand-by mode, using the quarter PID to regulate the output voltage. It will be kept in this state until the output variation is larger than the error threshold, i.e., $e[n] > e_{th}$ (normalization), or an activity signal $m = 1$ is detected. Then the controller switches to procedure 2);
2. The controller will switch to transient mode using RST control law to regulate the output voltage $V_o\,(t)$, and this control mode will be maintained long enough ($\Delta t_1 > t_{tune1}$) to achieve $e[n] < e_{th}$, which means the buck converter enters a steady-state mode;
3. In steady-state mode, the controller selects the PID control to regulate the output voltage. This mode will be maintained until the output variation is larger than the error threshold, i.e., $e[n] > e_{th}$, or an activity signal $m = 0$ is detected;
4. The RST control will be selected again for the regulation of unloading in transient mode. This control mode will be held long enough ($\Delta t_2 > t_{tune2}$) until $e[n] < e_{th}$, which means that unloading has finished and the SMPS arrives in a steady-state mode again;

5. After transient, the controller stays in an unloaded situation and will be set in stand-by mode, which returns to procedure 1) again waiting for a next operation cycle.

2.2.2 An Improved Version of Tri-mode Control Dedicated to ASIC

Based on the tri-mode controller, this section introduces an improved version to accommodate system-level low-power requirements by a power-aware technique. The *mode arbitration logic* is also optimized to satisfy the digital IC design requirements.

According to (2.7) and (2.11), the control output $d(k)$ in the current period is derived by the state variables in the previous cycles. For example, the PID controller requires the state variables at least two cycles prior to the current period. If there is no operation overlap in time domain, the controller is bound to generate a large offset in the first periods after a mode change. In order to overcome this difficulty, a so-called pre-post-operation in transient mode is proposed during mode change.

From Fig. 2.10, the robust RST control is next to any adjacent control. For example, when the mode changes from stand-by mode to transient mode, the operation of RST control can be manually extended to the interval of quarter PID. This extension should be long enough to set up a stable closed-loop response of RST control. So it can be regarded as pre-operation. On the contrary, when the mode changes from transient mode to steady-state mode, the RST control extends to the interval of PID control so as to perform the post-operation. In the second situation, several periods during mode change are sacrificed to avoid potential instability. Two overlaps are therefore suggested only requiring small modifications to the hardware configuration as

- Extend the tuning time Δt_1 and Δt_2 to ΔT_1 and ΔT_2 respectively according to the experimental results that satisfy the stability criterion during mode change;
- Permit that two controls operate simultaneously;
- Add another arbitrary module to select the Mux output in *used controller block* (in Fig. 2.8) following the timing sequence discussed above.

The improved power-aware tri-mode controller is realized in a digital IC. Implementation details are discussed in Chapter 6 along with experimental results. The tri-mode controller offers more flexible selection with three modes to save power consumption. Due to the tri-mode controller where the quarter PID updates the whole control-law computation in stand-by mode at a switching frequency of $\frac{f_s}{4}$, evidently it can reduce the power consumption compared to the stand-alone PID or RST controllers. Power consumption associated issues will be discussed in Chapter 7.

2.3 Review of SM Control

2.3.1 Design Methodology of a SM Control for Power Converters

As one of the most important nonlinear controls, SM control initially employs a specific sliding surface as a reference in order to force the target state variables towards the given equilibrium [Utkin 09]. So an ideal SM control requires an absolute satisfaction of several conditions including

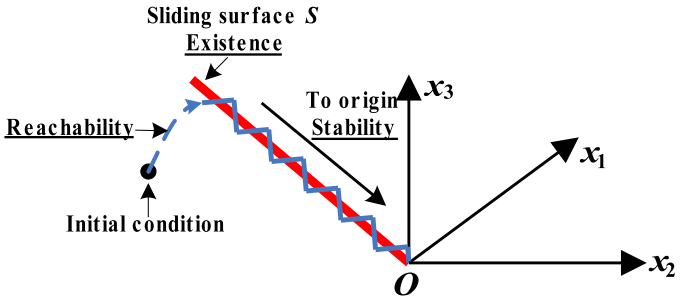


Figure 2.11: Graphical representation of the convergence process of SM control satisfying manipulation conditions

the reachability, the existence and the stability condition. It has been proven to be an effective method within a wide range of applications. The most obvious advantages of SM control are the predicable control trajectory and the inherent rapid response to almost all types of perturbation. However, the original intention of SM control requires infinite switching frequency to ensure the state on sliding manifold. Conventional hysteresis modulation (HM) based method makes SM control suitable for the converter's control purpose with finite switching frequency. Whereas HM-based SM control generally suffers from significant switching frequency variation when the input voltage and the output load are varied [Mattavelli 93, Tan 05a]. As for the fixed-frequency SM control, PWM-based SM control was proposed as a feasible method that successfully solved the problem [Tan 05b, Tan 08a].

PWM-based SM control is generally designed to determine the switch position u as

$$u = \begin{cases} 0, & \text{if} \quad S(e) < 0 \\ 1, & \text{if} \quad S(e) > 0 \end{cases} \tag{2.12}$$

where $S(e)$ is a smooth scalar function called sliding surface taken usually as a linear function of the state variables. For example, a 3-dimensional sliding surface by a factor of control variable e is described as

$$S(e) = J^T e = K_1 e_1 + K_2 e_2 + K_3 e_3 \tag{2.13}$$

where appropriate sliding coefficients $J^T = \begin{bmatrix} K_1 & K_2 & K_3 \end{bmatrix}$ will assure necessary conditions of SM control, and can be adjusted to improve the control performances. A graphical representation gives the sliding trajectory in Fig. 2.11 representing the controller behavior during SM control process.

Provided that the sliding surface $S(e)$ describes the behavior as shown in Fig. 2.11, the trajectory requires to be driven to get rid of the initial value and to reach the vicinity of the sliding surface. It is the so-called reachability condition. When the trajectory falls into the vicinity of the sliding surface, existence condition is usually guaranteed so as to avoid that the trajectory jump away from $S(e)$. Another criterion, the stability condition, then ensures that the state trajectory will always reach a stable equilibrium point O. In other words, after the aforementioned three

steps, the SM control will eventually achieve the steady-state operation. The trajectory will at the same time reach the stable equilibrium point O. Hence, the equivalent trajectory will evolve on the surface.

$$S\left(e\right)=0 \tag{2.14}$$

Rearranging the state-space description of control variable e into the standard form, the differentiation format can be expressed as $\dot{e}=Oe+Pu+Q$ where O, P and Q are control variable matrix that depend on converter type, and u stands for the switching position. The concept of equivalent control is introduced from the assumption that the motion of the trajectory is mainly dominated by the low-frequency component, while the high-frequency component will be filtered out by the power stage [Tan 08a]. Therefore, the equivalent control signal u_{eq} can be derived by the invariance condition $\dot{S}\left(e\right)=0$ [Utkin 09] as

$$\dot{S}\left(e\right)=J^{T}\dot{e}=J^{T}Oe+J^{T}Pu_{eq}+J^{T}Q=0 \tag{2.15}$$

So the equivalent control signal u_{eq} can be obtained as

$$u_{eq}=-\left[J^{T}P\right]^{-1}J^{T}[Oe+Q] \tag{2.16}$$

u_{eq} is also an effective variable that can be mapped to the duty cycle of the PWM-based SM control.

It is beneficial to re-discuss the existence condition in order to determine the precise sliding motion range. The reachability condition is obliged to satisfy

$$\lim_{S(e)\to 0} S\left(e\right)\cdot\dot{S}\left(e\right)<0 \tag{2.17}$$

It can be rewritten into the following two conditions

$$\begin{cases} \dot{S}(e)_{S(e)\to 0^{+}}=J^{T}Oe+J^{T}Pu_{S(e)\to 0^{+}}+J^{T}Q<0 \\ \dot{S}(e)_{S(e)\to 0^{-}}=J^{T}Oe+J^{T}Pu_{S(e)\to 0^{-}}+J^{T}Q>0 \end{cases} \tag{2.18}$$

According to (2.18), the range of sliding coefficients can be obtained as a reference to determine the optimal values. However, (2.18) only offers the range of the valid coefficients. [Tan 05b] proposes a general method for the second-order converters depending on the bandwidth of the desired frequency response in conjunction with the existence condition for PWM-based SM control.

2.3.2 SM Control for the Buck Converter

Fig. 2.12 shows the block diagram of SM controlled buck converter. Based on the discussion in the previous section, the sliding surface $S(e)$ can be chosen by forcing the output voltage V_{out} to approach its reference value V_{ref} within acceptable margins under load change, as

$$S(e)=K_{1}(V_{ref}-V_{out})+K_{2}\frac{d}{dt}(V_{ref}-V_{out})+K_{3}\int(V_{ref}-V_{out})dt \tag{2.19}$$

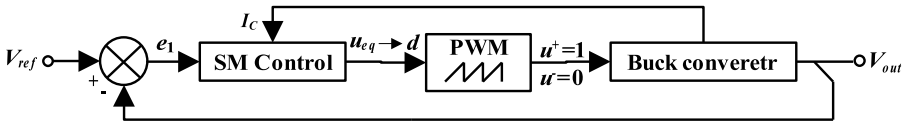


Figure 2.12: Block diagram of SM controlled buck converter

where K_1,K_2,K_3 are sliding coefficients to ensure the system trajectory within the sliding motion ranges and maintain the stability of SM control, i.e. $J^T = \begin{bmatrix} K_1 & K_2 & K_3 \end{bmatrix}$. The control variables can be therefore rewritten as

$$e = \begin{bmatrix} e_1 \\ e_2 \\ e_3 \end{bmatrix} = \begin{bmatrix} V_{ref} - V_{out} \\ \dfrac{d\left(V_{ref} - V_{out}\right)}{dt} \\ \int \left(V_{ref} - V_{out}\right) dt \end{bmatrix} \tag{2.20}$$

Extracting the time differentiation of (2.20) leads to

$$\begin{bmatrix} \dot{e}_1 \\ \dot{e}_2 \\ \dot{e}_3 \end{bmatrix} = O \begin{bmatrix} e_1 \\ e_2 \\ e_3 \end{bmatrix} + Pu + Q \tag{2.21}$$

where

$$O = \begin{bmatrix} 0 & 1 & 0 \\ 0 & -\dfrac{1}{RC} & 0 \\ 1 & 0 & 0 \end{bmatrix}, P = \begin{bmatrix} 0 \\ -\dfrac{V_{ref}}{LC} \\ 0 \end{bmatrix}, Q = \begin{bmatrix} 0 \\ \dfrac{V_{out}}{LC} \\ 0 \end{bmatrix} \tag{2.22}$$

For each interval of commutation $(kT_e, (k+1)T_e)$ where T_e is one switching period, we can write the control u as

$$u = \begin{cases} u^+ = 1, & kT_e \leq (k+d)\, T_e \\ u^- = 0, & (k+d)\, T_e \leq (k+1)\, T_e \end{cases} \tag{2.23}$$

At high switching frequency replacing u by a smooth function known as the equivalent control signal u_{eq} which is equivalent to duty-cycle control for the buck converter, the equivalent control is determined using the invariance conditions by setting $S = 0$ and $\dot{S} = 0$ as

$$\begin{aligned} u_{eq} = d &= -\left[J^T P\right]^{-1} J^T \left[Oe + Q\right] \\ &= \frac{1}{V_{in}} \left[V_{ref} + LC \left(\frac{K_1}{K_2} - \frac{1}{RC} \right) e_2 + LC \left(\frac{K_3}{K_2} - \frac{1}{RC} \right) e_1 \right] \end{aligned} \tag{2.24}$$

This control requires the knowledge of V_{out} which is measured to arrive at e_2. A simple numerical derivation is considered to determine e_2, so (2.24) can be rewritten as

$$d = \frac{1}{V_{in}}\left[V_{ref} - LC(\frac{K_1}{K_2} - \frac{1}{RC})\frac{V_{out}(n) - V_{out}(n-1)}{T_s}\right] + \frac{1}{V_{in}}\left[LC(\frac{K_3}{K_2} - \frac{1}{LC})(V_{ref} - V_{out})\right] \tag{2.25}$$

which indicates that SM control has a similar computing complexity as a PID controller and can fit FPGA and ASIC implementations.

Next, a brief discussion about motion range and stability of SM control is introduced. The first step is to use the Lyapunov's second method [Slotine JJ 91] to determine the sliding motion range. The existence condition of S must be verified by

$$\lim_{S(e)\to 0} S(e) \cdot \dot{S}(e) < 0 \tag{2.26}$$

Two possibilities are analyzed as follows

$$\begin{cases} \dot{S}(e)\Big|_{S(e)\to 0^+, u=u^+=1} = J^T O e + J^T P u + J^T Q < 0 \\ \qquad\qquad = \left(K_1 - \dfrac{K_2}{RC}\right) e_2 + \left(K_3 - \dfrac{K_2}{LC}\right) e_1 + \dfrac{K_2}{LC}(V_{ref} - V_{in}) < 0 \\ \dot{S}(e)\Big|_{S(e)\to 0^-, u=u^-=0} = J^T O e + J^T P u + J^T Q > 0 \\ \qquad\qquad = \left(K_1 - \dfrac{K_2}{RC}\right) e_2 + \left(K_3 - \dfrac{K_2}{LC}\right) e_1 + \dfrac{K_2}{LC} V_{ref} > 0 \end{cases} \tag{2.27}$$

If K_2 is positive, as a consequence, the motion range of S can be represented into the (e_1, e_2) phase plane as

$$\begin{cases} l_1(e) = (\dfrac{K_1}{K_2} - \dfrac{1}{RC})e_2 + (\dfrac{K_3}{K_2} - \dfrac{1}{LC})e_1 + \dfrac{V_{ref} - V_{in}}{LC} < 0 \\ l_2(e) = (\dfrac{K_1}{K_2} - \dfrac{1}{RC})e_2 + (\dfrac{K_3}{K_2} - \dfrac{1}{LC})e_1 + \dfrac{V_{ref}}{LC} > 0 \end{cases} \tag{2.28}$$

Thus two lines $l_1(e) = 0$ and $l_2(e) = 0$ determine the two boundaries of sliding surface existence range respectively. As shown in Fig. 2.13, (2.28) provides two lines with the same slope in the (e_1, e_2) plane. By setting $l_1(e) = 0$ and $l_2(e) = 0$, four points A, B, C and D shown in Fig. 2.13 can be derived as

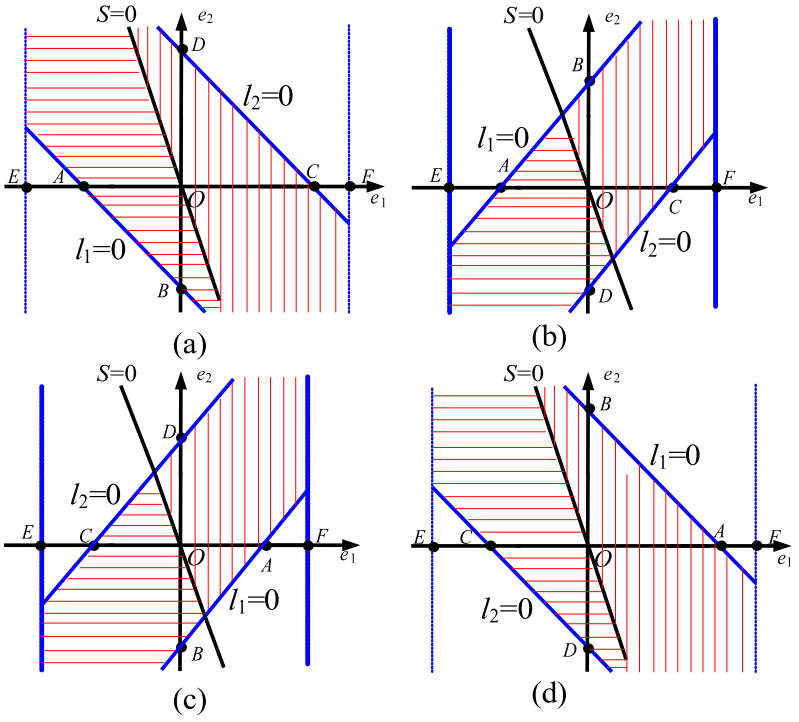


Figure 2.13: Existence range of SM control mapped on (e_1,e_2) phase plane

$$\begin{cases} A & \left(\dfrac{V_{in}-V_{ref}}{LC\left(\dfrac{K_3}{K_2}-\dfrac{1}{LC}\right)}, 0 \right) \\ B & \left(0, \dfrac{V_{in}-V_{ref}}{LC\left(\dfrac{K_1}{K_2}-\dfrac{1}{RC}\right)} \right) \\ C & \left(\dfrac{-V_{ref}}{LC\left(\dfrac{K_3}{K_2}-\dfrac{1}{LC}\right)}, 0 \right) \\ D & \left(0, \dfrac{-V_{ref}}{LC\left(\dfrac{K_1}{K_2}-\dfrac{1}{RC}\right)} \right) \end{cases} \tag{2.29}$$

The axis e_1 falls in the range as $e_1 \in ((V_{ref}-V_{in}), V_{ref})$ in which the two ends are expressed as point E and point F respectively. For different values of the parameters $\frac{K_1}{K_2}$ and $\frac{K_3}{K_2}$, the slope of the two parallel lines is changing. Therefore the existence condition falls in positive slope region and negative slope range for each line. (2.28) shows four possibilities for the motion range in Fig. 2.13 which can be catalogued as follows

$$\begin{cases} \frac{K_1}{K_2} < \frac{1}{RC}, \ \frac{K_3}{K_2} < \frac{1}{LC} & \text{(a)} \\ \frac{K_1}{K_2} > \frac{1}{RC}, \ \frac{K_3}{K_2} < \frac{1}{LC} & \text{(b)} \\ \frac{K_1}{K_2} < \frac{1}{RC}, \ \frac{K_3}{K_2} > \frac{1}{LC} & \text{(c)} \\ \frac{K_1}{K_2} > \frac{1}{RC}, \ \frac{K_3}{K_2} > \frac{1}{LC} & \text{(d)} \end{cases} \tag{2.30}$$

where (a) and (d) belong to the negative slope region, (b) and (c) belong to the positive one.

Regarding stability issues of SM control, Laplace transform can be used to (2.19) to get the equation about S

$$(s^2 + \frac{K_1}{K_2}s + \frac{K_3}{K_2})e_1 = 0 \tag{2.31}$$

Using the Routh's stability criterion, the stability conditions can be satisfied if all the parameters K_1, K_2 and K_3 have the same sign. The convergence dynamics can be chosen as a standard second-order system form as

$$s^2 + 2\xi\omega_n s + {\omega_n}^2 = 0 \tag{2.32}$$

where the pulsation ω_n and damping ratio ξ are respectively

$$\omega_n = \sqrt{K_3/K_2}, \quad \xi = K_1/2\sqrt{K_3K_2} \tag{2.33}$$

The SM control parameters are extracted from the stability conditions and the desired behavior. After simulation, the damping ratio ζ is set to 0.9 and the pulsation $f_n = \frac{\omega_n}{2\pi}$ is set to one-fifteenth of the switching frequency to achieve better dynamic performances according to the simulation results. So the following sliding parameters are obtained as

$$\frac{K_1}{K_2} = 4\pi\frac{f_s}{15} \quad \text{and} \quad \frac{K_3}{K_2} = 4\pi^2\left(\frac{f_s}{15}\right)^2 \tag{2.34}$$

where f_s is the switching frequency. When the buck converter operates at 4MHz, the coefficients are $\frac{K_1}{K_2} < \frac{1}{RC}$ and $\frac{K_3}{K_2} > \frac{1}{LC}$. Thus the existence region for the proposed SM control corresponds to the case in Fig. 2.13(c).

To verify the performance of SM controller, a simulation is performed using the same buck converter testbench described in Section 2.1.3. Fig. 2.14 shows the converter output voltage and inductor current responses during load change from 0.3A to 0.45A. A short settling time (27μs) verifies a good dynamic performance. SM control in this simulation supports 4MHz switching frequency. However, an obvious steady-state error can be found in Fig. 2.14(a). This is an inherent drawback of this type of SM control based on the equivalent control approach. [Tan 08b] proposed a solution via double integral sliding surface, however, this approach generally requires the exact value of inductor current that requires a current sensor, and a more complex implementation architecture.

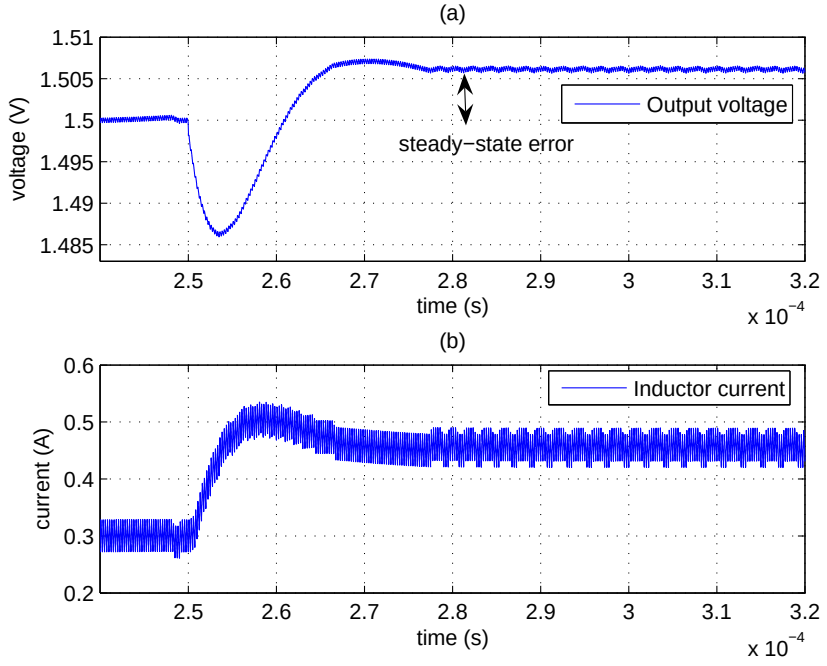


Figure 2.14: Dynamic response of the SM control under load change from 0.3A to 0.45A (a) output voltage, (b) inductor current

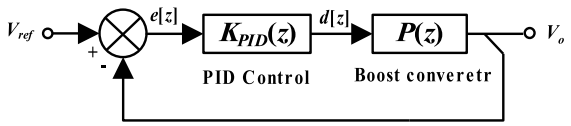


Figure 2.15: Block diagram of a PID controlled boost converter

2.4 Design and Test of Control-laws for the Boost Converter

In order to enrich the target DC-DC converters, especially to some non-minimum phase systems exhibiting more serious nonlinearity, this section applies the linear PID and nonlinear SM control-laws to the boost converter. The existing theories in previous sections must be reconsidered so as to better accommodate the boost converter. The models describing the behaviors of the boost converter are given in Appendix A.2.2.

2.4.1 PID Control for the Boost Converter

Appendix A.2.2 discusses the state-space model of a boost converter as well as the derived transfer function $P(s) = \dfrac{\hat{V}_{out}(s)}{\hat{d}(s)}$, obtained by the state-space averaging method and the small signal method around an operation condition. The corresponding discrete-time model can be seen as of the same form as in (2.4). The closed-loop boost converter with PID control is shown in Fig. 2.15. The common design methodology has already been discussed in Section 2.1.1 and can be directly transplanted to the boost converter.

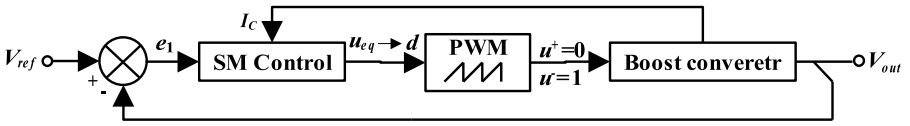


Figure 2.16: Block diagram of SM controlled boost converter

2.4.2 SM Control for the Boost Converter

The design methodology of SM control has been discussed in Section 2.3.1. Fig. 2.16 shows the block diagram of SM controlled boost converter. In order to force the output voltage, V_{out}, to approach its reference value, V_{ref}, within acceptable margins under load change, the sliding surface $S(e)$ is chosen as

$$S(e) = K_1(V_{ref} - V_{out}) + K_2\frac{d}{dt}(V_{ref} - V_{out}) + K_3\int (V_{ref} - V_{out})dt \tag{2.35}$$

where K_1,K_2,K_3 are sliding coefficients to ensure the system trajectory within the sliding motion ranges and maintain acceptable stability, i.e. $J^T = \begin{bmatrix} K_1 & K_2 & K_3 \end{bmatrix}$. The control variables can be therefore rewritten as

$$e = \begin{bmatrix} e_1 \\ e_2 \\ e_3 \end{bmatrix} = \begin{bmatrix} V_{ref} - V_{out} \\ \dfrac{d\,(V_{ref} - V_{out})}{dt} \\ \int (V_{ref} - V_{out})\,dt \end{bmatrix} \tag{2.36}$$

Extracting the time differentiation of (2.36) leads to

$$\begin{bmatrix} \dot{e}_1 \\ \dot{e}_2 \\ \dot{e}_3 \end{bmatrix} = O\begin{bmatrix} e_1 \\ e_2 \\ e_3 \end{bmatrix} + P\bar{u} \tag{2.37}$$

where

$$O = \begin{bmatrix} 0 & 1 & 0 \\ 0 & -\dfrac{1}{RC} & 0 \\ 1 & 0 & 0 \end{bmatrix}, P = \begin{bmatrix} 0 \\ \dfrac{V_{out}}{LC} - \dfrac{V_{in}}{LC} \\ 0 \end{bmatrix}, Q = 0 \tag{2.38}$$

For each interval of commutation $(kT_e, (k+1)T_e)$ where T_e is one switching period, we can write the control $\bar{u}$ as

$$\bar{u} = 1 - u = \begin{cases} u^+ = 0, & kT_e \le (k+d)\,T_e \\ u^- = 1, & (k+d)\,T_e \le (k+1)\,T_e \end{cases} \tag{2.39}$$

At high switching frequency by means of replacing $\bar{u}$ by a smooth function known as the equivalent control signal $\bar{u}_{eq}$, the equivalent control is determined using the invariance conditions by setting $S = 0$ and $\dot{S} = 0$ as

$$\begin{aligned}\bar{u}_{eq} &= -\left[J^T P\right]^{-1} J^T [Oe] \\ &= \frac{L}{V_{out}-V_{in}}\left(\frac{K_1}{K_2}-\frac{1}{RC}\right) i_C - \frac{K_3}{K_2}\cdot\frac{LC\left(V_{ref}-V_{out}\right)}{V_{out}-V_{in}}\end{aligned} \tag{2.40}$$

where an approximation is adopted as

$$i_C = C\frac{dV_C}{dt} \approx C\frac{dV_{out}}{dt} \tag{2.41}$$

By setting

$$K_{P1} = L\left(\frac{K_1}{K_2}-\frac{1}{RC}\right), K_{P2} = \frac{K_3}{K_2}LC \tag{2.42}$$

The duty cycle d becomes

$$d = u_{eq} = 1-\bar{u}_{eq} = 1 - \frac{K_{P1} i_C}{V_{out}-V_{in}} + \frac{K_{P2}\left(V_{ref}-V_{out}\right)}{V_{out}-V_{in}} \tag{2.43}$$

To verify the existence condition, as discussed in Section 2.3.1, it should be analysed in two cases in order to determine the sliding motion range.

$$\begin{cases} \dot{S}(e)\Big|_{S(e)\to 0^+,\bar{u}=u^+=0} = J^T Oe + J^T P\bar{u} < 0 \\ \qquad\qquad = -K_1\dfrac{i_C}{C} + K_2\dfrac{i_C}{RC^2} + K_3\left(V_{ref}-V_{out}\right) < 0 \\ \dot{S}(e)\Big|_{S(e)\to 0^-,\bar{u}=u^-=1} = J^T Oe + J^T P\bar{u} > 0 \\ \qquad\qquad = -K_1\dfrac{i_C}{C} + K_2\dfrac{i_C}{RC^2} + K_3\left(V_{ref}-V_{out}\right) - K_2\left(\dfrac{V_{in}-V_{out}}{LC}\right) > 0 \end{cases} \tag{2.44}$$

Therefore the motion range can be obtained as

$$0 < -K_{P1} i_C + K_{P2}\left(V_{ref}-V_{out}\right) + \left(V_{out}-V_{in}\right) < V_{out}-V_{in} \tag{2.45}$$

Regarding stability issues of SM control, Laplace transform can be used in (2.35) to get the equation about $S(e)$ as

$$(s^2 + \frac{K_1}{K_2}s + \frac{K_3}{K_2})e_1 = 0 \tag{2.46}$$

The Routh's stability criterion given in Section 2.3.1 can also be used as a common approach to determine the sliding parameters in the case of the boost converter.

2.4.3 Simulation Results

The fixed-point simulations are carried out in Matlab using a hybrid model of the boost converter written in S-function. The boost converter performs a regulation of an input voltage 3V

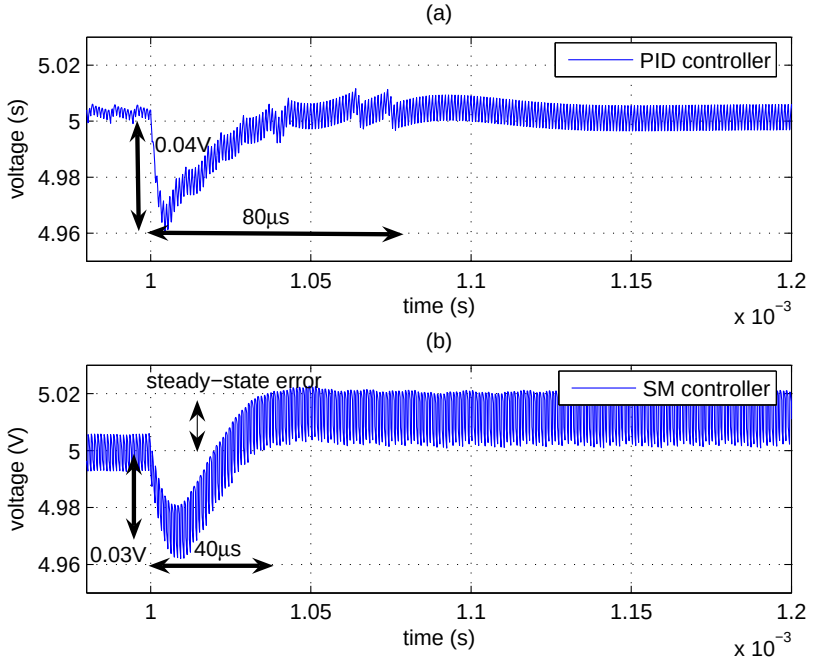


Figure 2.17: Dynamic responses under load change from 0.33A to 0.5A using (a) PID control-law, (b) SM control-law

to an output voltage of 5V. The filter inductor L=3.3μH, filter capacitor C=22μF, and the nominal load R_L=15Ω. The ESRs of the inductor and the capacitor are R_I=0.16Ω and R_C=3mΩ, respectively. All the circuit parameters in simulation have the same values as in the test board. The default switching frequency f_s=1MHz which is limited by the discrete components in the test board.

Considering the trade-off between the dynamic performances and robustness (modulus and delay margins) of a PID controller, the pulsation ω_{cr} is set to 14 times the open-loop pulsation ω_0 corresponding to 999449 rad/s with the closed-loop damping ratio $\zeta_{cr} = 0.7$. The SM control parameters are extracted from the stability conditions and the desired behavior. The damping ratio ζ is set to 0.75 and the pulsation $f_n = \dfrac{\omega_n}{2\pi}$ is set to one-sixtieth of the switching frequency to achieve better dynamic performances. So the following sliding parameters are obtained

$$\frac{K_1}{K_2} = 4\pi\frac{f_s}{60} \quad \text{and} \quad \frac{K_3}{K_2} = 4\pi^2\left(\frac{f_s}{60}\right)^2 \tag{2.47}$$

where f_s is the switching frequency. Simulation results shown in Fig. 2.17 illustrate the transient-state performances of PID and SM control-laws. The settling time is 40μs with 0.03V overshoot voltage for SM control, while settling time 80μs with 0.04V overshoot voltage for PID control. The SM control demonstrates better dynamic performances than the PID control for the boost converter. However, the steady-state error still occurs in the SM control that deteriorates the steady-state performances.

2.5 Summary

This chapter reviews important linear and nonlinear controllers for the buck converter, such as PID, RST, tri-mode and SM control-laws. A power-aware tri-mode controller for the buck converter is proposed along with improvements in terms of the stable operation and ASIC integration issues. Two of the most important controllers, linear PID and nonlinear SM control-laws, are also designed for the boost converter so as to verify the performances under such a non-minimum phase system exhibiting more serious nonlinearity. All referred controllers are realized into ASIC that is of possibility to evaluate the power consumptions in Chapter 7. In order to further improve the dynamic performances, a novel controller using predictive concept will be introduced in the next chapter.

Chapter 3

Direct Control with Dual-state-variable Prediction

As reviewed in Chapter 1, a double closed-loop control is often adopted with an outer voltage-loop and an inner current-loop. Dead-beat control is widely used for the inner current-loop. These control algorithms calculate the duty cycle according to a converter discrete model at every sampling period to make sure the inductor current tracks the reference in the next period. The current reference is generated by a classical voltage control loop. So the prediction is only made for the current-loop but not for the voltage-loop that restricts the dynamic performances. Moreover, due to its dependence on inductor current sensor, it cannot support high switching frequency.

In this chapter, a novel digital controller is proposed for the high switching frequency buck converter based on the principle of predictive control. Unlike the double closed-loop control method in the traditional current-mode predictive controller, the prediction of both the inductor current and the output voltage are performed at the same time by adopting a flexible PWM pattern that enables dynamic adjustment of the time of the voltage events (see Fig. 3.1(b)). The so called "direct control with dual-state-variable prediction (DDP control)" accelerates the convergence rate during transients, while inherently preserving the rejection of power and reference perturbations. With the knowledge of inductor current, the performances of the DDP controller are also analysed compared to a dead-beat controller.

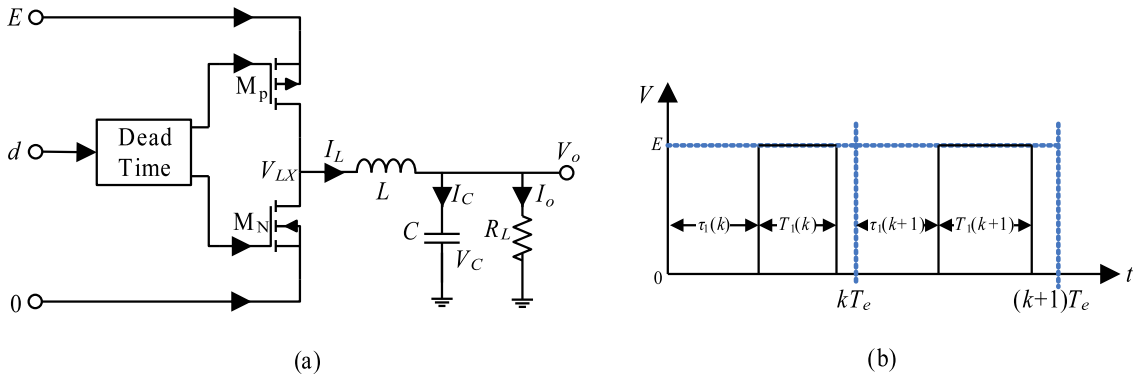


Figure 3.1: (a) Block diagram of the buck converter, (b) a sample of corresponding current and voltage predictive control waveform

3.1 Discrete Model of the Buck Converter

As shown in Fig. 3.1(a), the supply voltage is denoted E. The switched voltage, V_{LX}, is filtered through a LC tank to provide a constant output voltage, V_o, to the load, R_L. We do not take into account the capacitor ESR so that the output voltage V_o is regarded as equal to the capacitor voltage V_C. Only the continuous conduction mode (CCM) is considered. Choosing the inductor current and the capacitor voltage as the state variable $x(t) = \begin{bmatrix} I_L \\ V_C \end{bmatrix}$, the state equations of the buck converter in CCM can be written as

$$\dot{x}(t) = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix} x(t) + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix} u(t) \tag{3.1}$$

$$y(t) = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} x(t) \tag{3.2}$$

where the input variable $u(t) = \begin{bmatrix} E \\ I_o \end{bmatrix}$ when the PMOSFET is ON, $u(t) = \begin{bmatrix} 0 \\ I_o \end{bmatrix}$ when the NMOSFET is ON.

Assuming only a small variation of the output current I_o during a switching period T_e (that is to say, $\Delta I_o(k) \approx 0$), the input variable can be considered to be constant during T_e. So the discrete-time model of the buck converter limited to the first-order can be expressed as

$$x(k+1) = \begin{bmatrix} 1 & -\frac{T_e}{L} \\ \frac{T_e}{C} & 1 \end{bmatrix} x(k) + \begin{bmatrix} \frac{T_e}{L} & \frac{T_e^2}{2LC} \\ \frac{T_e^2}{2LC} & -\frac{T_e}{C} \end{bmatrix} u(k) \tag{3.3}$$

The description of the system state-space allows to analyze the behavior of the buck converter. The aim of the DDP controller is to make the inductor current and the capacitor voltage at the sampling point $(k+1)T_e$ equal to the reference current and voltage at the end of the corresponding

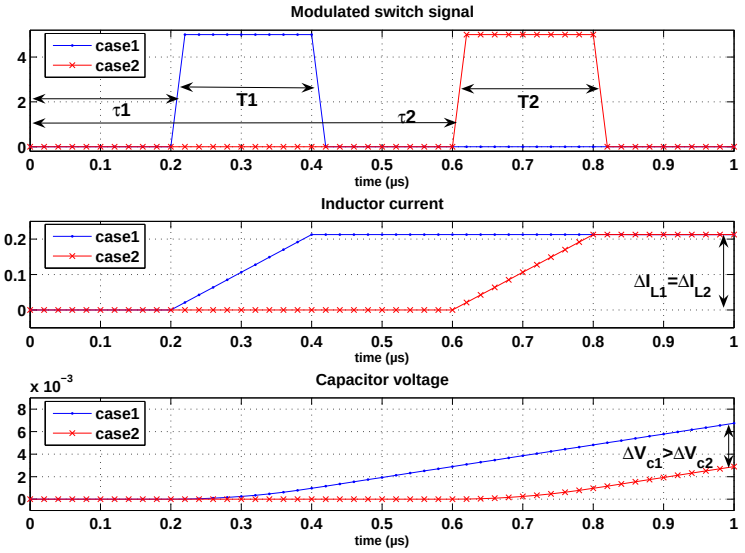


Figure 3.2: System variables in one switching period with different voltage events

switching period, respectively.

3.2 DDP Control Pattern

A simulation of each system variable in the buck converter during one switching period illustrates the relations between the switch signal d, the inductor current I_L and the capacitor voltage V_C, as shown in Fig. 3.2. There are two cases in Fig. 3.2. The durations of the positive voltage pulse in both of the two cases are equal, that is $T_1(k) = T_1'(k)$, while the duration before the trip point $\tau_1'(k) > \tau_1(k)$. From Fig. 3.2, the increase in the inductor current $\Delta I_L(k)$ is identical, however, the corresponding capacitor voltage $V_C(k)$ in $case1$ increases a little faster than that in $case2$. So in each switching period, the positive duration $T_1(k)$ directly determines the increase in the inductor current, while, the interval before the voltage event $\tau_1(k)$ can influence the capacitor voltage. Next, a theory analysis is performed to investigate the relations between the circuit variables and the two PWM control parameters (T_1 and τ_1) based on the calculation of the inductor current variation, $\Delta I_L(k)$, and the capacitor voltage variation, $\Delta V_C(k)$.

3.3 Calculation of the Current Variation

The PWM waveform pattern of the DDP control is shown in Fig. 3.1(b). The switching period is divided into three parts. Providing that all the current variations are defined as $\Delta I_i(k) = I_i(k+1) - I_i(k)$, the change in I_L over two adjacent cycles, $\Delta I_L(k)$, is derived as

$$\begin{cases} \Delta I_{L1}(k) = -\dfrac{1}{L} V_C(k)\,\tau_1 \\ \Delta I_{L2}(k) = -\dfrac{1}{L}\left(-ET_1 + V_C(k)\,T_1\right) \\ \Delta I_{L3}(k) = -\dfrac{1}{L}\left(V_C(k)\,T_e - V_C(k)\,\tau_1 - V_C(k)\,T_1\right) \end{cases} \tag{3.4}$$

where the three parts fall into $\left[\ 0;\quad \tau_1\ \right]$, $\left[\ \tau_1;\quad \tau_1 + T_1\ \right]$ and $\left[\ \tau_1 + T_1;\quad T_e\ \right]$, respectively. So accumulating over the three parts, the total change of I_L over one switching period is

$$\Delta I_L(k) = \sum_{i=1}^{3} \Delta I_{Li}(k) = \frac{1}{L}\left(E \cdot T_1(k) - V_C(k) \cdot T_e\right) \tag{3.5}$$

From (3.5), we can derived that $\Delta I_L(k)$ is related to T_1 and the capacitor voltage $V_C(k)$. That is to say, T_1 in the next switching period can be, therefore, predicted from $\Delta I_L(k)$ which dictates that the inductor current in the next cycle is compensated with the amount of $\Delta I_L(k)$. So $T_1(k+1)$ is represented as

$$T_1(k+1) = \frac{L}{E}\Delta I_L(k) + \frac{T_e}{E} V_C(k) \tag{3.6}$$

3.4 Calculation of the Voltage Variation

From the perspective of a current variation, the three parts in one switching cycle can be expressed as

$$\begin{cases} I_{C1}(t) = I_C(k) + \dot{I}_{C0}(k) \times t \\ I_{C2}(t) = I_C(k) + \dot{I}_{C0}(k) \times \tau_1 + \dot{I}_{C1}(k) \times t \\ I_{C3}(t) = I_C(k) + \dot{I}_{C0}(k) \times \tau_1 + \dot{I}_{C1}(k) \times T_1 + \dot{I}_{C0}(k) \times t \end{cases} \tag{3.7}$$

where the three parts also fall into aforementioned intervals. $I_C(k)$ denotes the capacitor current at the starting point of each period. $\dot{I}_{C0}(k)$ and $\dot{I}_{C1}(k)$ are the change rates of the capacitor current during the intervals of τ_1 and T_1 respectively. Here we define the capacitor voltage variation as $\Delta V_C(k+1) = V_C(k+1) - V_C(k)$. The corresponding variation of the capacitor voltage over a switching period is, therefore, described as

$$\begin{cases} \Delta V_{C1}(k+1) = \dfrac{1}{C}\displaystyle\int_0^{\tau_1} I_{C1}(t)\,dt \\ \Delta V_{C2}(k+1) = \dfrac{1}{C}\displaystyle\int_0^{T_1} I_{C2}(t)\,dt \\ \Delta V_{C3}(k+1) = \dfrac{1}{C}\displaystyle\int_{\tau_1+T_1}^{T_e} I_{C3}(t)\,dt \end{cases} \tag{3.8}$$

Accumulating over the three intervals, as well as applying the prediction concept to both control variables τ_1 and T_1, the overall voltage change across the filter capacitor can be derived as

$$\Delta V_C\left(k+1\right)=\sum_{i=1}^{3}\Delta V_{Ci}\left(k+1\right)=b_1\left(k+1\right)\times\tau_1\left(k+1\right)+b_0\left(k+1\right) \tag{3.9}$$

where

$$b_1\left(k+1\right)=-\frac{E\cdot T_1\left(k+1\right)}{LC} \tag{3.10}$$

and

$$b_0\left(k+1\right)=-\frac{E}{2LC}T_1(k+1)^2+\frac{ET_e}{LC}T_1\left(k+1\right)+\frac{I_C\left(k\right)}{C}T_e+\frac{\dot{I}_{C0}\left(k\right)}{2C}T_e^2 \tag{3.11}$$

From (3.9), (3.10) and (3.11), the increase in the capacitor voltage is associated to both τ_1 and T_1. τ_1 can be then expressed as

$$\begin{aligned}\tau_1\left(k+1\right)&=\frac{\Delta V_C\left(k+1\right)-b_0\left(k+1\right)}{b_1\left(k+1\right)}\\&=T_e-\frac{T_1\left(k+1\right)}{2}+\frac{L}{2E\cdot T_1\left(k+1\right)}\left(2I_C\left(k\right)T_e+\dot{I}_{C0}\left(k\right)T_e^2-2C\cdot\Delta V_C\left(k+1\right)\right)\end{aligned} \tag{3.12}$$

(3.6) and (3.12) determine directly the two PWM control parameters.

Fig. 3.3 shows a simulation example of the dynamic range for normalized values of T_1 and τ_1, written as ρT_1 and $\rho\tau_1$, in which the supply voltage E=3V, the inductor value L=4.7μH, the capacitor value C=22μF, and the normalization constant, that is the switching period T_e=1μs. The capacitor voltage is here approximately equal to the reference voltage $V_C=V_{ref}=1.5$ V. The extreme condition occurs at the two ends of the period that satisfy the curve presented as

$$\rho T_1\left(k+1\right)=\begin{cases}1-\sqrt{1+\dfrac{2F}{T_e^2}} & \tau_1{=}\,0\\ \dfrac{\sqrt{2LC\Delta V_C\left(k+1\right)-2LI_C\left(k\right)T_e-L\dot{I}_{C0}\left(k\right)T_e^2}}{T_e\sqrt{E}} & \tau_1{=}T_e-T_1\end{cases} \tag{3.13}$$

where

$$F=\frac{L}{2E}\left(2I_C\left(k\right)T_e+\dot{I}_{C0}\left(k\right)T_e^2-2C\Delta V_C\left(k+1\right)\right) \tag{3.14}$$

(3.13) and (3.14) illustrate the possible extreme values of T_1 and τ_1. It also provides an approach to anticipate the best transient-state performances and to interpret the current-limit response discussed in [Corradini 10].

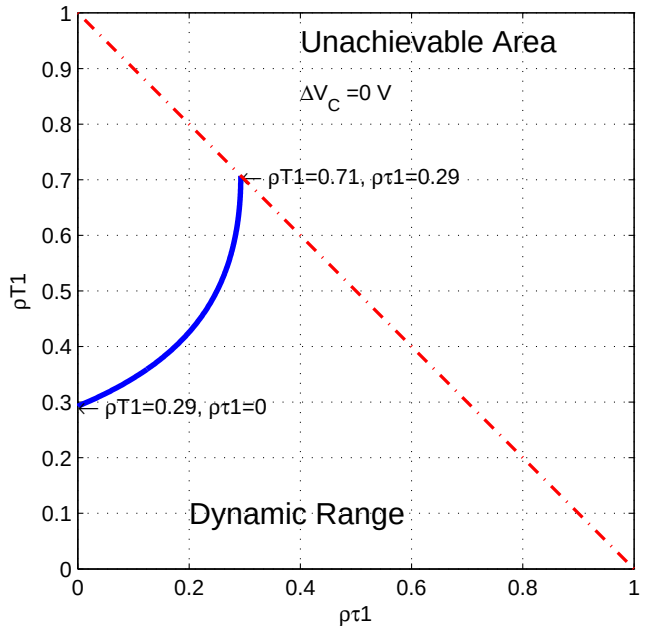


Figure 3.3: Dynamic range and the corresponding tracking curve

3.5 Operation of the Proposed Controller

Although (3.6) and (3.12) offer a calculation method for the modulated signals, as a matter of fact, they cannot give indication about the operation procedure including the generation of the predictive current and voltage. In order to simplify the analysis, (3.6) and (3.12) are represented respectively by

$$T_1(k+1) = f\left(\Delta I_L(k), V_C(k)\right) \tag{3.15}$$

$$\tau_1(k+1) = g\left(T_1(k+1), I_C(k), \dot{I}_{C0}(k), \Delta V_C(k+1)\right) \tag{3.16}$$

In order to obtain T_1 by (3.15), $V_C(k)$ and $\Delta I_L(k)$ are necessary values. If we ignore the capacitor equivalent series resistance (ESR), the output voltage can be considered as the required $V_C(k)$ so that it can be obtained at every switching period.

$\Delta I_L(k)$ is another necessary variable. Because the current sensor cannot support high switching frequency (200 kHz maximum), as well as an observer or an estimator take many calculation operations, a simple solution supporting high switching frequency is therefore required. The output voltage is a slowly varying signal and can be considered invariant during the current switching period, that is to say, $\Delta I_o(k) \approx 0$. Referring to the definition of $\Delta V_C(k+1)$, $\Delta I_L(k)$ can be expanded as

$$\Delta I_L(k) = C\frac{d\Delta V_C(k)}{dt} = C\frac{\Delta V_C(k+1) - \Delta V_C(k)}{T_e} \tag{3.17}$$

Substituting the reference capacitor voltage $V_{C,ref}(k)$ for the capacitor voltage in the next cycle

$V_C(k+1)$, (3.17) can be rewritten as

$$\Delta I_L(k) = \frac{C}{T_e}\left(V_{C,ref}(k) - 2V_C(k) + V_C(k-1)\right) \tag{3.18}$$

As above, T_1 can be obtained using the capacitor voltage prediction approach without any physical current sensor.

In (3.16), the calculation of τ_1 does not only depend on T_1 but also on $\Delta V_C(k+1)$, $\dot{I}_{C0}(k)$ and $I_C(k)$. The same voltage prediction approach is adopted so as to interpret $\Delta V_C(k+1)$ as

$$\Delta V_C(k+1) = V_{C,ref}(k) - V_C(k) \tag{3.19}$$

$\dot{I}_{C0}(k)$ stands for the reduction rate of the capacitor current during $\tau_1(k)$. An additional assumption is that $I_o(k)$ varies slowly over the adjacent periods. Also we take into consideration that $V_L(k) = -V_C(k)$ during the interval $\tau_1(k)$ because the ground ends of the inductor and capacitor keep at the same potential (see Fig. 3.1). The following equation applies in this case

$$\dot{I}_{C0}(k) = \frac{\Delta I_C(k)}{\Delta t} = \frac{\Delta I_L(k)}{\Delta t} = \frac{V_L(k)}{L} = -\frac{V_C(k)}{L} \tag{3.20}$$

The following analysis provides a method to estimate $I_C(k)$. Provided that the inductor current verifies $I_L(k+1) = I_o(k+1) + I_C(k+1)$, it can be expanded as

$$\Delta I_L(k) = I_o(k) - I_L(k) + \Delta I_o(k) + I_C(k+1) \tag{3.21}$$

The aforementioned assumptions are found to be suitable. Firstly, $\Delta I_o(k)$ approximates to zero if there is no significant load variation. Secondly, the predicted capacitor current satisfies $I_C(k+1) = I_{C,ref}(k) = 0$. Therefore, (3.21) can be simplified as

$$\Delta I_L(k) = I_o(k) - I_L(k) \tag{3.22}$$

According to (3.22), $I_C(k)$ can be solved as

$$I_C(k) = I_L(k) - I_o(k) = -\Delta I_L(k) \tag{3.23}$$

where $\Delta I_L(k)$ has already been obtained by (3.18). So the above analysis offers a feasible current predictive approach without sensor so as to obtain τ_1.

Fig. 3.4 summarizes the operation of the DDP controller. Besides the fixed converter parameters, the basic principles of predictive control are used only with the measured output voltage and the corresponding reference voltage. τ_1 and T_1 can be generated from the predicted $\Delta V_C(k+1)$ and $\Delta I_L(k)$.

3.6 Dynamic Range of τ_1 and T_1

According to (3.6), a range of $T_1(k+1)$ from 0 to T_e leads to the range of the predictive inductor current variation to make it possible to follow $V_{C,ref}(k)$ after each switching period,

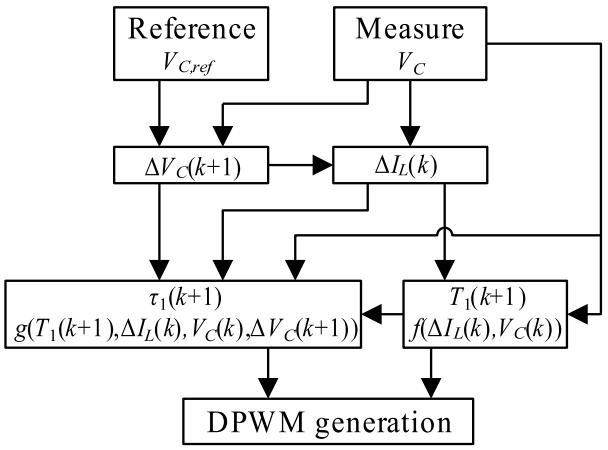


Figure 3.4: Operation of the DDP controller

following

$$-\frac{T_e}{L}V_C\left(k\right) < \Delta I_L\left(k\right) < \frac{T_e}{L}\left(E - V_C\left(k\right)\right) \tag{3.24}$$

The overall influence on V_C, here to be regarded as the output voltage V_o, requires an appropriate voltage margin that permits better dynamic performances, particularly, the immunity to the variation of the supply voltage and the tracking of the reference voltage. From (3.9), (3.10) and (3.11), the two extremes are given by

$$\begin{cases} \Delta V_{C,\max} = b_0 = -\dfrac{E}{2LC}T_1(k+1)^2 + \dfrac{E\cdot T_e}{LC}T_1\left(k+1\right) + \dfrac{I_C\left(k\right)}{C}T_e + \dfrac{\dot{I}_{C0}\left(k\right)}{2C}T_e^2 \\ \Delta V_{C,\min} = b_1 \times \left(T_e - T_1\left(k+1\right)\right) + b_0 = \dfrac{E\cdot T_1(k+1)^2}{2LC} + \dfrac{I_C\left(k\right)}{C}T_e + \dfrac{I_{C0}\left(k\right)}{2C}T_e^2 \end{cases} \tag{3.25}$$

$\Delta V_{C,\max}$ is satisfied when $\tau_1 = 0$, while $\Delta V_{C,\min}$ is achieved when $\tau_1 = T_e - T$. As shown in Fig. 3.4, the values of $\Delta I_L\left(k\right)$ and $\Delta V_C\left(k\right)$ are necessary factors that influence the two control variables τ_1 and T_1. The dynamic ranges and the corresponding effects on τ_1 and T_1 can be therefore summarized as

- The dynamic range of T_1 is limited from 0 to T_e and permits the adjustment of I_L within the margin given in (3.24);
- The dynamic range of τ_1 is limited from 0 to $T_e - T_1$ and permits the adjustment of V_C with the limits given in (3.25);
- The adjustment of V_C does not only depend on τ_1 but also on T_1, that is to say, in relationship with $\Delta I_L\left(k\right)$.

Based on the above analysis, the maximum voltage change occurs if and only if $\tau_1 = 0$, and the minimum one achieves at $\tau_1 = T_e - T_1$. The basic control scheme is given by the results of T_1 (3.6) and τ_1 (3.12). Since it is updated at every switching period, the scheme achieves the reference voltage in its best effort as mentioned above.

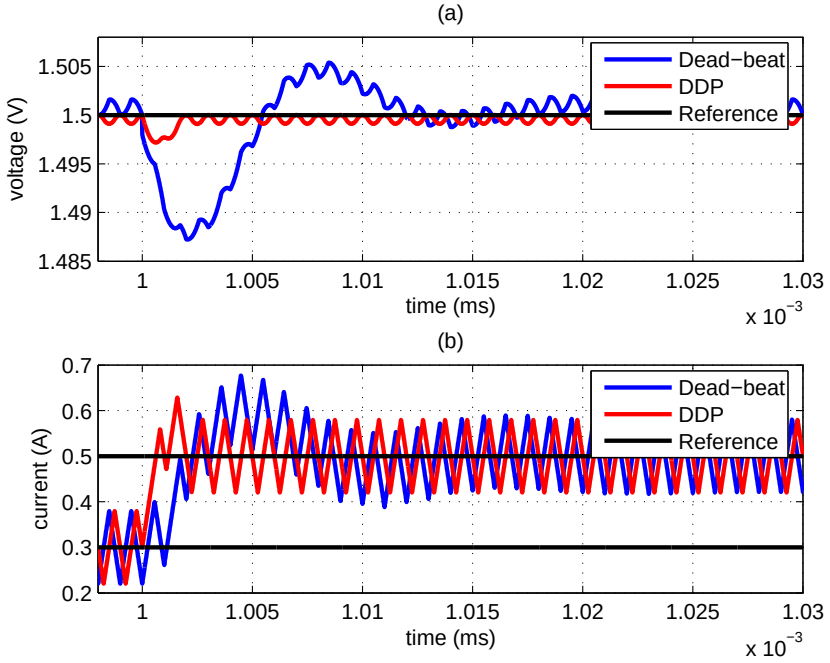


Figure 3.5: Dynamic performances of the DDP and dead-beat controllers operating at 1MHz switching frequency respectively (a) voltage responses, (b) inductor current regulations

3.7 System Analysis and Simulation Results

The fixed-point simulations are carried out using Matlab with a non-ideal buck model written in S-function. The buck converter transforms an input voltage of 3V to an output voltage of 1.5V. The default switching frequency f_s=1MHz, filter inductor L=4.7μH, filter capacitor C=22μF, and the nominal load R_L=5Ω. The ESRs of the inductor and the capacitor are R_I=0.2Ω and R_C=3mΩ, respectively. The switching frequency is limited by the discrete active components in the test board.

As discussed in Section 3.2, the DDP controller can generate an asymmetric modulation pattern that is capable of further boosting the dynamic performances than that of traditional current-mode controllers. With the knowledge of the inductor current which is possibly obtained by a sensor, an observer or an estimator, we take the predictive dead-beat controller as a reference to take a better comparison of the current regulation effect [Bibian 02]. Fig. 3.5 shows the dynamic behaviors in the transient-state when the load current changes from 0.3A to 0.5A. An obvious observation from Fig. 3.5(a) is that the regulation rate of the DDP controller is significantly faster than that of the dead-beat controller. The settling time of DDP controller is 2μs, while that of the dead-beat control is 12μs. The corresponding overshoot voltage is only 2.5mV (0.15% of the specified output voltage), instead of 15mV for the dead-beat controller. Inherent novel regulation variables in the DDP controller can be used to explain this fast convergence phenomenon which is also illustrated in the change rate of the inductor current as shown in Fig. 3.5(b). It only requires two switching periods under this transient-state condition.

As a feasible representation, the state-space plane (V_e, I_C) defined by the voltage error V_e =

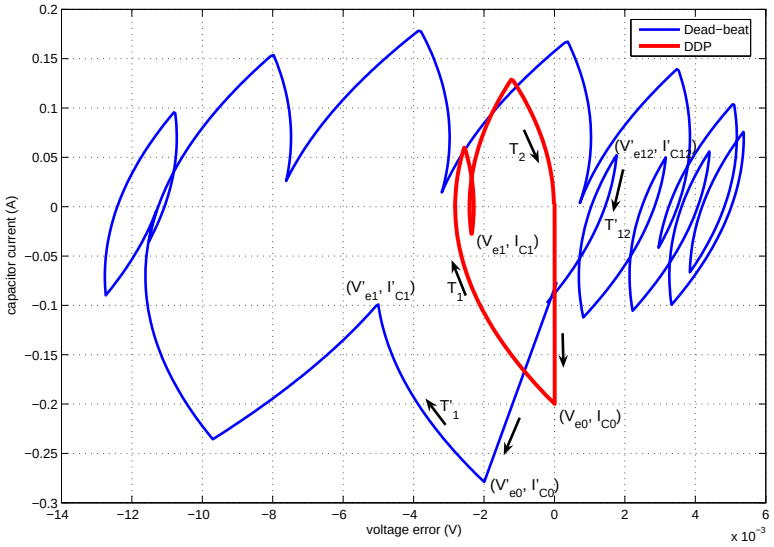


Figure 3.6: State-space representation (V_e, I_C) to describe the transient-state performances of the DDP and deadbeat controllers respectively

$V_C - V_{C,ref}$ and by the capacitor current I_C can be used to analyze the dynamic performances. Referring to Fig. 3.6, the transient-state behaviors of the DDP controller can be handled as follows. Firstly, the load current change forces the state variables to the initial condition (V_{e0}, I_{C0}). Then the DDP controller starts to regulate the output voltage V_C (here expressed as the error voltage V_e) by a series of new PWM patterns. The last switching action occurs at (V_{e1}, I_{C1}). Two switching periods (T_1 and T_2) are required before returning to the steady-state point. There is no positive overshoot ($V_e < 0$) over the whole operation. The dead-beat controller requires 12 switching periods to return to the steady-state point as well as a large part operating in the positive overshoot region. Because the enclosed area represents the power losses during transient-state, the DDP controller shows better transient-state performance than the dead-beat controller.

By adopting the operations described in Section 3.5. Fig. 3.7 compares other control-laws against the DDP control under load changes in 4MHz switching frequency. The counterparts include the linear PID, robust RST and the nonlinear SM controllers. All referred controllers do not necessarily require a current sensor. Table. 3.1 shows a comparison of the dynamic performances. Four comments can be made with respect to Fig. 3.7 and Table. 3.1. First, the DDP controller generates the smallest size of steady-state output ripples. Second, compared to the traditional linear PID controller, it exhibits better dynamic performance. Third, it is excellent to reject the steady-state error that will be introduced in indirect type of SM controller without double integral sliding surface. Finally, as a robust form of PID controller, the robust RST controller shows comparable dynamic performances as the DDP control, but it occupies more hardware resources than the DDP controller. This issue will be discussed in Chapter 5 along with the experimental results.

The converter gives a regulated output that ranges from 0.4V to 2.5V as shown in Fig. 3.8(a). The converter can track within a large output range.

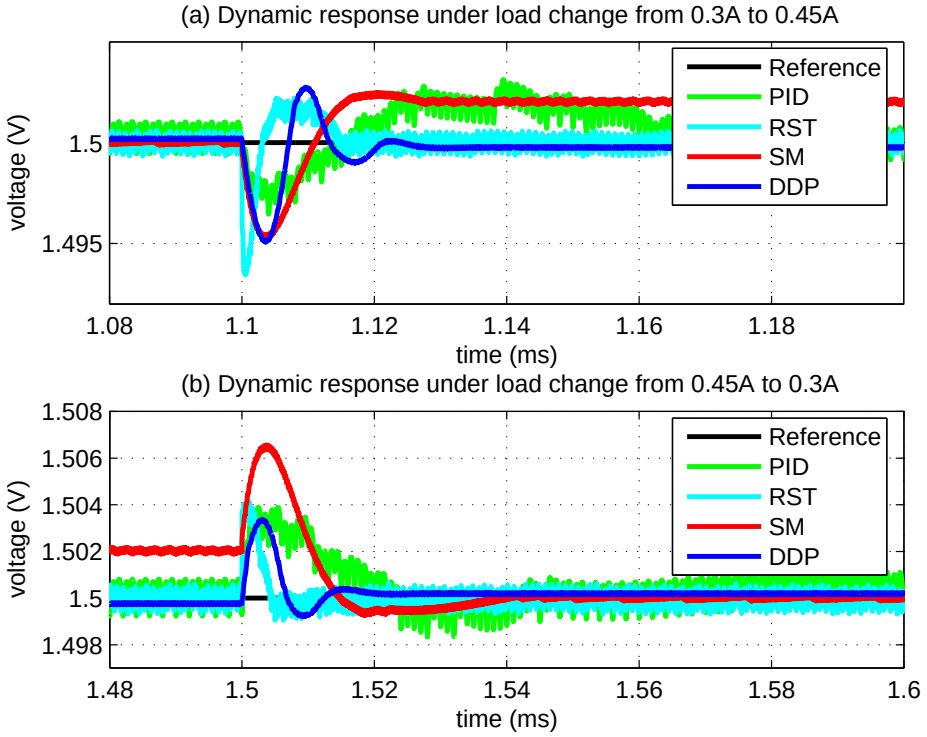


Figure 3.7: Dynamic responses under load current change (0.3A → 0.45A → 0.3A) using DDP, PID, RST and SM control-laws operating at 4MHz switching frequency

Table 3.1: Dynamic performances of the DDP controller compared to other popular controllers based on simulation results at 4MHz switching frequency

Controller type	Settling time 0.3A →0.45A (μs)	Settling time 0.45A→0.3A (μs)	Negative overshoot (mV)	Positive overshoot (mV)
DDP controller	11	16	5	3
RST controller	10	15	7	4
SM controller	16	40	5	5
PID controller	60	49	6	5

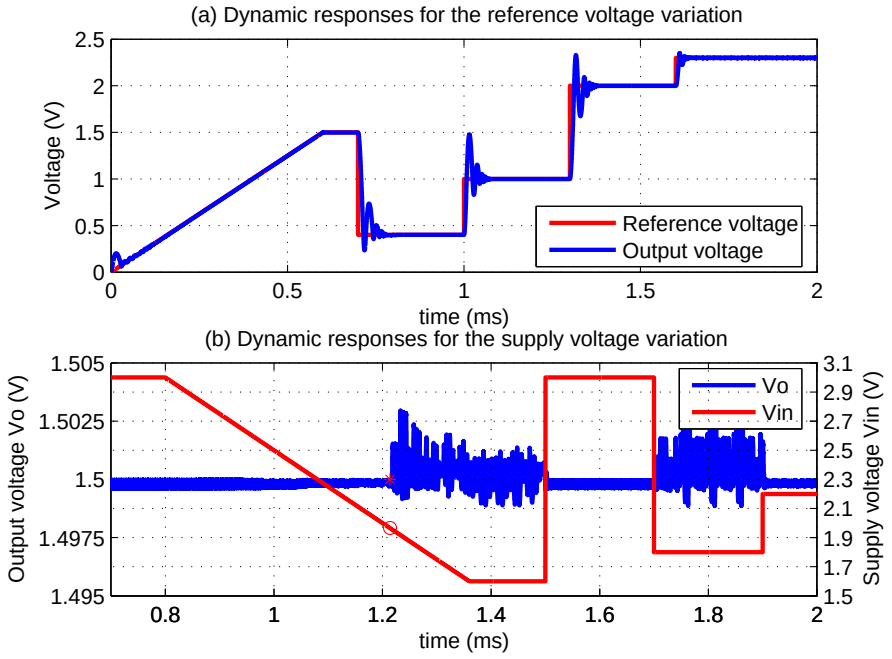


Figure 3.8: (a) Dynamic responses for the reference voltage variation as well as the slope trajectory tracking, (b) dynamic responses for the supply voltage variation in slope mode and transition mode

When the power supply has an input disturbance from 3V to 1.6V, the regulated output voltage is shown in Fig. 3.8(b). The slope mode test from 1.2ms to 1.5ms shows that the supply voltage must be larger than 1.96V. A very short convergence time shown in the transition mode test in Fig. 3.8(b) guarantees an excellent performance to reject the input voltage disturbance.

3.8 Summary

A full synthesizable PWM-based DDP control is proposed for high switching frequency, low power buck converter. The predictions of the inductor current and the capacitor voltage are performed simultaneously by adopting a flexible PWM pattern that enables dynamic adjustment of the time of the voltage events. The DDP control preserves the merits of predictive current-mode control and allows to further improve the dynamic performances. The dynamic performances of the DDP controller are analyzed compared to reviewed dead-beat, PID, RST and SM controllers to demonstrate the advantages with respect to the load perturbations. The performances of the rejection to the reference and input voltage perturbations are also verified in this chapter. Experimental results at high switching frequency up to 4MHz will be given in Chapter 5. In the next chapter, we will focus on another module in the feedback loop, DPWM.

Chapter 4

Quantizers and Peripheral Building Blocks

As mentioned in Chapter 1, two quantizers including DPWM and ADC are performed as the interfaces between the control-law and the power stage. The quantizers will bring in the closed-loop constrains in terms of LCO, the tiny intervals in the two quantizers to achieve high switching frequency, etc. Details concerning the implementation of ADC can benefit the delay-line architecture and the windows concept. Since ADC is not the main scope of this thesis, it will not be elaborated in this chapter. In this chapter, we will focus our attention on DPWM techniques. The challenge to design an appropriate DPWM depends not only on the closed-loop requirement, but also on the implementation feasibility that consumes acceptable power. Two possible techniques cover the generation of small intervals by the delay-cell-based methods and the time-domain averaging techniques by the Σ-Δ modulation or the effective dither. In fact, above methods can be regarded as two high frequency clock generation approaches in time-domain and in frequency-domain respectively.

As reviewed in Table 1.4, Σ-Δ modulator for DPWM consumes less power than the delay-cell-based ones. In the first part of this chapter, after a review of Σ-Δ modulation techniques, a closed-loop analysis is given to demonstrate the effect of the Σ-Δ modulator. Since the DC-DC converter always outputs a constant DC voltage, the derived modulator performances with different orders under DC excitation permit us a way to avoid some idle-tone sensitive input words. Note that the DC excitation of the Σ-Δ modulator is the steady-state requirements associated directly with the converter output that has rarely been mentioned in previous articles.

1-1 MASH Σ-Δ DPWM proposed in [Guo 09b] is reconsidered and analysed in the second part of this chapter. According to the analysis, there is no improvement to the noise-shaping effect compared to the second-order Σ-Δ DPWM, although significant dynamic performance is anticipated to be improved. Here a dither generator is added to the 1-1 MASH Σ-Δ DPWM so

that it can effectively reduce the idle-tone effect without many additional hardware resources. Both the steady-state and transient-state analyses will be given along with the experimental results in Chapter 5.

In order to provide a stable clock with synchronous phase, PLL is another necessary building block located in the feedback loop. The third part of this chapter gives a cost effective approach adopting the delay-cell based VCO and the charge-pump based phase frequency detector. The adopted PLL is implemented using the $AustriaMicrosystemS$ 0.35μm CMOS process. The experimental result will be given in Chapter 6.

4.1 Σ-Δ Modulation for PWM

Normally, the basic Nyquist-rate converter samples the input data at the Nyquist-rate according to Shannon's sampling theorem. That is to say, the minimum sampling frequency f_s is required to be at least twice of the signal bandwidth f_b so as to ensure no loss in the input signal. So the minimum sampling rate is therefore $f_s = 2f_b$. Nyquist-rate converter normally requires a high-order filter to remove the out-band components without significant attenuation of the signal-band. If the sampling rate comes faster than twice the signal bandwidth f_b, that is $f_s \gg 2f_b$, the theory of oversampling is derived. Oversampling converter generally focuses on decreasing the quantization error power within the signal-band and on increasing the conversion accuracy. The two concerns are just the most important concepts to oversampling converters: oversampling and noise-shaping that determine the implementation of Σ-Δ modulator. ADC and digital-to-analog converter (DAC) are two main applications of Σ-Δ modulator. They operate with the inherent anti-aliasing filter that doesn't need independent sample/hold circuit so that they consume less power than the Nyquist-rate counterparts. Normally, the resolution is meanwhile limited due to the imperfect matching of the analog components and other non-ideal circuits.

As a building block of the digital controller, DPWM is of the most probability to occur in critical path during RTL synthesis. This type of possibility is derived from the required ultra-high clock frequency. In order to maintain the low-power feature as well as take less hardware resources, Σ-Δ modulator is one of the most cost-effective approaches.

4.1.1 Design of the Σ-Δ Modulation

The block diagram of the Σ-Δ DPWM is shown in Fig. 4.1. Taking into account the power plant, ADC and control-law along with the Σ-Δ DPWM, the loop illustrates a system-level perspective. That is just the advantage because the other necessary components across the loop perform the noise-shaping functions. The power converter acts as a low-power filter to eliminate the out of band noise, while the ADC oversamples the regulated output. Taking the buck converter as an example, it is the second-order LC lowpass filter with the corner frequency $f_b = \frac{1}{2\pi\sqrt{LC}}$ that limits the bandwidth of the output where L is the inductor value, C is the capacitor value. It leads to the oversampling rate as $OSR = \frac{f_s}{2f_b}$ where f_s here stands for the sampling rate of ADC. A diagram of the amplitude to frequency characteristic, including spectra of the noise, noise-filter

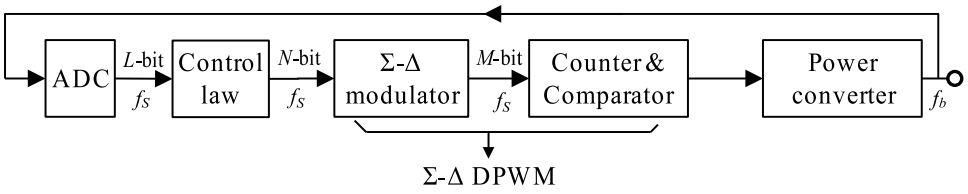


Figure 4.1: Block diagram of the Σ-Δ DPWM

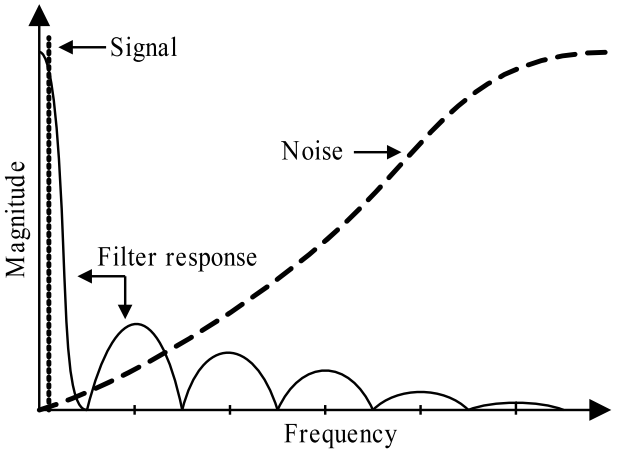


Figure 4.2: Amplitude frequency characteristic of oversampling modulator

and signal is given in Fig. 4.2. The multibit Σ-Δ modulator can effectively reduce the output word-length to the following counter-comparator based PWM, also known as "core DPWM". No analog-related block is required before the core DPWM due to the modulator attribute. Although truncation noise accompanied the in-band signal exposes at the output of the core DPWM, that is also the output of Σ-Δ DPWM, the LC filter in the power stage can perform as the lowpass filter to exclude the out-of-band noise and recreate the regulated output.

The relationship between the digital value and the corresponding modulated signal in time-domain depends on the bit of Σ-Δ $(M - N)$ and the architecture of adopted modulator. The error feedback structure, as a special configuration of Σ-Δ modulator, can be applied as the implementation architecture. Next, we will focus on the Σ-Δ modulator. A review of the error feedback structure and a common design approach of the Σ-Δ modulator will be given.

As shown in Fig. 4.3, we take the first-order Σ-Δ modulator as an example. Fig. 4.3(a) is the Σ-Δ quantizer. The input signal, $U(z)$, feeds to the quantizer via an integrator, and the quantized output, $V(z)$, feeds back to subtract from $U(z)$. Such feedback architecture forces the average quantized signal to follow $U(z)$. Any difference between $U(z)$ and $V(z)$ will be corrected by the integrator. The block diagram of the first-order modulator in z-domain, shown in Fig. 4.3(b), exhibits the relationship with practical implementation and can explain well the derivation of Σ-Δ quantizer. Referring to Fig. 4.3(b), the quantized output can be repressed as

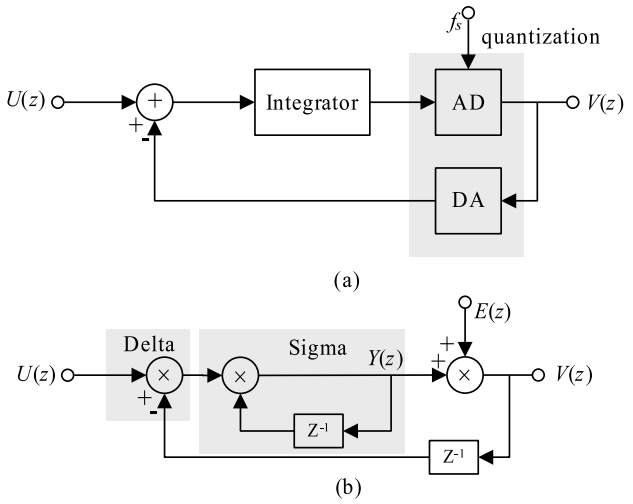


Figure 4.3: Block diagram of the first-order (a) Σ-Δ quantizer, (b) z-domain linear model

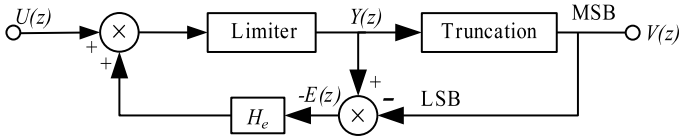


Figure 4.4: Error-feedback structure

$$\begin{aligned} V(z) &= Y(z) + E(z) = U(z) + \left(1 - Z^{-1}\right) E(z) \\ &= STF \cdot U(z) + NTF \cdot E(z) \end{aligned} \tag{4.1}$$

where $E(z)$ models the quantization error. The aim is to reduce the influence of $E(z)$ by a noise-shaping factor, such as $\left(1 - Z^{-1}\right)$ in (4.1). Here the noise transfer function is abbreviated as NTF. The corresponding signal transfer function is written as STF. The target of noise-shaping by the Σ-Δ modulator is to largely reduce the amplitude of quantization error $E(z)$ while rebuilds the original input. In (4.1), z^{-1} should indefinitely approach to 1 as

$$\lim_{f \to 0} z^{-1} = \lim_{f \to 0} e^{-j2\pi f} = 1 \tag{4.2}$$

According to (4.2), the effective frequency f must be maintained relatively low. It requires a high oversampling rate that moves most of the noise signal, $E(z)$, to a range of frequency spectrum higher than f. Analysis details can be found in [R. Schreier 05] and [Norsworthy 97].

From a viewpoint of noise-shaping effect, a so-called error-feedback model, as shown in Fig 4.4, is preferable if DPWM is the design target. The quantization error, $E(z)$, is defined as the difference between the input and output of the quantization block which is a bit truncation block when applying to DPWM. The error signal is then compared to the input voltage via a delay module H_e. Such circuit configuration shows the same signal and noise transfer function in (4.1)

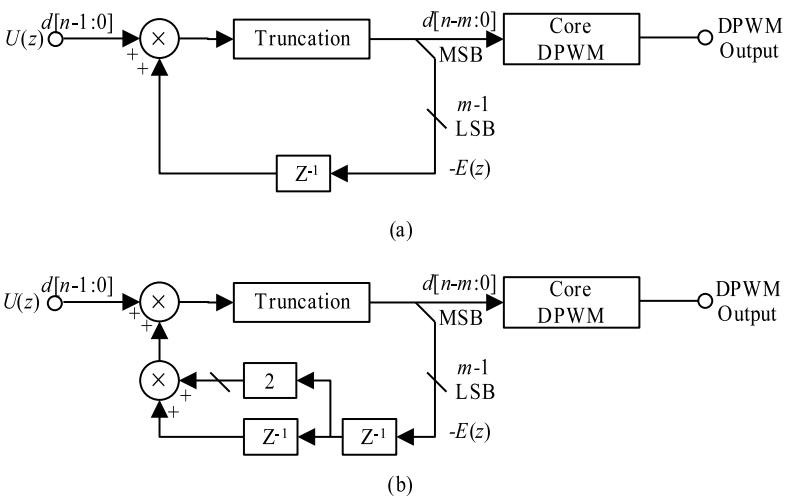


Figure 4.5: Block diagram of (a) the first-order DPWM, (b) the second-order DPWM

as

$$V(z) = STF \cdot U(z) + NTF \cdot E(z) = U(z) + (1 - H_e(z)) E(z) \tag{4.3}$$

It is easy to set the delay module in order to achieve different orders of noise-shaping effects. For example, $H_e = z^{-1}$ assures the first-order noise-shaping effect, while $H_e = z^{-1}\left(2 + z^{-1}\right)$ assures the second-order noise-shaping effect, and etc. The corresponding implementations of the first-order and second-order DPWMs are shown in Fig. 4.5(a) and (b) respectively.

The error-feedback model is not a good candidate for ADC due to the need for a high precise multi-level sub-DAC. However as the main implementation topology, it is very suitable for the digital implementation of PWM [R. Schreier 05]. All building blocks such as bit truncator, bit extension and unit delay modules are easy to be integrated into FPGA and ASIC. [Lukic 05] firstly put Σ-Δ method into use, known as the first-order Σ-Δ DPWM. The core DPWM is also a necessary part. It is subject to the applied power train in which the most important parameter is the corner frequency f_c. [Lukic 07] increases the noise-shaping function to the second-order to increase the effective resolution of DPWM with less magnitude low-frequency idle-tone because of the decreased periodicity of the resultant patterns. However, the idle-tone is still a critical challenge especially applied to DPWM, because most of the operating condition is under DC excitation. We will focus on this issue in the next section.

4.1.2 Σ-Δ Modulator under DC Excitation

Provided that internal or external perturbations don't turn up frequently, most operations of the DC-DC converter are in steady-state. So the performances of the Σ-Δ modulator mainly relies on the behavior under DC-excitation. However, Σ-Δ modulator inherently generates a periodic pattern called the idle-tone effect. Here we take the first-order modulator shown in Fig. 4.5(a) as an example. As shown in Fig. 4.6, 4-bit LSB constructs a feedback loop via the unit-delay so as

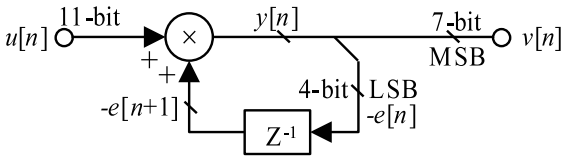


Figure 4.6: An implementation example of the first-order Σ-Δ modulator

Table 4.1: A variable and average duty-cycle example of the first-order Σ-Δ modulator

n	*u[n]*	*-e[n+1]*	*-e[n]*	*y[n]*	*v[n]*	average *v[n]*	average duty cycle
1	1006	0	14	1006	62	62	0.4844
2	1006	14	12	1020	63	62.5	0.48828
3	1006	12	10	1018	63	62.67	0.48958
4	1006	10	8	1016	63	62.75	0.49023
5	1006	8	6	1014	63	62.8	0.490625
6	1006	6	4	1012	63	62.833	0.49089
7	1006	4	2	1010	63	62.8571	0.49107
8	1006	2	0	1008	63	62.857	0.4910703
9	1006	0	14	1006	**62**	62.778	0.49045
10	1006	14	12	1020	**63**	62.8	0.490625
11	1006	12	10	1018	**63**	62.818	0.490767
12	1006	10	8	1016	**63**	62.833	0.49089
13	1006	8	6	1014	**63**	62.846	0.49099
14	1006	6	4	1012	**63**	62.857	0.49107
15	1006	4	2	1010	**63**	62.867	0.49115
16	1006	2	0	1008	**63**	62.875	***0.49121***
17	1006	0	14	1006	62	62.823	0.49081
18	1006	14	12	1020	63	62.833	0.49089
19	1006	12	10	1018	63	62.833	0.49095
20	1006	10	8	1016	63	62.842	0.49102

to realize the noise-shaping function. The truncated 7-bit most significant bit (MSB) is considered as the effective signal to be processed by the power filter. The target resolution is anticipated to be 11-bit (MSB&LSB). Table. 4.1 illustrates a part of the state variables as well as the anticipated results of the output duty-cycle under DC excitation. The corresponding waveform is shown in Fig. 4.7. The input signal, $u\,[n]$, is set to 1006 in decimal format. An observation can be obtained that the desired duty-cycle appearers at $n = 16$, and the oscillation amplitude of the average duty-cycle becomes smaller and smaller so as to converge to the target duty-cycle. Another observation from Table. 4.1 is that it exists a periodic sequence in $v\,[n]$ every 8 sampling points, from $n = 9$ to 16 for example. The periodic sequence will introduce a noise appearing at the output of the power stage if the frequency falls into the filter pass-band. This is the origin of idle-tone effect.

The higher-order Σ-Δ modulators can achieve a faster convergence speed than that of the lower-order ones [R. Schreier 05, Norsworthy 97, Johns 97]. The corresponding effective number of bit (ENOB) of Σ-Δ modulator can be expressed as

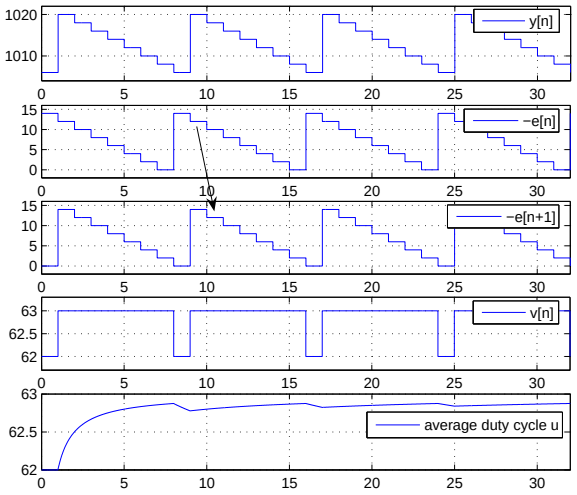


Figure 4.7: A simulation example of the first-order Σ-Δ modulator

$$N_{\Sigma-\Delta} = p \cdot \log_2 OSR \tag{4.4}$$

where OSR is the DPWM oversampling rate. p is the topology associated parameter of which normally the first-order is 1.5, the second-order is 2.5, etc [Johns 97]. The total resolution of a Σ-Δ DPWM depends on the sum of the core DPWM resolution and Σ-Δ modulator resolution.

In order to interpret the advantage of higher-order DPWM, a fixed-point simulation is performed in Matlab using a non-ideal buck converter model written in S-function. The default switching frequency is set to f_s=1MHz, filter inductor L=4.7μH, filter capacitor C=22μF, and the nominal load R_L=5Ω. The simulation model is shown in Fig. 4.8. It is composed of a configurable Σ-Δ modulator, a core DPWM and the power stage. The target resolution for the power stage is 11-bit with 6-bit core DPWM and 5-bit Σ-Δ DPWM. The input binary word in decimal format is 1025. Fig. 4.9 gives the modulator output with the first-order (MOD1), the second-order (MOD2) and the third-order (MOD3) Σ-Δ noise-shaping modules. It illustrates that the change rate of the output bins becomes faster as the noise-shaping order increases. The amplitude of steps, in the mean time, becomes larger. It just satisfies the conclusion in [Lukic 07]. So the low-frequency periodic sequence generated by the first-order modulator is attenuated by the higher-order ones. Such a periodic sequence generated by higher-order modulators is of greater possibility to be filtered out across the power stage. Such phenomenon can also be explained that the low-frequency idle-tone is moved to higher frequency by the more intensive scatter operations of the higher-order modulator. The outputs of the power converter regulated by a Σ-Δ DPWM with different orders as well as by an ideal 11-bit DPWM are shown in Fig. 4.10. Compared to the higher-order Σ-Δ DPWM, the regulated power converter output with the first-order DPWM exhibits obviously periodic oscillation. Such phenomenon is reduced in the second-order and third-order modulators. Thus it is clear that the corresponding amplitude of oscillation is reduced with an increase of Σ-Δ

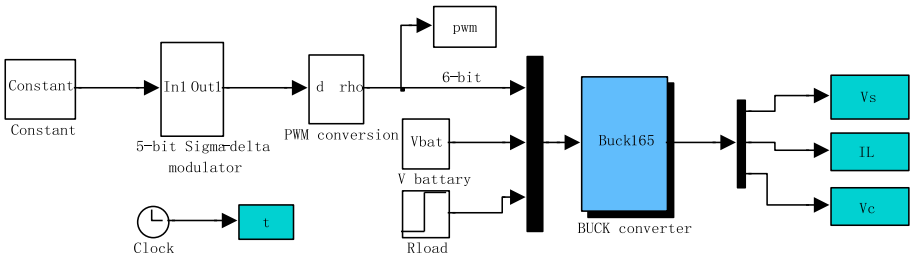


Figure 4.8: Matlab simulink model to interpret the behavior of a Σ-Δ modulator

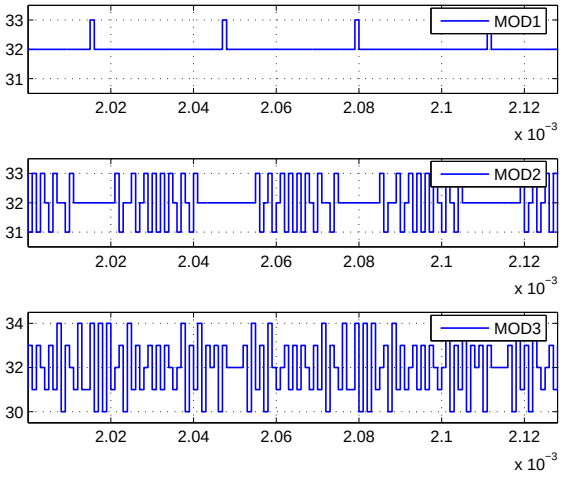


Figure 4.9: Outputs of the Σ-Δ modulators with different orders

order.

If we focus on the higher-order Σ-Δ DPWM, the decision for the word-length of the core DPWM and Σ-Δ modulator is still a problem. Smaller word-length for the core DPWM requires a bigger word-length for Σ-Δ DPWM what is of high potential to idle-tone. Meanwhile, a relatively bigger word-length for core DPWM implemented as counter-comparator architecture requires a higher clock frequency leading to strict requirements of timing and power issues. The analysis of such a trade-off is usually a complex function associated with all the building blocks shown in Fig. 4.8. Fortunately, simulation tool gives a feasible approach that is able to obtain an optimal choice.

Taking into account the filter response in the power stage, the total noise power of each input binary word is defined as the accumulation of power difference between the target modulator and the reference within half of the switching frequency. So an ideal 11-bit DPWM is simultaneously simulated to provide the reference. Fig. 4.11 shows the simulation results of in-band quantization noise power versus the input binary word. In Fig. 4.11(a), there are three floors exhibiting two types of in-band noise. The central floor can be regarded as an effective input binary word range floor which is constant and symmetrical to the central binary word (this case is 1024). All inputs falling in this floor can achieve better noise-shaping effect than other ones. The other two floors are placed at two ends of the binary word sweep range. So they are named “side floors”. They exhibit

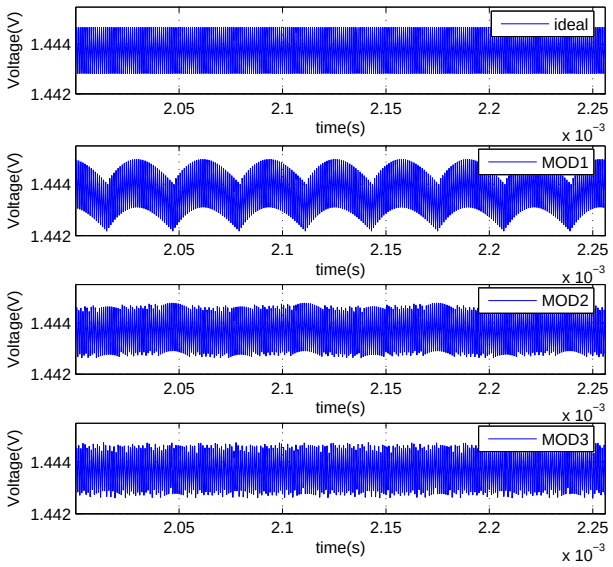


Figure 4.10: Regulated power converter outputs by the Σ-Δ DPWMs with different orders

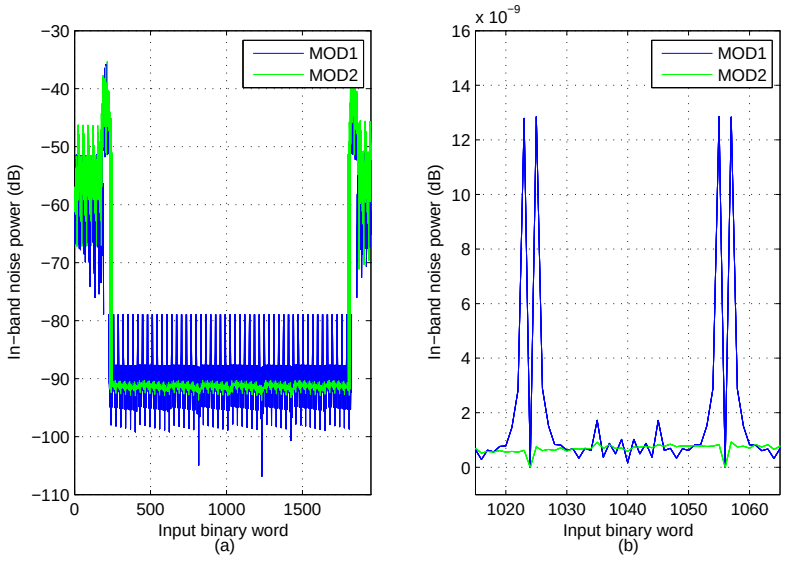


Figure 4.11: (a) In-band quantization noise power versus input binary word of the first-order and second-order modulators in the buck converter, (b) the periodic peak noise around a specific input binary word

weaker noise-shaping effect than the central floor. The following reasons explain the phenomenon

- Small enough or large enough input binary word is more prone to introduce saturation into the modulator leading to the repeated low frequency patterns that most likely appear at the converter output;
- Imperfect lowpass filter in the power stage (second-order for the buck converter) deteriorates the performance of the post analog filter and introduces more serious in-band noise, especially in the side floors;
- The in-band noise is of higher amplitude in the first-order DPWM than in the second-order. It just explains the pattern scattering effect discussed above.

Another obvious observation is that the in-band noise is more serious in the first-order DPWM than that in the second-order. Anyhow, Fig. 4.11(a) reveals the similarly behavioral characteristics compared to that of the linear model discussed in [Friedman 88, Candy 81, Norsworthy 97, R. Schreier 05]. Fig. 4.11(b) enlarges the central floor around the central input binary word (from 1015 to 1065). It shows that the peak noise power always occurs at

$$l \cdot 2^{n-m} \pm 1 \tag{4.5}$$

where n is the number of input bit, m is the number of output bit, $l \in \mathbb{Z}^+$ and $q_{th} \leq l \leq 2^m - q_{th}$. q_{th} is the absolute value of threshold in the central floor. A confidence interval can be obtained from the testbench in Fig. 4.8. The example requires the length of one side floor to be at least 12.5% of the total length of input binary word range, that is $q_{th} \geq 8$.

Provided that the input binary word maintains $l \cdot 2^{n-m}$, the minimum noise-shaping effect can be achieved for all modulators with different orders. It can be explained that all modulators generate the same output pattern without the sensitive periodic sequence. For example, the modulated outputs of all modulators with different orders to the input binary word 992 are the same output sequence as $\{31, 31, \ldots 31\}$.

Based on above analysis, a recommended design guideline of the Σ-Δ DPWM comes as follows

- Use less bit of Σ-Δ modulator so as to generate higher frequency periodical sequences that are more likely eliminated by the power filter;
- A higher order modulator is always preferable to attenuate the effect of idle-tone by inherent more intensive scatter operations;
- The estimation in (4.5) should be performed off-line to determine the idle-tone sensitive binary words. The corresponding regulated outputs should not fall into the set of sensitive outputs.

In the next section, a MASH Σ-Δ modulator along with the dither module is proposed to further reduce the idle-tone noise.

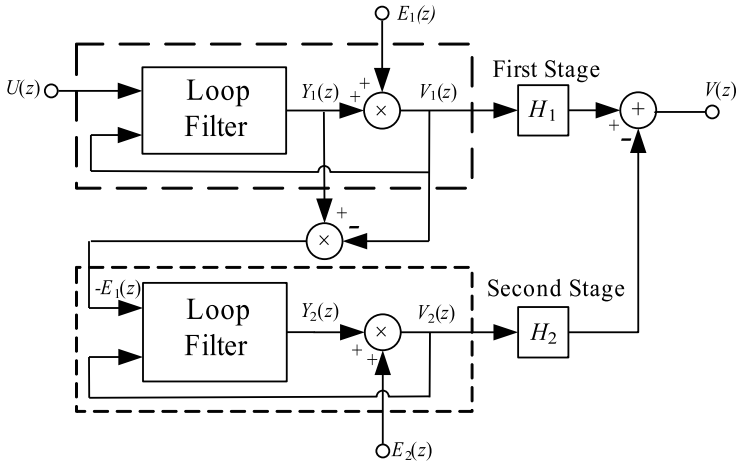


Figure 4.12: Block diagram of a two stage MASH Σ-Δ modulator [R. Schreier 05]

4.2 1-1 DMASH Σ-Δ DPWM

The cascade multi-stage noise-shaping modulator is another approach to further improve the noise-shaping performance. The technique was proposed with no less than two lower-order Σ-Δ modulators and has since been widely applied to Σ-Δ ADC and DAC [R. Schreier 05]. The block diagram of a two stage MASH Σ-Δ modulators is shown in Fig. 4.12. The noise of the cascade circuits is often dominated by the truncation error $E_1(z)$ and the idle-tone from the first stage. Such noise is feed to the second stage to be further processed. The total noise-shaping effect is determined by the total order over the two stages. It greatly reduces the possibility leading to excess noise caused by quantizer overload. It therefore provides a modulator without incurring the danger of instability that is likely to occur in the traditional modulator with the same order.

Referring to Fig. 4.4 and (4.3), the transfer function of each stage is given by

$$\begin{cases} V_1(z) = U(z) + (1 - H_e(z)) \cdot E_1(z) \\ V_2(z) = -E_1(z) + (1 - H_e(z)) \cdot E_2(z) \end{cases} \tag{4.6}$$

So the signal transfer function of each stage is $STF_1 = STF_2 = 1$, and the noise transfer function of each stage is $NTF_1 = NTF_2 = 1 - H_e(z)$. The transfer function of the whole MASH modulator is expressed as

$$\begin{aligned} V(z) &= H_1 \cdot V_1(z) + H_2 \cdot V_2(z) \\ &= H_1 \cdot U(z) + H_1 \cdot (1 - H_e(z)) \cdot E_1(z) + H_2 \cdot (-E_1(z)) + H_2 \cdot (1 - H_e(z)) \cdot E_2(z) \end{aligned} \tag{4.7}$$

In order to eliminate the influence of $-E_1(z)$, the following condition must be satisfied by

$$H_1 \cdot (1 - He) = H_2 \tag{4.8}$$

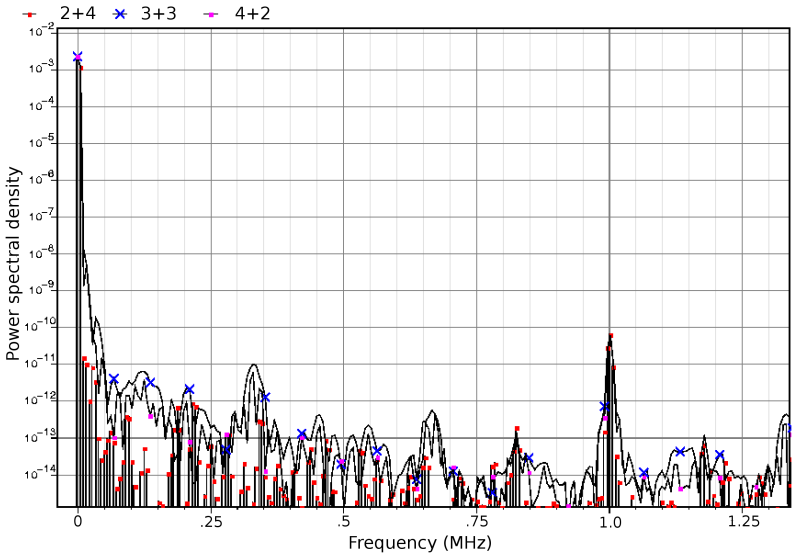


Figure 4.13: Noise-shaping comparison between three 1-1 MASH Σ-Δ modulations with different bit distributions

By simply setting $H_1 = 1$ and $H_2 = 1 - He$, that is to say $H_1 = STF_2$ and $H_2 = NTF_1$, the transfer function can be simplified as

$$V(z) = \frac{H_2}{1 - H_e(z)} U(z) + H_1 \cdot (1 - H_e(z))^2 \cdot E_2(z) = U(z) + (1 - H_e(z))^2 \cdot E_2(z) \quad (4.9)$$

According to (4.9), the MASH modulator is of the second-order by setting $H_e(z) = z^{-1}$ while the fourth-order by setting $He = z^{-1}\left(2 - z^{-1}\right)$. Such a second-order MASH Σ-Δ DPWM is usually expressed as 1-1 MASH Σ-Δ DPWM, and the fourth-order, 2-2 MASH Σ-Δ DPWM.

An 1-1 MASH Σ-Δ DPWM was proposed where both stages contain a first-order internal loop, resulting in a global second-order noise-shaping effect, but preserving the robust stability of the first-order [Guo 09b]. However it still suffers from the idle tone existing in the first-order modulator and particularly the tone's overlapping across the two stages introducing extra low-frequency interference without any attenuation in the baseband [Lukic 07]. The relevant analyses and improvements are given as follows.

Benefiting from the DPWM error-feedback structure as shown in Fig. 4.4, designated modulator does not require a sufficient linear internal DAC compared to a Σ-Δ ADC. Therefore, multi-bit internal-loop can be adopted in the modulator. To avoid a large offset of digit, bit distribution across each stage is an important issue for designers. In a 6-bit Σ-Δ modulator, Fig. 4.13 shows a simulation of the power spectral density (PSD) for 2+4 bits (2-bit MSB in the first-stage and 4-bit MSB in the second-stage, similarly hereafter), 3+3 bits, 4+2 bits, respectively. Here the switching frequency is 1MHz, meanwhile the corner frequency is around 18.6kHz for the power filter. So 2+4 bits modulation structure is selected here as a better choice due to the better noise-shaping performance.

Provided that an artificial binary noise can be cancelled at the MASH Σ-Δ DPWM output, the

Table 4.2: An example of maximum length sequence (MLS) with the shift register length from 5 to 11

Number of registers	MLS length	Feedback taps
5	$2^5 - 1 = 31$	$[4, 3, 0]$
6	$2^6 - 1 = 63$	$[5, 3, 0]$
7	$2^7 - 1 = 127$	$[6, 5, 0]$
8	$2^8 - 1 = 255$	$[7, 6, 0]$
9	$2^9 - 1 = 511$	$[8, 6, 5, 4, 0]$
10	$2^{10} - 1 = 1023$	$[9, 5, 0]$
11	$2^{11} - 1 = 2047$	$[10, 7, 0]$

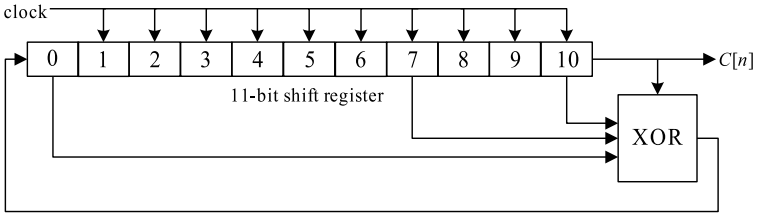


Figure 4.14: Proposed 11-bit PN dither generator

quantizer input behaves like a noise and therefore the quantization noise of MASH is likely white. In order to further decrease the idle-tone effect, a dither generation module, a pseudo-noise (PN) sequence generator, is added to the latter stage of 1-1 MASH Σ-Δ DPWM. The dither module consists of a shift register series and several XOR gates connecting certain shift register outputs. If we denote $c[n]$ the PN dither generator output, we have $c[n] = \pm 1$ so that $c[n] \times c[n] = 1$. An example of the output is shown in Table. 4.2. In this work, an 11-bit PN dither generator is adopted of which the generator polynomial is $\begin{bmatrix} 10 & 7 & 0 \end{bmatrix}$ as shown in Fig. 4.14. Fig. 4.15 shows the block diagram of the proposed 1-1 DMASH DPWM. The overall output signal is represented by

$$V(z) = U(z) + \left(1 - z^{-1}\right)^2 E_2(z) + \frac{1}{L}\left(1 - z^{-1}\right)^2 D(z) \tag{4.10}$$

where $D(z)$ is the dither signal, $E_2(z)$ is the truncation error of the second stage. For this design, $n = 11$, and we set $m_1 = 2$ and $m_2 = 4$. The output spectrum under a DC input of which equivalent duty-cycle equals $0.5 + \dfrac{1}{2^N}$, indicates the idle-tone attenuation effect as shown in Fig.

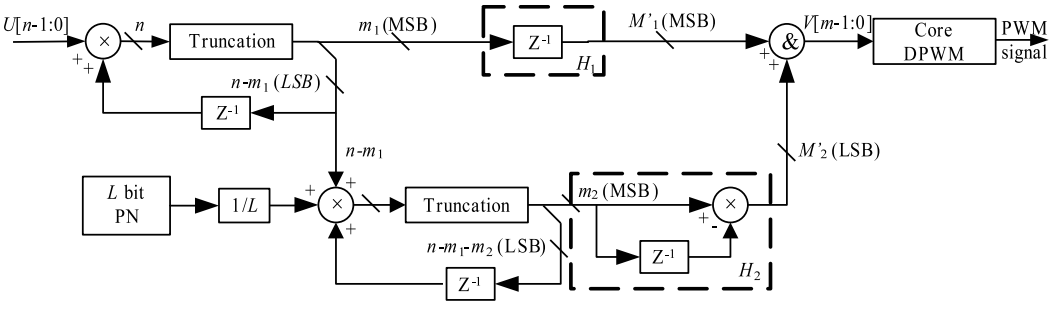
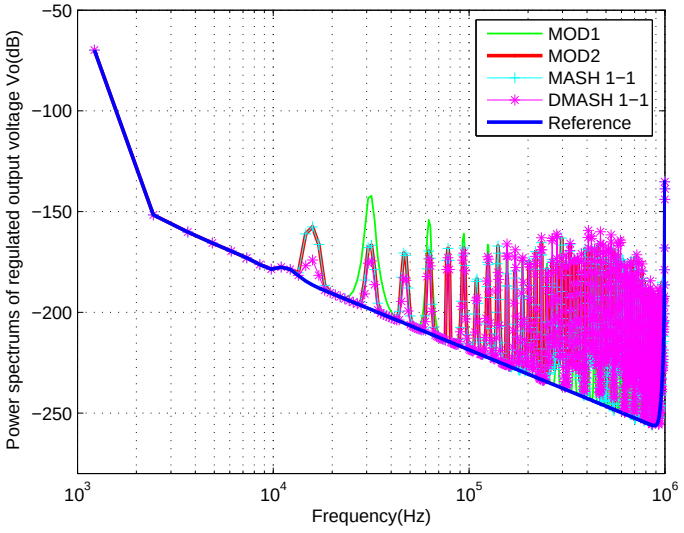
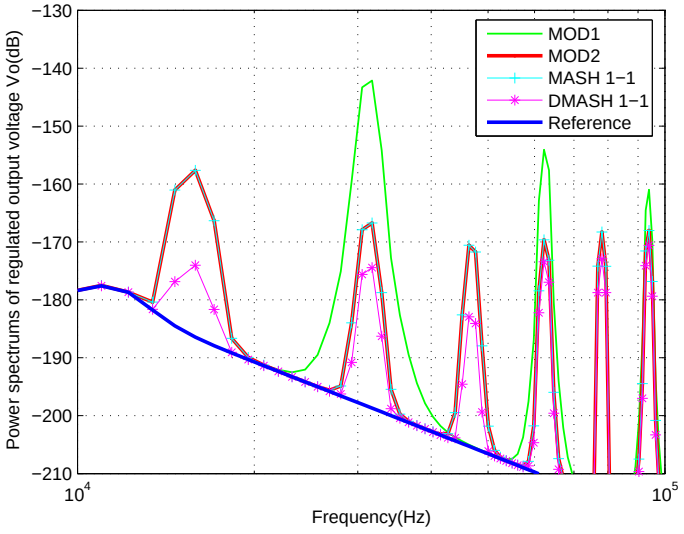


Figure 4.15: Proposed 1-1 DMASH Σ-Δ DPWM

4.16. The simulation results are analyzed by the Welch's method with a Hanning window size of 8192. In Fig. 4.16, the noise power peaks begin to occur after the nature corner frequency of the buck converter, here 10.7kHz. Another power peak at the frequency of the basic idle-tone appears at $\frac{Fs}{2^{N-m_1-m_2}}$ as shown in Fig. 4.16(b). The second-order DPWM has lower idle-tone noise than that of the first-order DPWM [Norsworthy 97, Lukic 07]. However, compared to the traditional second-order DPWM, no noise attenuation appears in 1-1 MASH DPWM [Guo 09b]. The proposed 1-1 DMASH Σ-Δ DPWM in Fig. 4.15 exhibits larger idle-tone attenuation effect than all the referred architectures.



(a)



(b)

Figure 4.16: (a) Power spectrums of output voltage V_o using 1-1 DMASH and existing DPWMs, (b) Power spectrums in the vicinity of the corner frequency

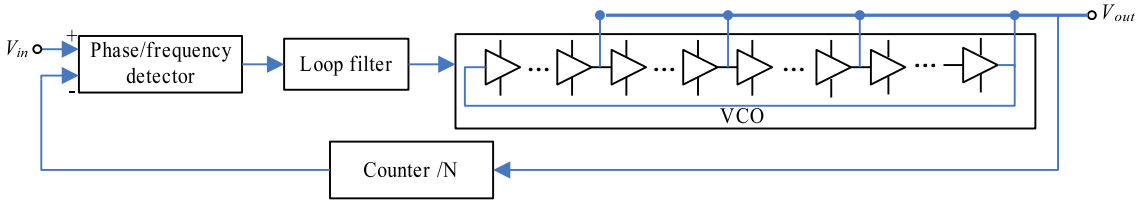


Figure 4.17: Block diagram of a PLL

4.3 Phase-locked Loop for Clock Generation

A well-defined ordering of the power switching events requires an on-chip clock generator devoted to the digital controller. The general PLL is based on the VCO with LC tank. The ring oscillator, composed of a series of delay-cells, is a feasible approach to design a VCO. Although it exists some drawbacks taken into account the PVT variations, it occupies smaller die size than other topologies. Fig. 4.17 shows the basic architecture of a PLL. The phase detector (PD) generates an output voltage proportional to the phase difference between the reference signal, V_{in} and the divided VCO output. The loop filter (LP) is used to extract the average value from the PD output. It drives the VCO to generate the required clock signal. In our design, PD is implemented with an asynchronous sequential logic circuit. LP adopts a second-order RC filter outside the chip.

A typical current-starved delay-cell VCO is shown in Fig. 4.18. Transistors $\mathrm{M_1}$ and $\mathrm{M_2}$ compose a CMOS inverter, and $\mathrm{M_N}$ and $\mathrm{M_P}$ limit the current to the inverter. Normally, current-limit transistors $\mathrm{M_N}$ and $\mathrm{M_P}$ operate in either saturation region or triode region. In order to achieve a larger signal swing and better phase noise, it is better to keep $\mathrm{M_N}$ and $\mathrm{M_P}$ in saturation region. According to the discussion in [Baker 10], the oscillation frequency of the current-starved VCO for N stages is

$$f_{osc} = \frac{I_D}{2NC_{tot}V_{DD}} \tag{4.11}$$

where V_{DD} is the supply voltage, I_D is the current flowing through the current-starved inverter and C_{tot} can be expressed as

$$C_{tot} = \frac{5}{2}C_{ox}\left(W_P L_P + W_N L_N\right) \tag{4.12}$$

where C_{ox} represents the capacitance per unit area between the gate metal and the bulk surface in a transistor. It is a constant, voltage-independent value which depends on geometrical properties, such as gate area and oxide thickness, and on material properties of the oxide. The nominal value of C_{ox} in $AustriaMicrosystemS$ $0.35\mu m$ CMOS process is $4.6 \times 10^{-15} F/\mu m^2$. W_N, L_N, W_P and L_P are the width and length of transistors $\mathrm{M_N}$ and $\mathrm{M_P}$ respectively. If we build each inverter with the minimum transistors size, that is to say C_{tot} equals $1.61 \times 10^{-14} F$, the size of current-limiting transistor $\mathrm{M_N}$ and $\mathrm{M_P}$ can be obtained by (4.11), (4.12) and relevant process parameters. In this design, the target oscillation frequency is 128MHz, and the amount of delay-cells $N = 24$. So the maximum drain current I_D is anticipated to be $163\mu A$. It determines the W/L ratios of $\mathrm{M_N}$ and $\mathrm{M_P}$ that equal 1.4 and 6 respectively. Fig. 4.19 shows the simulation result of the biasing

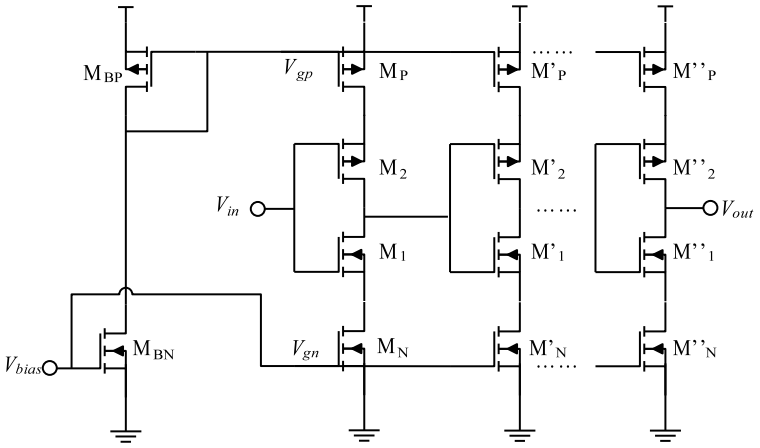


Figure 4.18: Typical current-starved delay-cell with biasing circuit

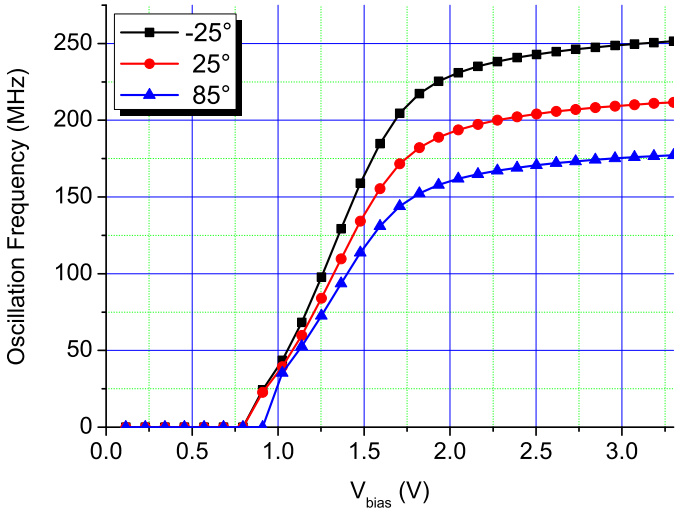


Figure 4.19: Oscillation frequency of the current-starved VCO with the bias voltage

voltage effect on the oscillation frequency under three different temperatures ($-25°$, $25°$ and $85°$). It indicates that the output frequency will keep around 128MHz when the bias voltage comes about 1.5V. Fig. 4.19 also illustrates the temperature impact on the oscillation frequency. With a constant $V_{bias} = 1.45V$, the relation between oscillation frequency and temperature is shown in Fig. 4.20. The influence of the voltage variation can be found in Fig. 4.21. According to aforementioned simulations, the PLL is enough qualified to be a clock generator for the digital controller. As a test prototype devoted to a wide range of clock frequency, this project adopts the classic type to construct the ring oscillator VCO. Experimental results will be given in Chapter 6.

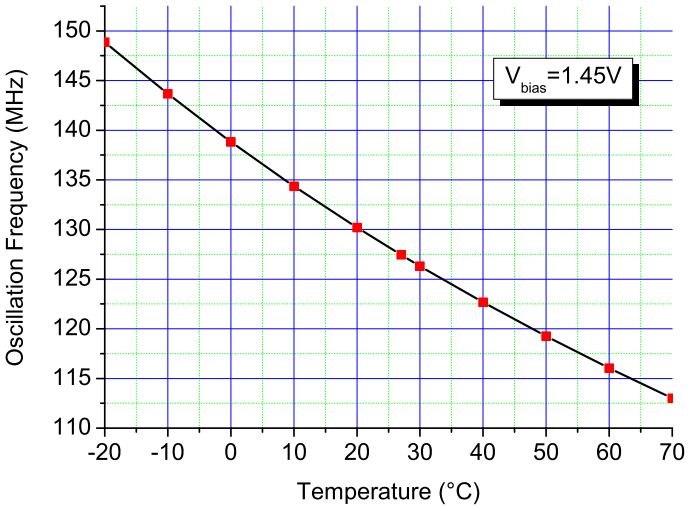


Figure 4.20: Oscillation frequency of the current-starved VCO with the temperature

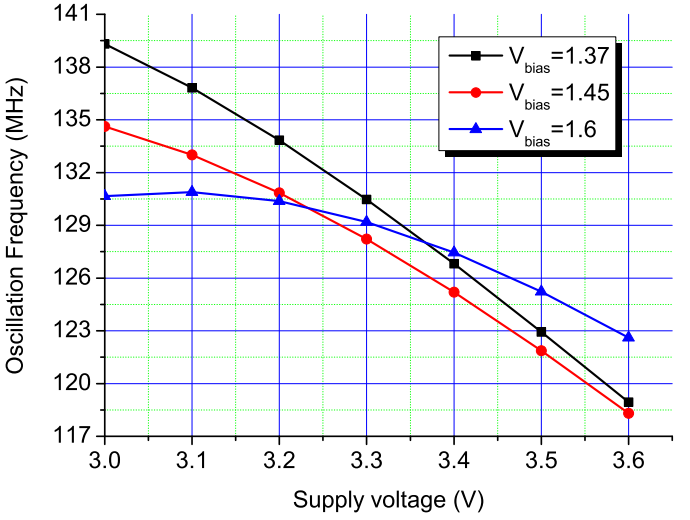


Figure 4.21: Oscillation frequency of the current-starved VCO with the supply voltage

4.4 Summary

This chapter intends to introduce a high efficient DPWM eliminating a complicated architecture. After an analysis of the closed-loop requirement to DPWM, Σ-Δ is proven to be one of the best trade-off. The absence of a solution to the inherent idle-tone therefore becomes a bottleneck. The improved prototype proposed in this chapter is to achieve spur-tone free effect. The 1-1 DMASH DPWM is also proposed to achieve acceptable steady-state and transient-state performances. Experimental results will be given in the next chapter. A global clock generator is also discussed in this chapter to offer a feasible case for the further chip integration. The power losses of the PLL-based clock generator will be given in Chapter 7 along with power losses information for implemented digital controllers.

Chapter 5

Experimental Results in FPGA

This chapter will demonstrate experimental results of the DPWMs and controllers discussed in previous chapters. Firstly, the experimental platforms for the buck and boost converters are introduced along with the basic converter parameter setup. Then experimental results verify the improvements to the DPWM. With the aid of improved DPWM, the experimental results of the DDP controller for the buck converter operating at 1MHz switching frequency are given compared to the PID, RST and SM control-laws. A 4MHz switching frequency case is also demonstrated to show the best performances of the proposed controller. Finally, the performances of the boost converter using PID and SM controllers are provided.

5.1 Testbench for the Buck and Boost Converters

To verify the performances of the proposed DPWMs and controllers, a high switching frequency low-power buck converter is connected to a VIRTEX-II Pro XC2VP30 FPGA with 3.0V input voltage and 1.5V output voltage as shown in Fig. 5.1. The output power of the buck converter prototype ranges from 450mW to 682mW over the switching frequency range. Fig. 5.2 is the experiment platform in which board 1 is the buck converter and board 2 is the ADC. In terms of design specifications, the steady-state and transient-state performances are to be obtained through a closed-loop test. The important system parameters are summarized in Table. 5.1. An open-loop environment can be also implemented on the same platform to test the proposed DPWM.

To verify the performances of the PID and SM controllers, a high switching frequency low-power boost converter is also connected to the Virtex-II Pro XC2VP30 FPGA board with 3V input voltage and 5V output voltage as shown in Fig. 5.3. Fig. 5.4 is the experimental platform in which board 1 is the boost converter and board 2 is the ADC. Basic converter parameters are illustrated

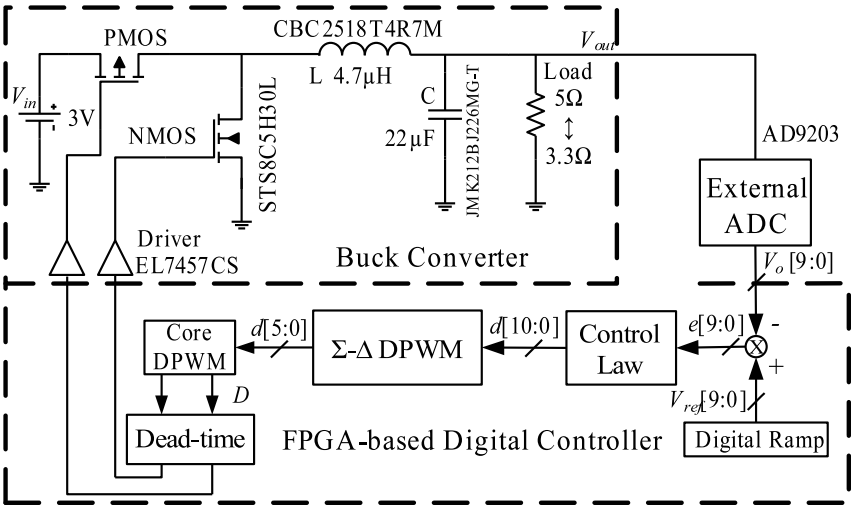
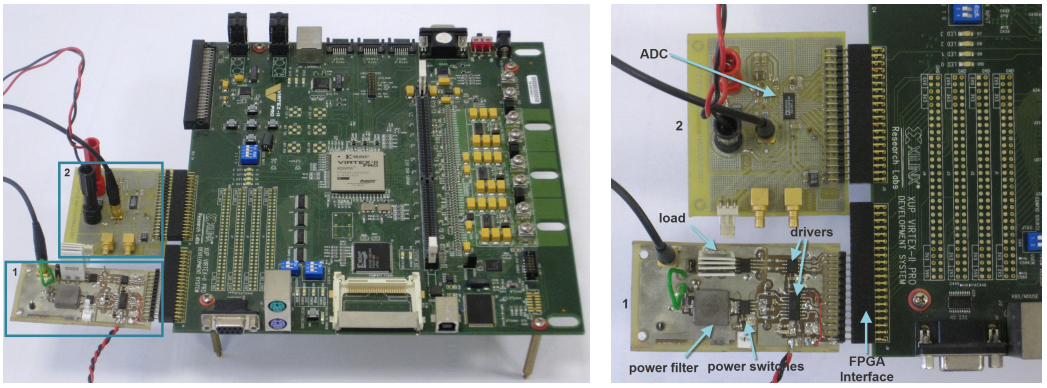


Figure 5.1: Circuit configuration of the FPGA-based digital controller for the buck converter



(a) (b)

Figure 5.2: The FPGA-based experimental platform of the buck converter (a) a system view, (b) a closed view of buck converter and ADC

Table 5.1: Parameters of the digitally controlled buck converter

Buck	Switched mode power converter	Step down
R	Nominal load	5Ω
L	Inductor	$4.7\mu H$
C	Capacitor	$22\mu F$
V_{in}	Input voltage	3.0V
V_o	Output voltage	1.5V
f_s	Switching frequency	4MHz (up to 10MHz)
ADC	Analog to digital converter	10-bit(AD9203)
DPWM	1-1 DMASH DPWM	11-bit
N_{DPWM}	Core DPWM resolution	6-bit
$N_{\Sigma-\Delta}$	Proposed DPWM resolution	5-bit
f_{clk}	DPWM counter frequency	64MHz

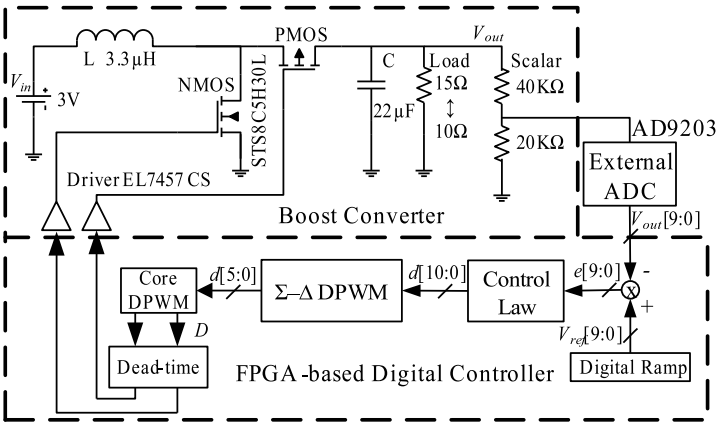
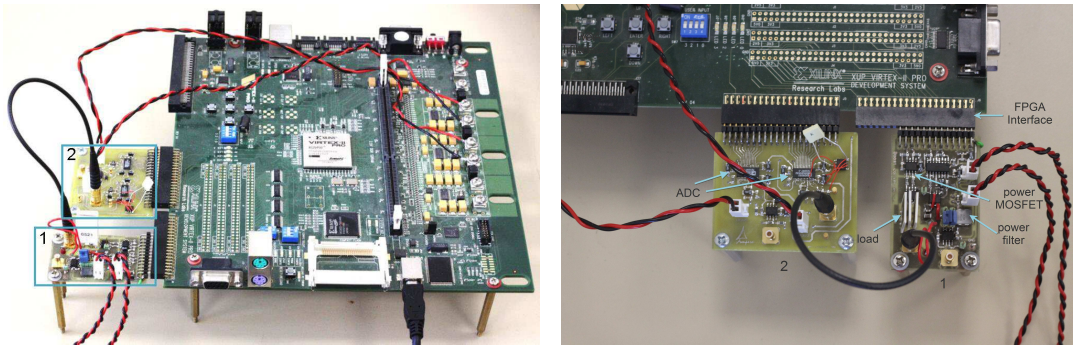


Figure 5.3: Circuit configuration of the FPGA-based digital controller for the boost converter



(a) (b)

Figure 5.4: The FPGA-based experimental platform for the boost converter (a) a system view, (b) a closed view of boost converter and ADCs

in Table. 5.2.

5.2 Test of DPWM

Firstly, an open-loop buck converter is used to test the performances of proposed 1-1 DMASH Σ-Δ DPWM.

Steady-state test: A 6-bit counter-comparator based DPWM, also known as the core DPWM embedded within the 1-1 DMASH Σ-Δ DPWM, is realized as a reference. Fig. 5.5 shows the LC-filtered output of the duty-cycle for a generated ramp signal from 2047 to 0 that is also the duty-cycle sweep range for an 11-bit DPWM. An obvious observation from the results of the open-loop DPWM test is that the slope of the proposed DPWM is smoother than that of the core DPWM because of the Σ-Δ noise shaping effect. Referring to the Σ-Δ attribute, it conforms to the noise shaping principal that also leads to the increase in the effective resolution. Inherent non-linear characteristics will introduce errors added to the control-law error. In practice, it is always compelling to come to a trade-off between the hardware complexity and the acceptable linearity. Integral nonlinearity (INL) and differential nonlinearity (DNL) are two effective parameters with

Table 5.2: Parameters of the digitally controlled boost converter

Boost	Switched mode power converter	Step up
R	Nominal load	15 Ω
L	Inductor	3.3 μH
C	Capacitor	22 μF
V_{in}	Input voltage	3.0 V
V_o	Output voltage	5.0 V
f_s	Switching frequency	1 MHz (up to 10 MHz)
ADC	Analog to digital converter	10-bit (AD9203)
DPWM	1-1 DMASH DPWM	11-bit
N_{DPWM}	Core DPWM resolution	6-bit
$N_{\Sigma-\Delta}$	Proposed DPWM resolution	5-bit
f_{clk}	DPWM counter frequency	64 MHz

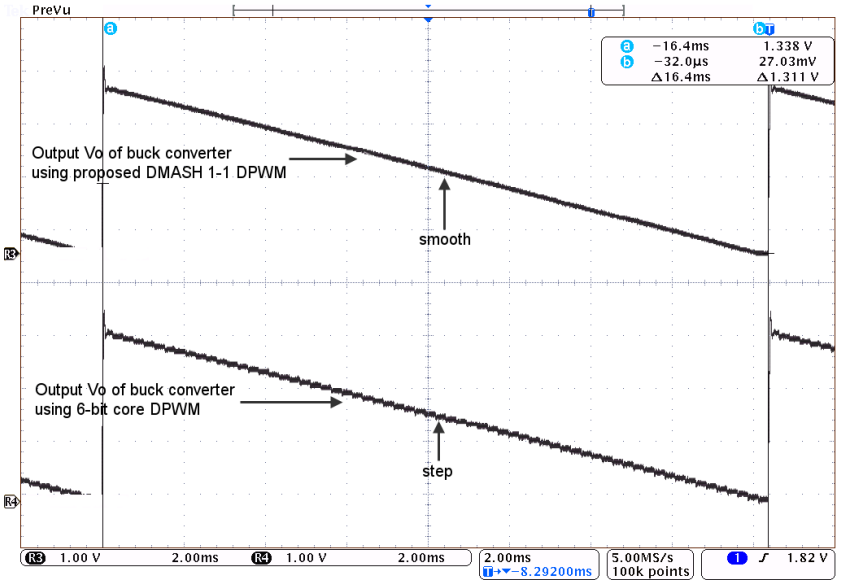


Figure 5.5: Regulated output voltage V_o of the experimental converter for a digital ramp from 2047 to 0

respect to the conversion accuracy that are usually used in ADC and DAC. DPWM can also adopt the two performance indexes to estimate the linearity. The dynamic performances of DPWM can exhibit the behavior under transient-state. Identical control-law with different DPWMs will lead to different closed-loop performances related to the stability issue. The INL and the DNL are measured with a 61.44Hz full-scale ramp input. At 61.44kS/s, 60011 sample points are collected. The measured DNL and INL profiles are shown in Fig. 5.6. The DNL is within ±0.62LSB and the INL curve never exceeds +0.55/-0.83LSB over the 3V dynamic range. The experimental results and linearity analyses guarantee an absolute monotonicity for the proposed DPWM, and an acceptable derivation of DPWM transfer characteristic compared to ideal one.

Transient-state test: Fig. 5.7 shows an example of the dynamic behavioral characteristic in which there is a step of equivalent input bins from 2047 to 0. The convergence time for the proposed 1-1 DMASH DPWM is 204μs that is significantly smaller than that of the first-order Σ-Δ DPWM (383μs).

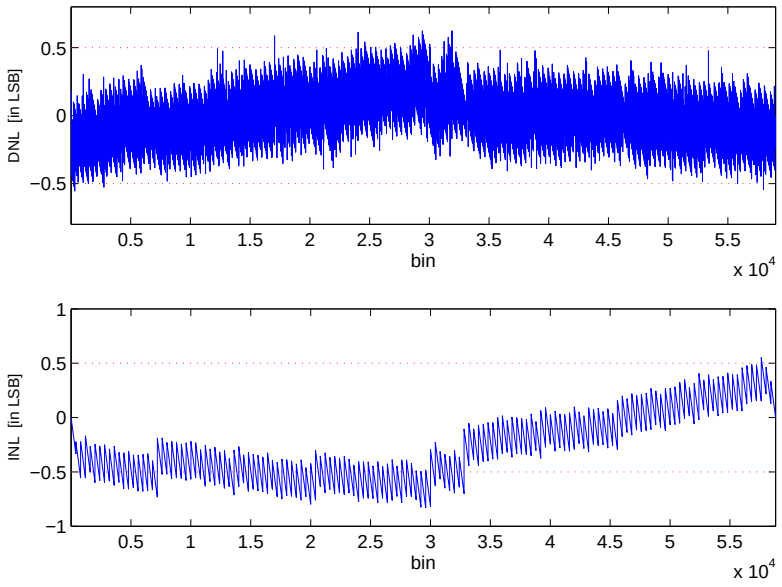


Figure 5.6: Measured DNL and INL of the proposed 1-1 DMASH DPWM

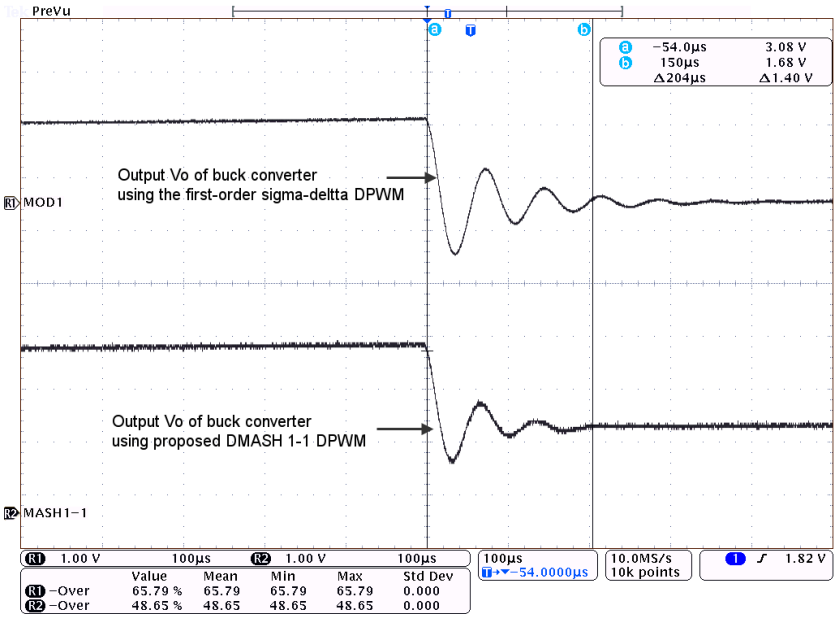


Figure 5.7: Comparison of the regulated output voltage V_o in transient state using the first order Σ-Δ DPWM and the proposed 1-1 DMASH DPWM

Table 5.3: A comparison to reviewed controllers with respect to hardware resources

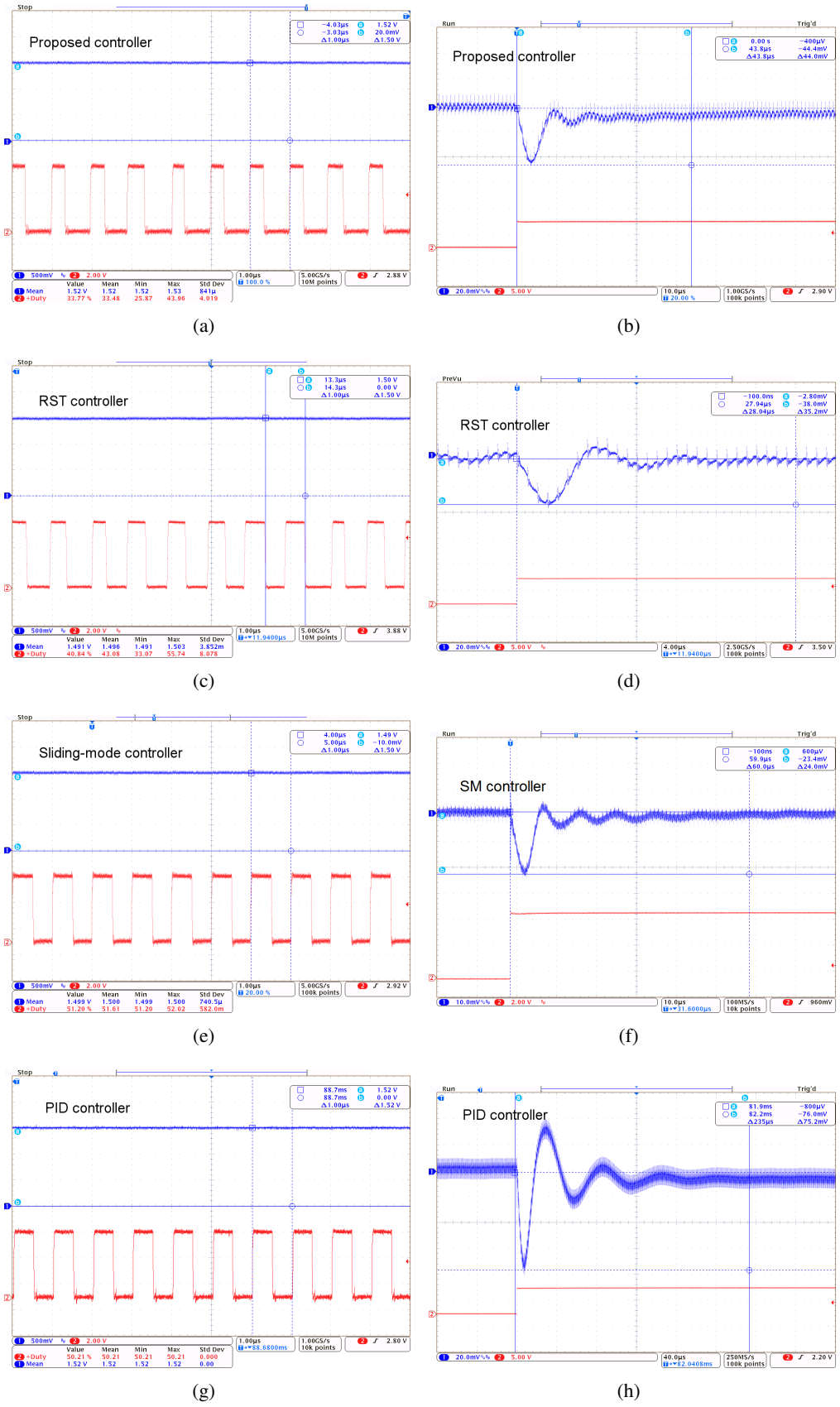
Controller type	Hardware multiplier	Hardware adder	Number of Tunable parameters	Total equivalent gates
DDP controller	5	7	3	6997
RST controller	9	8	9	10569
SM controller	3	3	2+2	3046
PID controller	5	4	5	5059

According to the experimental results, the proposed 1-1 DMASH DPWM is a good candidate for the digital controller dedicated to high switching frequency.

5.3 Test of DDP Controller

As introduced in Section 5.1, a buck converter is built and controlled by the FPGA-based digital controller in order to verify the closed-loop operation. Due to frequency limits of the discrete buck architecture, tests are currently performed up to 4MHz, but can be possibly extended to 10MHz with an integrated controller IC. Two second-order Σ-Δ DPWMs are required to map the two control variables to a PWM signal. The PWM calculations based on T_1 and τ_1 in one period are performed simultaneously to avoid unwanted signal competition.

The dead-beat controller taken as a comparison in Section 3.7 cannot perform at so high a switching frequency due to the absence of a current sensor. So experimental results are presented in Fig. 5.8 including the DDP, PID, RST, and SM controllers. Unlike the predictive dead-beat controller, the four controllers can operate without the aid of a current sensor. Fig. 5.8(a), (c), (e) and (g) show the high-side PWM signals in the steady-state respectively. Fig. 5.8(b), (d), (f) and (h) show the transient-state output voltage under a load change from 0.3A to 0.45A (5Ω to 3.3Ω). Comparisons of occupied hardware resources and dynamic performances of the four controllers are summarized in Table. 5.3 and 5.4. According to the experimental results, the SM controller suffers from a steady-state error without the aid of double integral sliding surface [Tan 08b] and the dynamic performances deteriorate. Double integral method requires inductor current information that does not satisfy the current sensorless specification. So it is not a good candidate for a digital controller compatible with high switching frequency. Linear PID controller demonstrates a settling time over 200 μs that is the longest convergence time compared to other implemented controllers. Both the proposed DDP and RST controllers exhibit better dynamic performances (settling time less than 50 μs). Moreover, the proposed DDP controller saves more than 30$\%$ hardware resources compared to the RST controller. It should be mentioned that PID and RST controllers can only support a switching frequency up to 1 MHz due to the voltage-mode control attributes and the complexity of the control algorithm. So for a high switching frequency buck converter, the DDP controller is a better trade-off taking into account the hardware implementation, dynamic performances and power consumption.

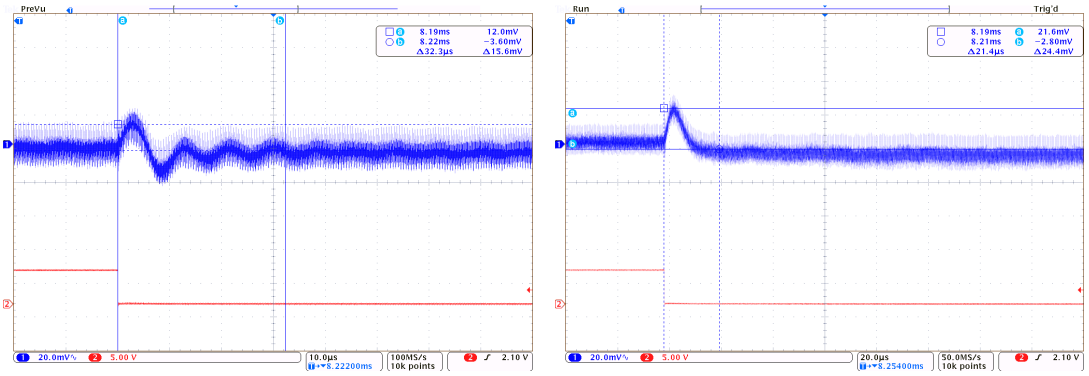


(a) (b) (c) (d) (e) (f) (g) (h)

Figure 5.8: Transient output voltages at 1MHz switching frequency during load change from 0.3A to 0.45A (R: from 5Ω to 3.3Ω) as well as the steady-states using (a) DDP controller in steady-state, (b) DDP controller in transient-state, (c) RST controller in steady-state, (d) RST controller in transient-state, (e) SM controller in steady-state, (f) SM controller in transient-state, (g) PID controller in steady-state, (h) PID controller in transient-state

Table 5.4: A comparison to reviewed controllers operating at 1MHz switching frequency with respect to dynamic performances

Controller type	Settling time 0.3A →0.45A (μs)	Settling time 0.45A→0.3A (μs)	Negative overshoot (mV)	Positive overshoot (mV)
DDP controller	43.8	44.0	44.0	17.4
RST controller	38.5	42.2	35.2	22.4
SM controller	60.0	82.7	24.0	48.4
PID controller	235.0	232.0	75.2	40.4



(a) (b)

Figure 5.9: Transient output voltage during load change from 0.45A to 0.3A (R: from 3.3Ω to 5Ω) using DDP controller (a) operating at 2MHz switching frequency, (b) operating at 4MHz switching frequency

Fig. 5.9 shows the dynamic responses under load current change from 0.45A to 0.3A. With the increase of the switching frequency, the DDP controller enables faster response and results in relatively lower overshoot in the output voltage. Detailed results related to the dynamic performances of the DDP controller operating at different switching frequencies are reported in Table. 5.5.

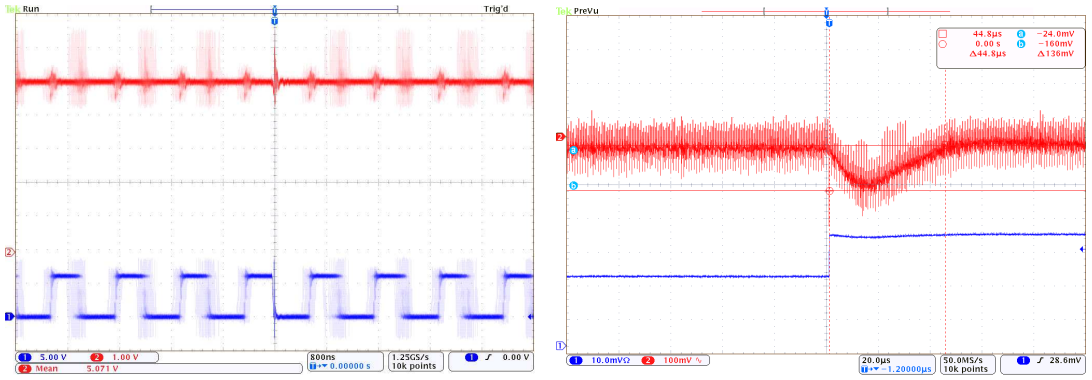
According to the experimental results, the DDP controller achieves a fixed switching frequency with better steady-state and transient-state performances. The hardware implementation is quite simple: only few memories, multipliers and adders in FPGA/ASIC are needed. The experimental results validate the functionality and performances of the DDP controller and confirm the feasibility of an ASIC.

5.4 Test of PID and SM Controllers for the Boost Converter

In this section, tests are performed to verify the performances of the PID and SM controllers for the boost converter. Fig. 5.10(a) and 5.11(a) show the output voltage and the corresponding high-side PWM signal for the PID and SM controllers respectively under steady-state operation at 1MHz. They both exhibit sufficient stability in the output. Fig. 5.10(b) and 5.11(b) show the transient output response when the load varies from 15Ω to 10Ω. The SM controller responses

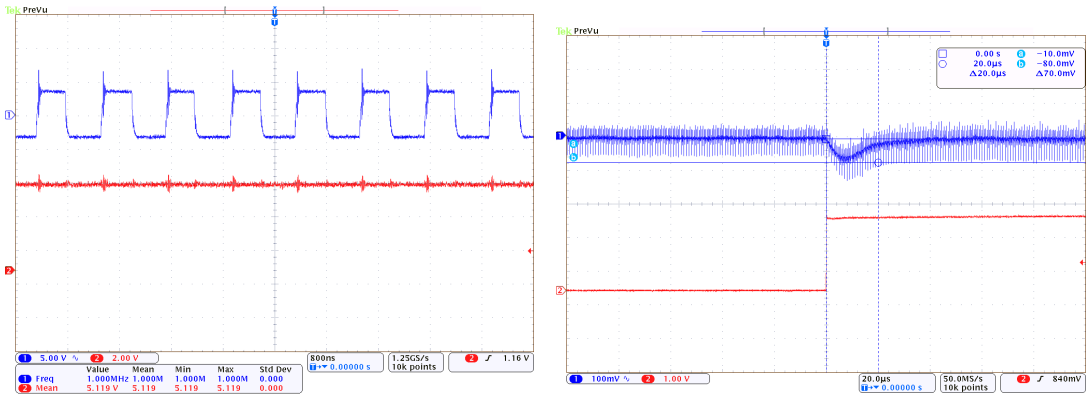
Table 5.5: Dynamic performances of the DDP controller under a load perturbation between 0.3A and 0.45A

Switching frequency	Settling Positive perturbation (μs)	Time Negative perturbation (μs)	Negative overshoot (mV)	Positive overshoot (mV)
1MHz	43.8	44.0	44.0	17.4
2MHz	31.5	32.3	35.0	15.6
4MHz	23.8	21.4	30.7	24.4



(a) (b)

Figure 5.10: PID controller: (a) steady-state operation at 1MHz, (b) load change from 0.33A to 0.5A (R: from 15Ω to 10Ω)



(a) (b)

Figure 5.11: SM controller: (a) steady-state operation at 1MHz, (b) load change from 0.33A to 0.5A (R: from 15Ω to 10Ω)

Table 5.6: Performance summary of SM and PID controllers for the boost converter

Load change	Performance index	SM controller	PID controller
15Ω	Recovery time	40μs	45μs
to	Undershoot	70mV	136mV
10Ω	Output ripple	30mV	30mV
10Ω	Recovery time	42μs	102μs
to	Overshoot	90mV	92mV
15Ω	Output ripple	30mV	30mV

faster than the PID controller in transient state. The dynamic response of SM controller is very fast ($<$40 μs) and the negative overshoot voltage is also very small ($<$70mV) which is less than 1.4% of the specified output voltage (5V). The performances of the two controllers are summarized in Table. 5.6. Nevertheless, this test executes a conservative load variation exclusively in order to guarantee the CCM. In effect, a load variation from 45Ω to 10Ω is available in a serious condition test. Moreover as an improvement, it is possible to add an observer to obtain the inductor current value which helps to further ameliorate the control performance.

5.5 Summary

This chapter represents the experimental results of the proposed DPWMs and controllers in FPGA. The results from FPGA can validate the performances discussed in previous chapters. The FPGA board acts as a prototyping emulators prior to ASIC integration. With the aid of ASIC, the controller will probably achieve better performances in advance CMOS technologies. We also anticipate to obtain important information from ASIC, such as the power consumption. In the following chapters, we will focus on two issues, ASIC integration and evaluation of power consumption.

Chapter 6

ASIC Integration

ASIC is a type of integrated circuit customized for a special purpose. With the development of CMOS technology, the integration density gradually increases, meanwhile, the cost of digital controller dedicated to the DC-DC SMPS becomes not expensive. Our purpose is to obtain the control performance and the power efficiency of the digital controller compared to analog counterpart.

From the system perspective, the viability of a digital IC depends on many conflicting factors in terms of operating frequency, power consumption and system flexibility. There is no doubt that the full custom design is a conceivable approach that can achieve high cost-efficiency. However it normally brings about more design and layout work that may greatly delay TTM. So far, this approach is still in use specially in some performance-aware parts, such as the arithmetic logic unit (ALU) in a microprocessor.

Apart from that, cell-based approach is a common methodology for digital IC design. It is also known as top-down design methodology that shortens and automates the design flow. The necessary elements in this approach is the standard cell contained in a process library provided by a specific foundry. A typical library usually contains some basic logic cells and complex functional cells, such as MUX, comparator and full adder. Normally, each cell has three types so as to assist the digital IC design flow. As the behavior-level model, a specific language, such as VHDL or verilog HDL, offers a compilable gate-level model to describe the logic functions. A physical model is usually assembled as a layout view. Cells are placed in rows that construct the designated gate-level netlist. Another important model contains the timing information to evaluate the timing sequence during gate-level synthesis and post-layout simulation. With the aid of a standard cell library, the designer can begin the design using a HDL and can demonstrate the simulation results compared to the design specifications. All above tasks can be categoried into the front-end design. The purpose of the front-end design concentrates within the high effective code that maps to less

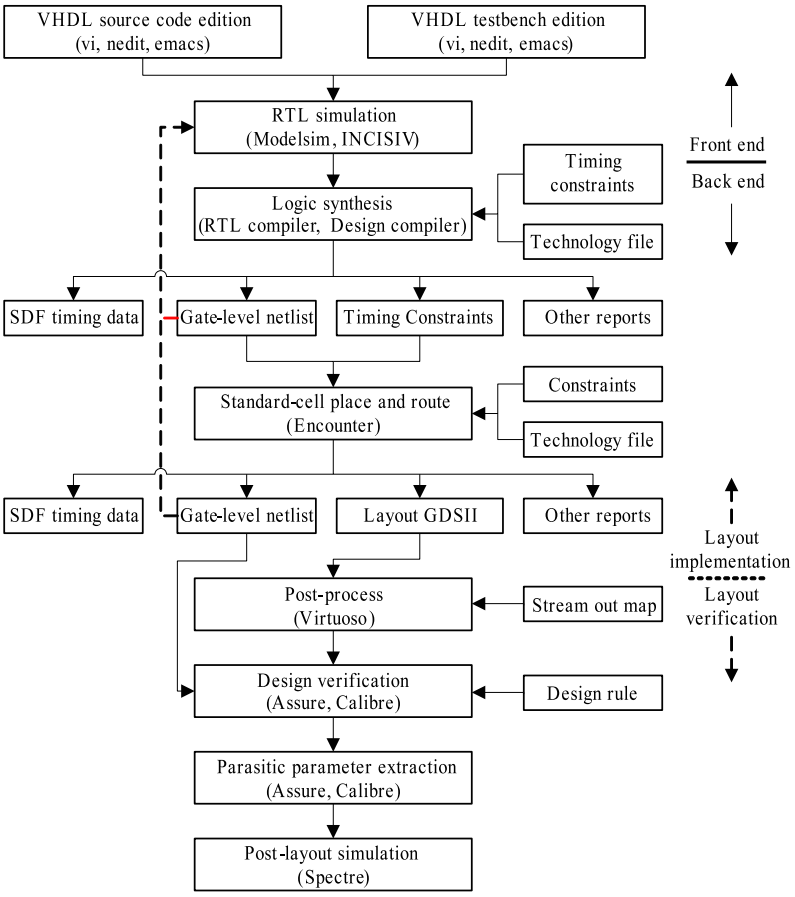


Figure 6.1: Common digital IC design flow

hardware resources and acceptable timing sequence.

6.1 Design Flow

Fig. 6.1 shows a common digital IC design flow as well as the general industry design software. We will discuss each design step in the back-end and provide practical design tips.

As a member of electronic design automation (EDA) tools, gate-level synthesis software provides an automatic translation from the RTL HDL code to the gate-level netlist using the standard cell library. If the RTL description satisfies design specifications, the HDL code can be then synthesized into a gate-level netlist. This task is regarded as the first step over the back-end design. As shown in Fig. 6.1, the timing constraints and library files are necessary in order to perform the synthesis. The library files offer the design reference as mentioned above. The constraints are critical to synthesis because they define the anticipated performances of the sequential parts along with the design rules in terms of fanout and capacitance limits, operating conditions and wire-load models. It is also important to interpret the synthesis reports, such as area, power and timing report, so as to guarantee an accurate mapping satisfying the design specifications and keeping the original behavior as in the RTL code. We can obtain the standard delay format (SDF) after syn-

thesis to perform a post-synthesis simulation so as to exhibit more accurate representation than the RTL simulation. The gate-level netlist and the standard design constraints are two necessary files for the following layout step.

The second design step over the back-end includes placing and routing the standard cells strictly based on the gate-level netlist and the generated design constraints. Since it requires complex procedures to generate the digital layout, this section only refers to important steps. Floorplanning a chip or block is an important task during physical design in which the location, size, and shape of soft modules, and the placement of hard macros are determined. The power plan should be done after the floorplan in order to construct a sufficient current flow path. It includes the plan of rings and strips as well as the connections of each modules and power lines. Then the standard cells can be placed within the framework created during floorplan and power plan. After the determination of each modules and standard cells, the clock tree synthesis will create a routing guide used for further routing to improve the timing sequence. Then the final step synthesizes all generated reports so as to create the final layout that satisfies the logical and sequential requirements. After each step, timing verification is normally necessary to ensure that the generated netlist meets the timing specifications. The final result is then delivered to do the design rule check (DRC) utility and other post-layout verifications.

The previous step has already created the layout view to tape-out. The purpose of the third step activates DRC and the extraction of parasitic parameters for post-layout simulation. Firstly, DRC is performed by comparing the whole layout with design rules from the foundry to ensure no violation. Then a layout versus schematic (LVS) is done so that the layout and schematic have a consistence. After that, the parasitic parameter extraction is performed to generate a netlist including not only the logic information as the gate-level netlist, but also the parasitic parameter information. Finally the post-layout simulation is performed to re-verify the logic and timing consistence. It comes to be regarded as the best proximity compared to the experimental results.

The aforementioned three steps make of a general digital IC design flow. Details are discussed in [Lee 00, Rabaey 03] and relevant EDA software manuals. An example of RTL to layout design flow is illustrated in Appendix D.

6.2 VHDL-AMS Based Testbench and the Parameter Read-in Module

6.2.1 VHDL-AMS Based Testbench

VHDL-AMS is a feasible description language to construct a mixed-signal system so as to evaluate the target system behaviors by the behavioral simulation. This is also the best way to estimate the performances of different control-laws before the implementation in FPGA or ASIC. VHDL-AMS can be applied to describe the power converter and ADC both of which are mixed-signal systems. The controller including control-laws and DPWM has been added to the system during each design step (RTL, gate-level and gate-level with back-annotated layout parasitic parameters). Compared to Matlab simulations, VHDL-AMS simulation is proven to be closer to

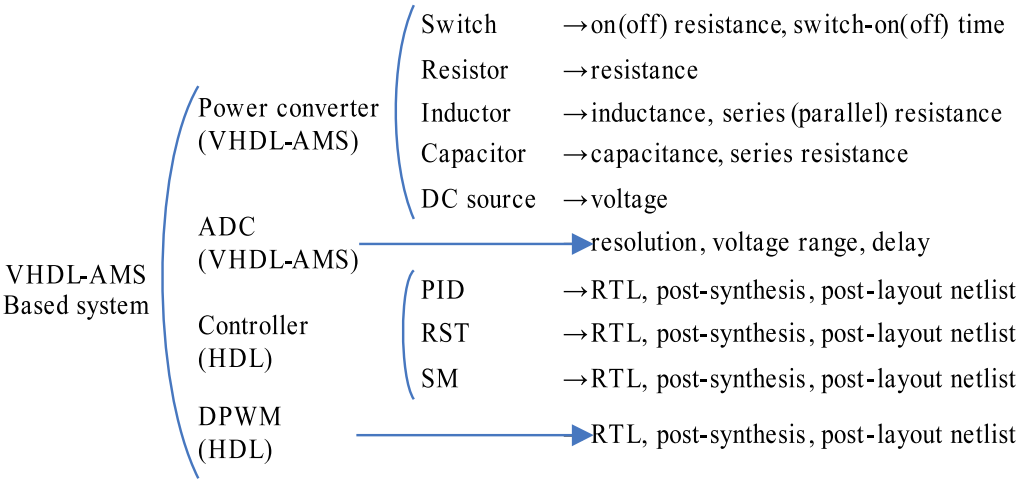


Figure 6.2: Organization of a digitally controlled DC-DC power converter using VHDL-AMS

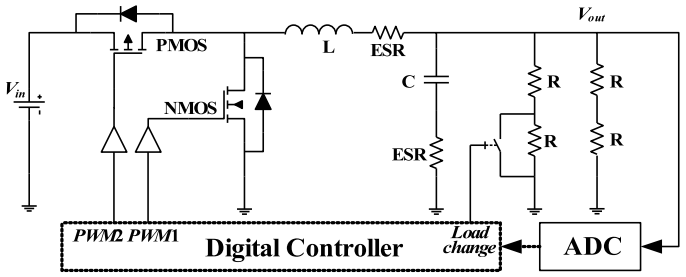


Figure 6.3: Buck converter testbench using VHDL-AMS

the experimental results. Fig. 6.2 describes an example of the digitally controlled DC-DC power converter using VHDL-AMS.

In this section, a buck converter is used as an example to illustrate the configuration to the VHDL-AMS simulation. Fig. 6.3 indicates the structure of the buck converter testbench. It is important to notice that the two power MOSFET models must include the built-in diode, otherwise DCM will occur so that greatly affects the simulation reliability. Table. 6.1 illustrates a summary of device parameters. With the aid of VHDL-AMS based system, it is easy to analyze the proposed parameter read-in module.

6.2.2 Parameter Read-in Module

Parameter read-in module is proposed to alleviate the requirement for the large pin amount in a chip. Using the VHDL-AMS based simulation platform, this section will introduce the design of the parameter read-in module. An example of SM controller is demonstrated here to verify the feasibility of the target controller with tunable parameters fed in by a serial interface. The SM controllers for the buck and boost converters are also included in the second chip. SMC1 denotes the SM controller for the buck converter, as well as SMC2 for the boost converter. The block diagram of the proposed parameter read-in module is shown in Fig. 6.4.

Table 6.1: A parameter summary for the buck converter and ADC

PMOS	Rise time	25ns
(STS8C5H30L)	Fall time	125ns
	$R_{DS(on)}$	$45m\Omega$
NMOS	Rise time	12ns
(STS8C5H30L)	Fall time	23ns
	$R_{DS(on)}$	$18m\Omega$
L	Inductance	$4.7\mu H$
(CBC2518T4R7M)	ESR	0.26Ω
C	Capacitance	$22\mu F$
(JMK212BJ226MG-T)	ESR	$3m\Omega$
R	Resistance	5Ω
ADC (AD9203)	Type:SAR	10-bit

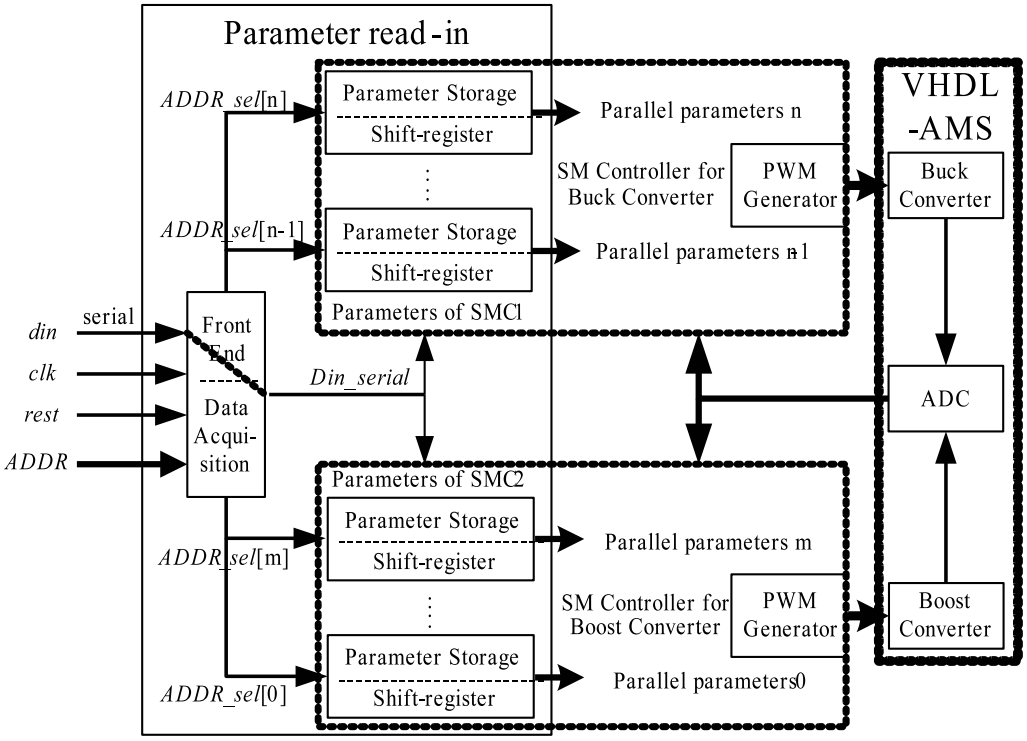


Figure 6.4: Block diagram of the parameter read-in module

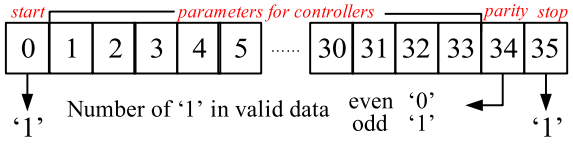


Figure 6.5: Serial data receiver for dedicated controller

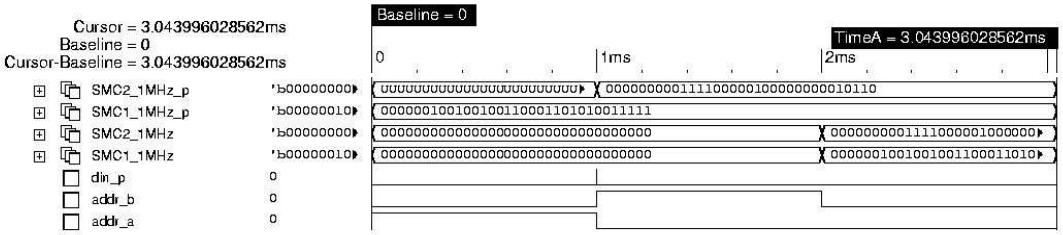


Figure 6.6: Timing sequence of the parameter read-in module

In order to implement the programmable parameters that introduce an adjustable control effect, a 36-bit shift-register is defined as a synchronous serial data receiver based on the implemented control-laws. Each parameter expresses a 33-bit signed binary. Fig. 6.5 shows the distribution of serial bit embedded in shift register. The parameter read-in module has its own synchronous clock and reset signal. The $ADDR$ signal can be modified easily to satisfy the complementary controllers. There are two phases to implement a full control. The first phase is to write parameters into the controller. Then the second phase is to execute the control algorithm so as to manipulate the DC-DC converter. The advantage of an integration the serial-to-parallel module into dedicated controller is its cancellation of the data-path between shift-register and the control-law.

It is worthwhile to note that the valid data sequence is in a reverse order of original parameters, nevertheless the parity check bit remains the same value. The default values of start bit and stop bit are both '1'. Taking the SMC1 as an example, the first control parameter is

$$(000000100100100110001101010011111)$$

According to the serial to parallel rule, the input serial digits should be

$$(111111001010110001100100100100000001)$$

Fig. 6.6 shows the timing sequence of the parameter read-in module during the first phase. In the period of valid $ADDR$ enable signal, serial data from din_p in a serial format is written into a shift-register and then is stored for the digital controller. Fig. 6.7 shows the timing details of the din_p signal.

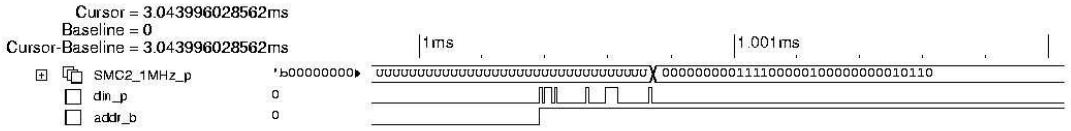


Figure 6.7: Timing details of the parameter read-in module

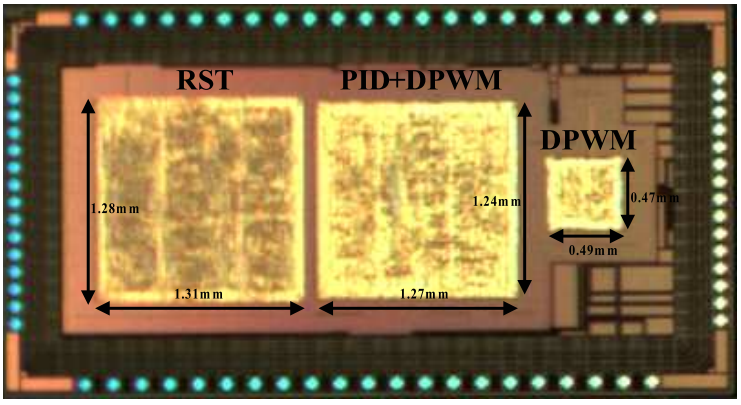


Figure 6.8: Die micrograph of the first chip

6.3 Realized ICs

Two ASICs have been designed and taped-out to evaluate the performance and efficiency of aforementioned digital controllers. We have implemented three control-laws into the chips including PID, RST and SM controllers. Some necessary peripheral circuits are also integrated such as DPWM, PLL and parameter read-in module. Next, a general description is given in term of design specifications, test platform and experimental results. Evaluations associated with power losses from the digital controller will be discussed in Chapter 7.

6.3.1 The First Chip and Testbench

This ASIC is the test chip that implements digital control strategies for the buck converter using a top management finite-state-machine (FSM) and dedicated control-laws depending on the converter state. The flexibility is achieved by means of PID and RST control-laws integration that responses under load change. With the aid of the digital clock manager existing in FPGA, a DPWM based on second-order idle-tone free Σ-Δ modulator is integrated into the chip independently. It has been also embedded into the PID controller to verify the closed-loop performances. The chip features are summarized as

– Robust RST controller achieving good dynamic performances;
– PID controller achieving stable response using less hardware resource;
– Idle-tone free Σ-Δ DPWM reducing required system clock frequency.

The above features are fabricated in $AustriaMicrosystemS$ $0.35\mu m$ CMOS process. Fig. 6.8 is the die micrograph. The whole chip occupies $4.58mm \times 2.42mm$ in which the RST con-

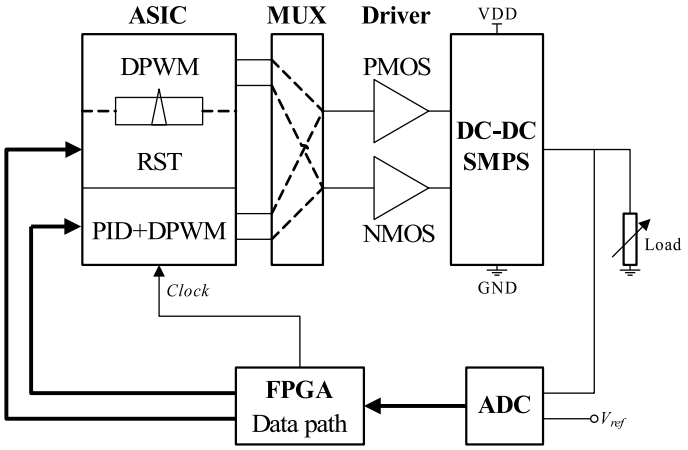


Figure 6.9: Block diagram of the first chip testbench

troller takes $1.28mm \times 1.31mm$, the PID controller including embedded DPWM takes $1.24mm \times 1.27mm$, while the stand-alone DPWM takes $0.47mm \times 0.49mm$. The package type is CLCC84.

An FPGA based testbench as shown in Fig. 6.9 is built to evaluate the performances and efficiency. We have designed an FPGA board (Xilinx Spartan XC3S500E) as the mother board. The ASIC test board is connected to the FPGA motherboard from which the test vectors can be conveyed directly to the ASIC. A buck converter is added to the circuit along with an ADC and the test target ASIC that construct a closed-loop. An FPGA controlled MUX is integrated to select the operation-mode as follows

- Stand-alone RST control performances;
- Stand-alone PID control performances;
- Improved power-aware tri-mode control performances.

In the test for RST control performances, RST control-law must work together with DPWM. So the FPGA should not only select the ASIC operation mode, but also provide a data-path between ADC and RST controller. In the test for PID control performances, the FPGA offers the control signal to MUX and provides a data-path.

As shown in Fig. 6.10, the test platform includes the buck converter controlled by the implemented ASIC and the FPGA motherboard. It enables the mode arbitrary logic for the improved power-aware tri-mode controller as well as provides test vectors, system clocks and control signals. The testbench schematics are shown in Appendix B.2 in detail. Table. 6.2 summarizes referred components dedicated to the testbench. The design specifications are illustrated in Table. 6.3.

6.3.2 The Second Chip and Testbench

The second ASIC consists of control strategies not only for the buck converter but also for the boost converter. The PID and SM control-laws are devoted to the two converters. The proposed 1-1 DMASH Σ-Δ modulator discussed in Chapter 4 is embedded along with all implemented controllers to alleviate the requirement for ultra-high clock frequency. We also integrated an on-chip PLL module discussed in Chapter 4 to provide a high frequency clock with four phase shifts. Also

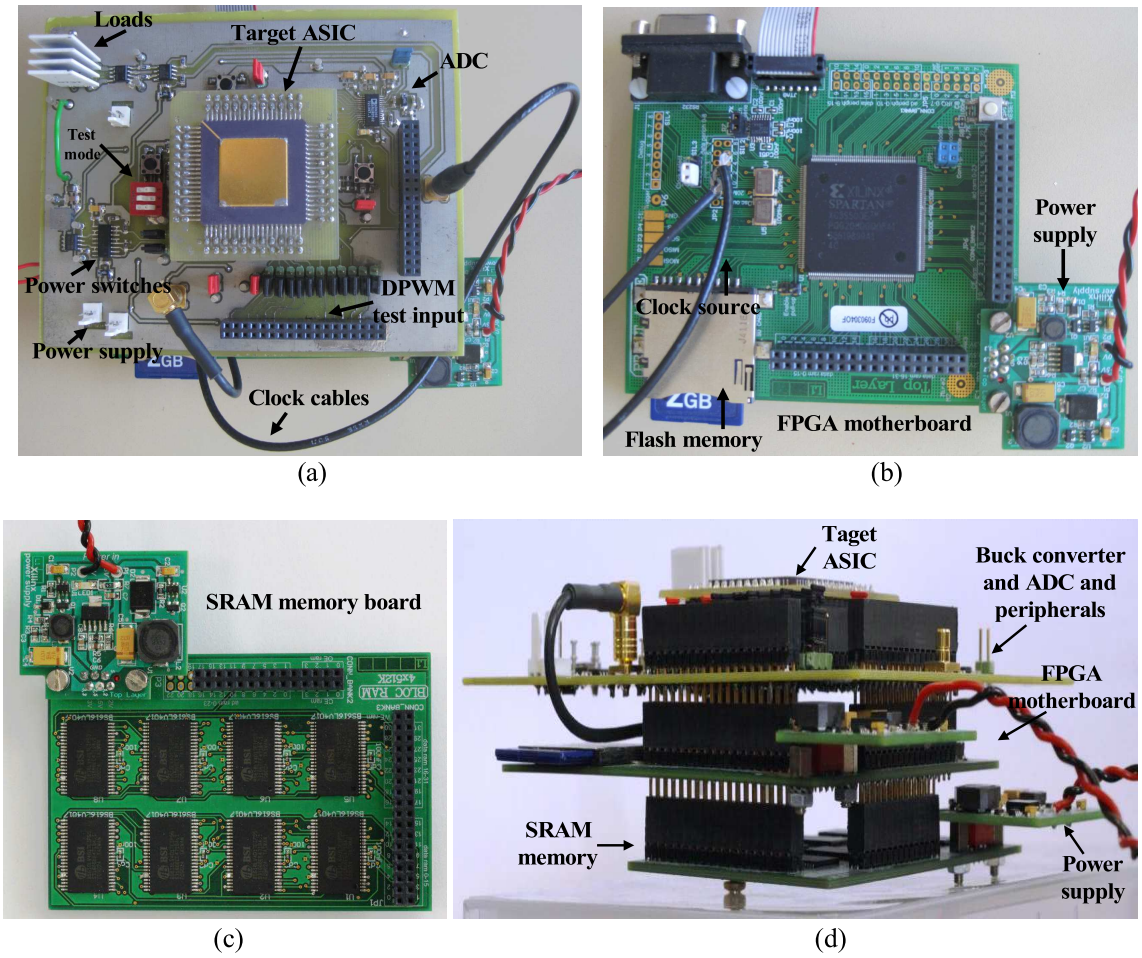


Figure 6.10: Experimental test platform for the first chip (a) buck converter controlled by implemented ASIC, (b) FPGA motherboard, (c) SRAM memory board, (d) a lateral view

Table 6.2: Referred devices and the parameters in the testbench

R	$TYCO$ resistor	5Ω and 10Ω (6Ω Nominal)
L	$TAIYOYUDEN$ inductor	CBC2518T4R7M (4.7μH)
r_L	Max. of DC resistance	0.26Ω
C	$TAIYOYUDEN$ capacitor	JMK212BJ226MG-T (22μF)
r_C	ESR at 1MHz	3mΩ
Power MOSFET	$STMicrochip$ P&N-channel	STS8C5H30L
CMOS drivers	$elantec$	EL7457C
Power MOSFET dirvers	$elantec$	EL7202C
Power MOSFET	$Internationalrectifier$	IRF7103
ADC	$AnalogDevice$	AD9203
FPGA	$Xilinx$	Spartan-3E

Table 6.3: Design specification of buck converter and ADC

N	Number of phase	1
V_{in}	Input voltage	3.0V
V_{ref}	Max. reference voltage	1.5V
I_{max}	Max. load current	0.45A
f_s	Switching frequency	up to 4MHz
N_{ADC}	ADC resolution	10-bit
f_{sample}	ADC sampling frequency	16MHz
ΔV	Sampling voltage range	0∼2V

a parameter read-in module is embedded as a serial data receiver prototype that greatly reduces the amount of physical pins. The chip features are summarized as follows

- Standard PID control for the buck converter as a reference;
- SM control for the buck converter;
- Standard PID control for the boost converter as a reference;
- SM control for the boost converter;
- 1-1 DMASH Σ-Δ DPWM embedded in each controller;
- PLL generating a clock up to 128MHz with four phase shifts;
- Parameter read-in module reducing the amount of physical pins.

The proposed digital controller is also fabricated in $AustriaMicrosystemA$ 0.35μm CMOS process. The core area is about $5.3mm^2$ ($3.21mm \times 1.65mm$). A corresponding pad frame occupies about $11.0mm^2$ ($4.01mm \times 2.74mm$). The area details of each block are shown in Table. 6.4. Fig. 6.11 shows the die micrograph. There are 68 pins including the power pins for both core cells and peripheral cells. The package type is CLCC68.

Using the same FPGA motherboard as with the first chip, another test platform including the designated buck converter, boost converter and necessary peripherals, i.e. PLL, are built to evaluate the performances and efficiency of the implemented controllers. Several test modes are set for each block as

- PID control dedicated to the buck converter;
- SM control dedicated to the buck converter;

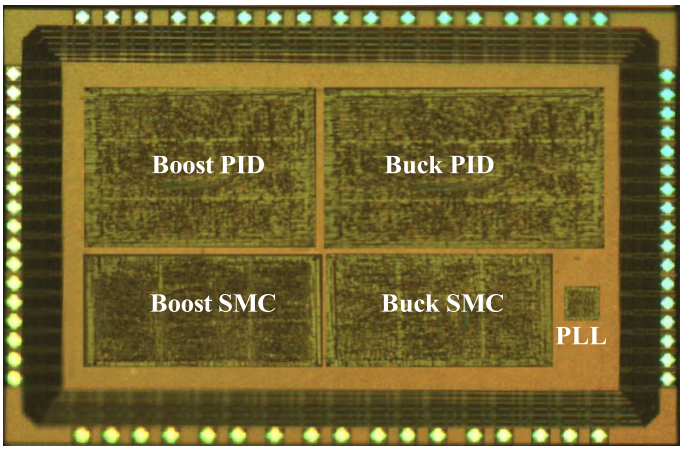


Figure 6.11: Die micrograph of the second chip

Table 6.4: Chip areas of each functional block

Module	Area/μm^2
PID control for the buck converter	1438603(1660×870)
SM control for the buck converter	837456(1375×605)
PID control for the boost converter	1155527(1370×840)
SM control for the boost converter	794660(1365×580)
PLL with four phase shift	24750(165×150)

– PID control dedicated to the boost converter;
– SM control dedicated to the boost converter;
– PLL performs as the clock source for each controller.

Fig. 6.12 shows the test board. The testbench schematics are shown in Appendix B.3 in detail. The buck converter configurations remain the same as with the previous chip as shown in Table. 6.2 and 6.3. The boost converter and PLL specifications are given in Table. 6.5.

6.4 Experimental Results with the First IC

A Xilinx XC3S500E FPGA board is used as the motherboard to provide necessary control signals and to implement the off-chip mode arbitration function as shown in Fig. 6.13. Here we use a 5-bit second-order idle-tone free Σ-Δ DPWM to achieve a better trade-off between required

Table 6.5: Design specification for the boost converter and PLL

N	Number of phase	1
V_{in}	Input voltage	3.0V
V_{ref}	Max. reference voltage	1.67V ($\frac{5V}{3}$)
I_{max}	Max. load current	0.5A
f_s	Switching frequency	up to 4MHz
f_{PLL}	PLL frequency	128MHz

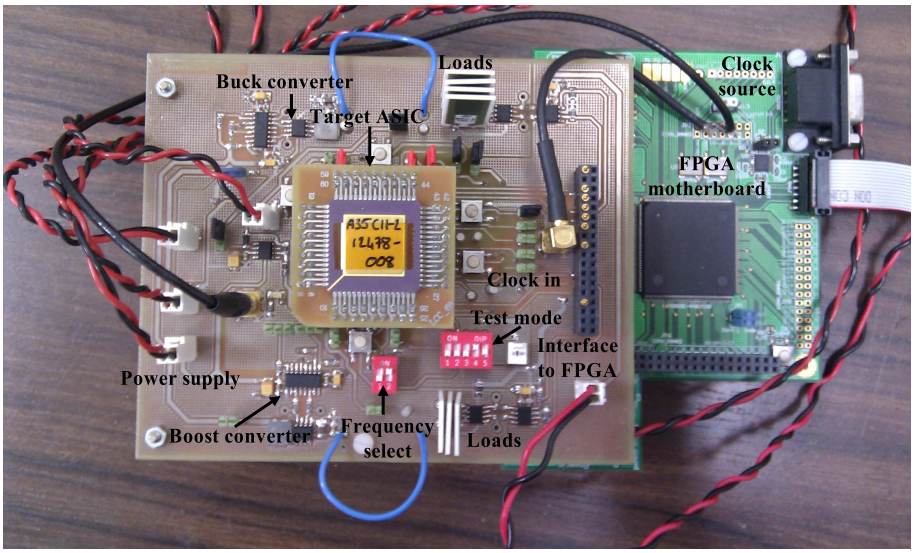


Figure 6.12: Experimental test platform for the second chip

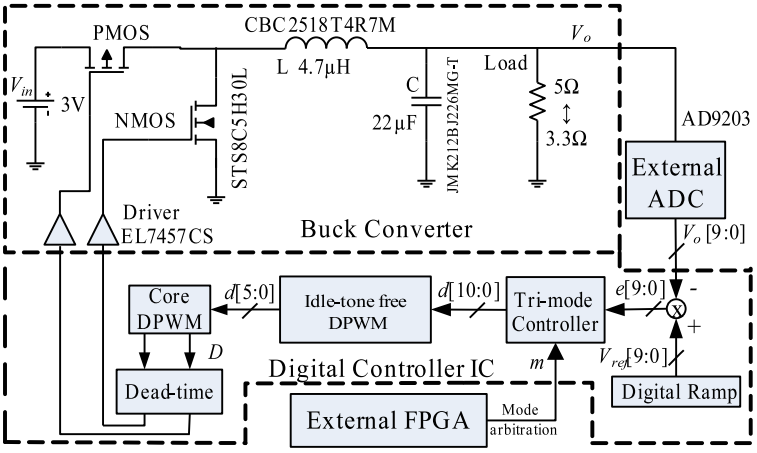


Figure 6.13: Experimental platform schematic of the improved power-aware tri-mode controller IC

system clock and output signal integrity. The stable DC output voltage of 1.5V can be normalized in the format of equivalent input bin as

$$\frac{V_{ref}}{V_{in}} \cdot 2^{N_{DPWM}} \notin l \cdot 2^{n-m} \pm 1 \tag{6.1}$$

that satisfies the guideline proposed in Section 4.1.2.

Fig. 6.14 shows the response using the improved tri-mode controller under load perturbations. Fig. 6.14(a) describes the operations from step 1 to step 3 illustrated in Section 2.2 when the load current changes from 0.3A to 0.45A. Fig. 6.14(b) describes the operations from step 3 to step 5 when the load current changes from 0.45A to 0.3A. Referring to Section 2.2, t_{tune1} and t_{tune2} are both set to $40\mu s$ to ensure a sufficient transient response time. e_{th} is set to $\frac{\Delta V}{2^{N_{ADC}}} = 15mV$. According to Fig. 6.14, the improved tri-mode controller exhibits better dynamic response ($153\mu s$ and $200\mu s$ respectively) than the stand-alone PID controller, although it takes a longer response

Table 6.6: Performances of the SM and PID controllers for the buck converter

Controller	PID	Sliding-mode		
Switching frequency(MHz)	1	1	2	4
Output voltage overshoot(mV)	69.0	10.2	19.0	33.2
Output voltage response (μs)	83.0	29.4	24.7	22.4

Table 6.7: Performances of the SM and PID controllers for the boost converter operating at 1MHz

Controller	PID	Sliding-mode
Output voltage overshoot(mV)	100.0	74.0
Output voltage response (μs)	75.6	22.0

than the stand-alone RST controller. The maximum output voltage ripple is 1.8mV. The power consumption of the tri-mode controller is anticipated to be much smaller than that of the stand-alone RST controller or the full-speed stand-alone PID controller. This issue will be discussed in Chapter 7.

6.5 Experimental Results with the Second IC

Fig. 6.15 describes a timing sequence example of the parameter read-in module. The enlarged part is the read-in details of the first parameter in the PID controller. The input digits are

$$(10000011000111000111001010000000001)$$

which correspond to the control parameter as

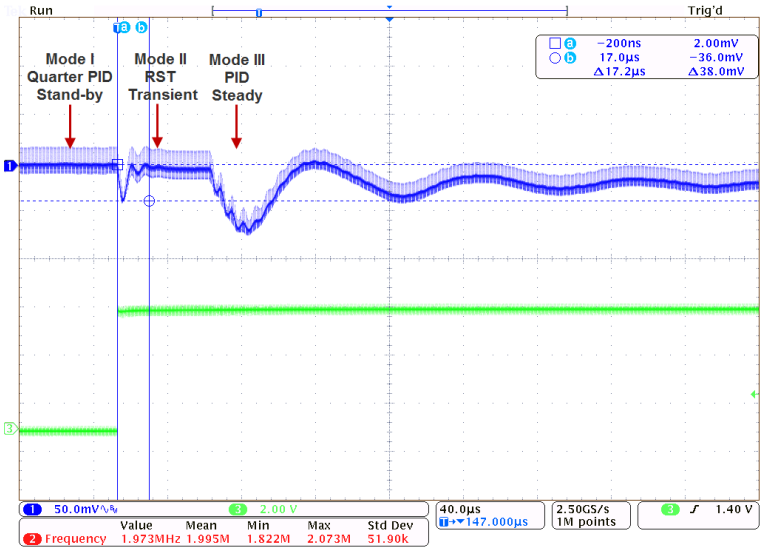
$$(00000000010100111000111000110000)$$

.

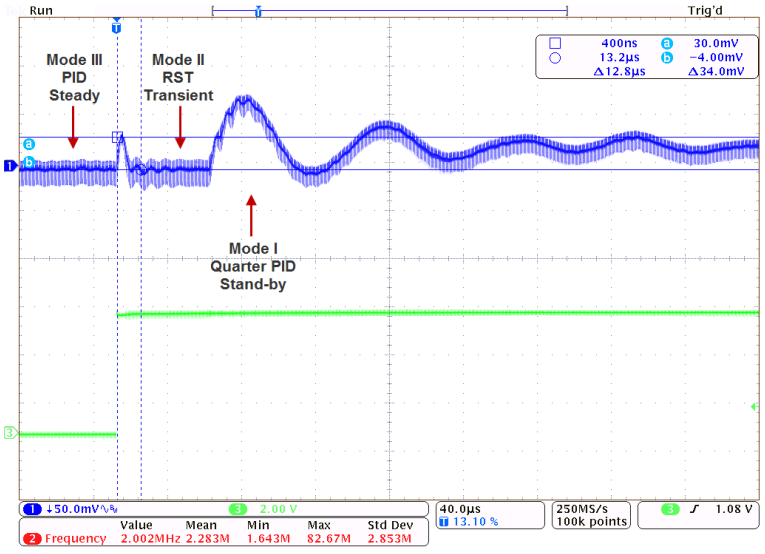
Fig. 6.16 shows the experimental results for the PLL. The implemented PLL with four phase shifts operates at 128MHz. Phase and frequency characteristics satisfy the specification of a standard digital system. A discussion about the power consumption of PLL will be given in Chapter 7 that leads to a feasible prototype of an on-chip clock generator dedicated to the digitally controlled DC-DC converter.

Fig. 6.17 and 6.18 show the performances of the SM and PID controllers for the buck converter, respectively. The SM controller operates up to 4MHz with acceptable steady-state and transient-state performances. Whereas the PID controller only supports up to 1MHz. The experimental results with lower frequencies are included in Appendix C. The controller dynamic performances for the buck converter are summarized in Table. 6.6.

Fig. 6.19 and 6.20 show the performances of the SM and PID controllers for the boost converter respectively. Both controllers operates up to 1MHz with acceptable steady-state and transient-state performances. The transient-state performances are summarized in Table. 6.7.



(a)



(b)

Figure 6.14: Output voltage of improved tri-mode controller operating at 2MHz switching frequency when load varies (a) from 0.3A to 0.45A, (b) from 0.45A to 0.3A

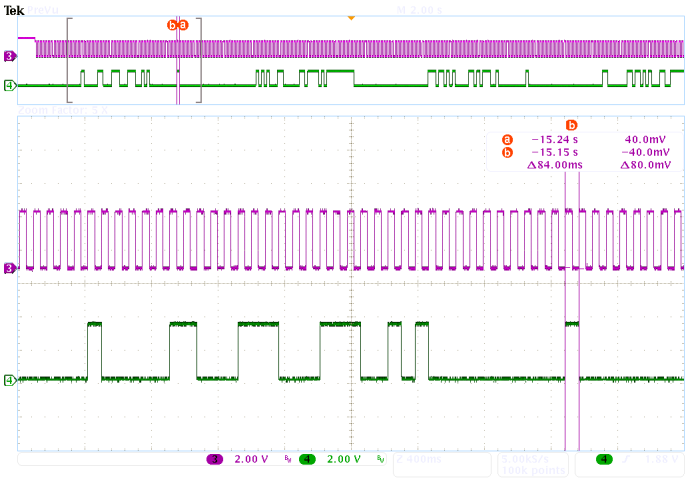
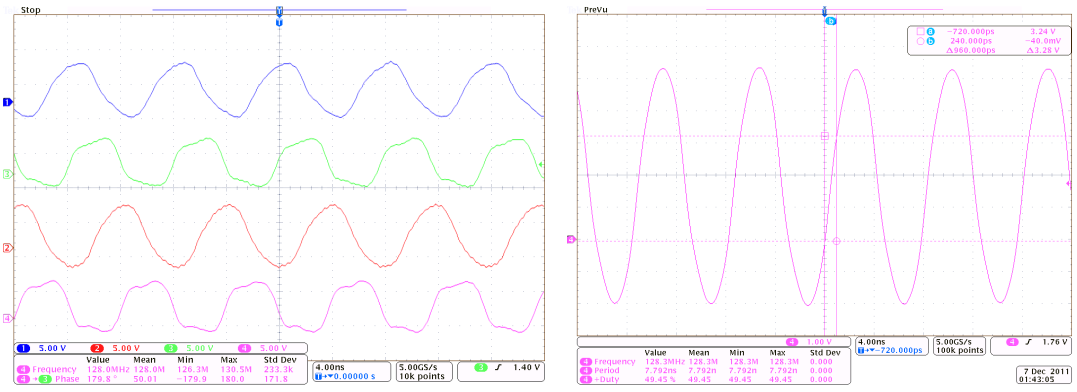
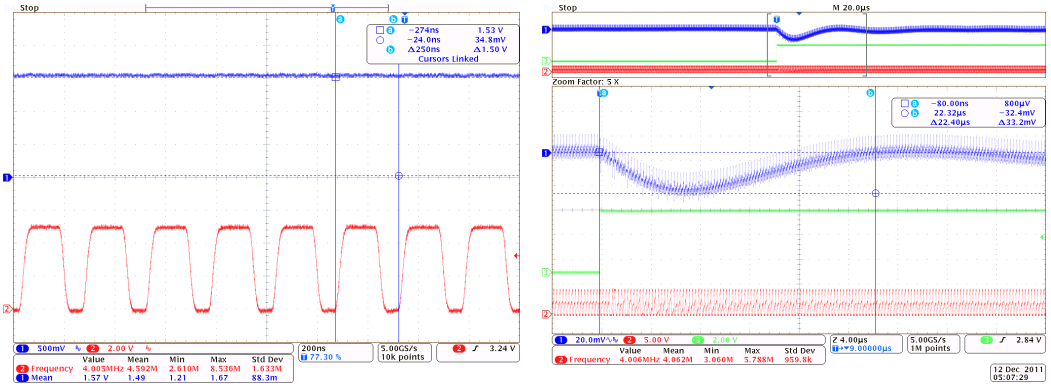


Figure 6.15: A timing sequence example of the parameter read-in module



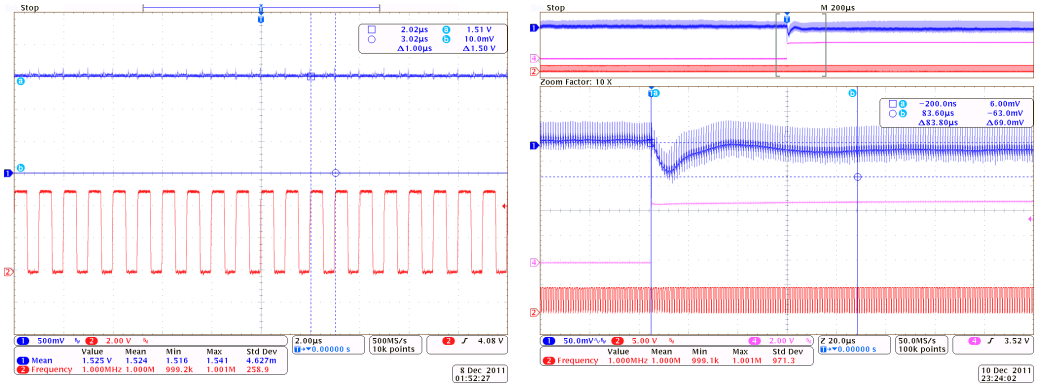
(a) (b)

Figure 6.16: Experimental waveform of the PLL at 128MHz (a) with 4 phase shifts, (b) one phase details



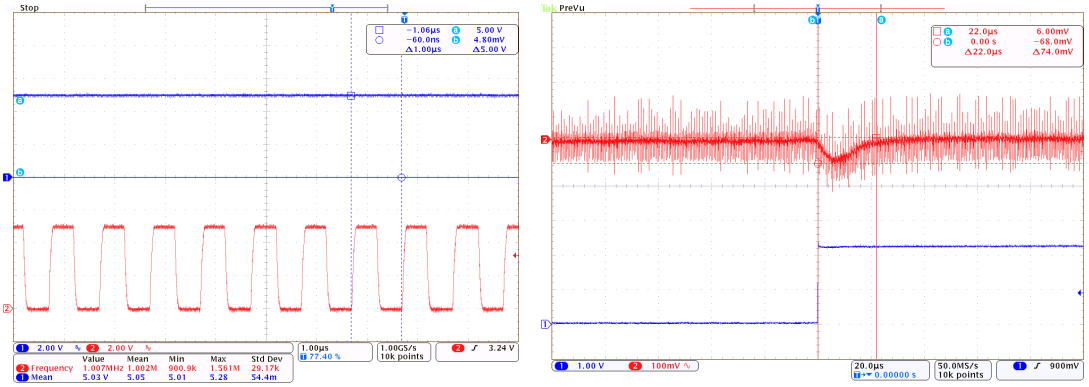
(a) (b)

Figure 6.17: SM controller for the buck converter: (a) steady-state operation at 4MHz, (b) load current change from 0.3A to 0.45A (R: from 5Ω to 3.3Ω)



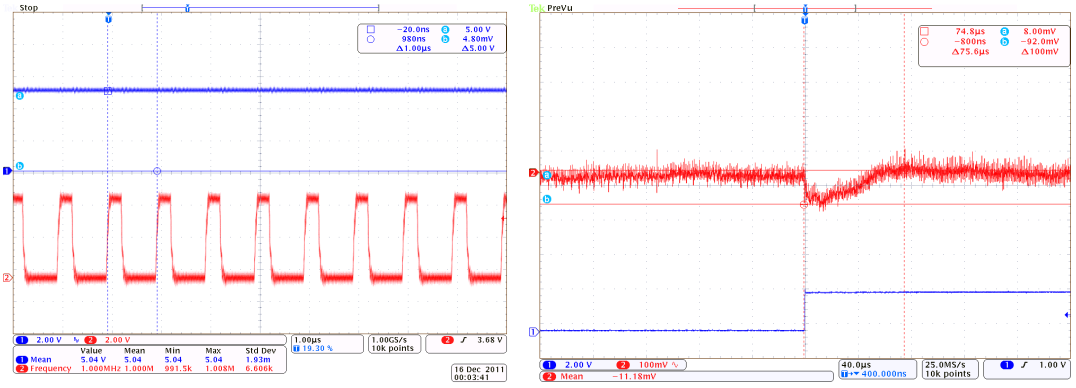
(a) (b)

Figure 6.18: PID controller for the buck converter: (a) steady-state operation at 1MHz, (b) load current change from 0.3A to 0.45A (R: from 5Ω to 3.3Ω)



(a) (b)

Figure 6.19: SM controller for the boost controller: (a) steady-state operation at 1MHz, (b) load current change from 0.33A to 0.5A (R: from 15Ω to 10Ω)



(a) (b)

Figure 6.20: PID controller for the boost controller: (a) steady-state operation at 1MHz, (b) load current change from 0.33A to 0.5A (R: from 15Ω to 10Ω)

6.6 Summary

Following the digital design flow, two controller ICs are designed, implemented and tested. A simulation model is built using VHDL-AMS that realizes the pre-chip performance simulation. The improved power-aware tri-mode controller is implemented in the first chip. PID and SM controllers for both buck and boost converters respectively are implmented in the second chip. Experimental results verify the closed-loop operations and the anticipated performances discussed in previous chapters. Based on the experimental results with respect to the power losses, the power issues of the digital controller will be discussed in the next chapter.

Chapter 7

Power Consumption Evaluation of Digital Controllers

In addition to the control performances mentioned in previous chapters, the power consumption of the implemented digital controllers is another main concern to evaluate the efficiency compared to the analog counterparts. According to [Wei 96a], the anticipated power consumed by the digital controller takes 4.55% to 9.44% of the total power losses. Based on this assumption, a static power analysis is performed to anticipate the appropriate applications of digital controllers. Firstly, the power consumption in VLSI is discussed to clarify the power contributors during static power analysis. Three main power contributors define the total power losses including the dynamic power consumption due to charging and discharging capacitances, another type of dynamic power consumption due to direct path currents and the static power consumption. In order to optimize the power consumption, circuit-level and system-level strategies can be performed simultaneously. Clock gating and operand isolation are also discussed as two important power optimization methods at circuit-level. System-level optimizations including parallelism, pipelining, sleep mode do not fall into the thesis scope.

Power analysis provides an effective approach to estimate a digital controller in different technologies especially in deep sub-micron or nanometer which will lead to expensive tape-out cost. The fitting operation between the experimental power consumption and the simulation results guarantee that such estimation falls in a practical power range. Therefore, the estimated power consumption in advanced CMOS technologies will be obtained to anticipate a reasonable power range of application.

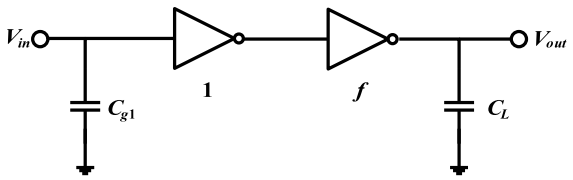


Figure 7.1: Schematic to determine the minimum sized inverter

7.1 Effective Power Estimation Model

From the perspective of power estimation, the power consumption of a digital integrated circuit can be modeled at circuit-level and system-level respectively. Within both levels, CMOS inverter is used as an objective case that eases an extrapolation to complex gate, such as logic gates, adders and data-path. Power analysis and optimization in circuit-level sort the power consumption approaches into three categories. The total power consumption of an inverter is expressed as [Liu 93, Unsal 03]

$$P_{total} = P_{cap} + P_{dp} + P_{static} \tag{7.1}$$

where P_{cap} is the dynamic power consumption due to the charging and discharging of capacitances also known as net power dissipation; P_{dp} is another type of the dynamic power consumption due to direct path during switching, also known as internal power dissipation; P_{static} is the static power dissipation caused by a leakage current during steady-state, also known as leakage power dissipation.

Dynamic power consumption due to the charging and discharging of capacitances can be obtained from the integration of the instantaneous power over the period of interest. Each switching cycle consumes a fixed amount of energy, equal to $C_L V_{dd}^2$. Here C_L stands for the net capacitance while V_{dd} is the supply voltage. Provided that the target gate exists the input voltage transient f_{TR} times per second, the power consumption is therefore given by

$$P_{cap} = C_L V_{dd}^2 f_{TR} \tag{7.2}$$

Actually f_{TR} is the toggle rate that turns out to reflect the switching activity. It is a critical parameter to determine P_{cap}.

The three factors included in (7.2) provide three possible power reduction approaches. It makes sense to reduce the load capacitance C_L in a power-aware design. Load capacitance C_L is mainly contributed by gate and diffusion capacitors that offer a trade-off between the reasonable transistor size and circuit performances. The circuit performance loss due to the reduction of load capacitance C_L can be compensated by specific system-level boost architecture such as pipeline architecture. The minimum transistor size can be estimated by a CMOS inverter-based testbenches as shown in Fig. 7.1

In Fig. 7.1, f is the effective fan-out per stage, while it also indicates the equivalent inverter size ratio with respect to the preceding gate, here known as sizing factor. As a two-stage serial

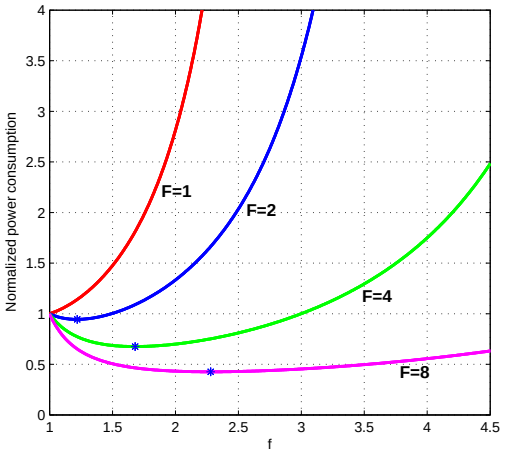


Figure 7.2: Normalized power consumption with respect to adopted process

inverter network, the overall effective fan-out is defined as $F = C_L/C_{g1}$, the relation between the effective fan-out f and the supply voltage V_{dd} conforms to [Rabaey 03]

$$\left(\frac{V_{dd}}{V_{ref}}\right)\left(\frac{V_{ref}-V_T-\frac{V_{DSAT}}{2}}{V_{DD}-V_T-\frac{V_{DSAT}}{2}}\right)\left(\frac{2+f+\frac{F}{f}}{3+F}\right)=1 \tag{7.3}$$

where V_T is the threshold voltage, V_{DSAT} is the saturation drain voltage. Based on (7.3), the normalized power consumption as a function of the sizing factor f reads

$$E_{norm}=\left(\frac{V_{dd}}{V_{ref}}\right)^2\left(\frac{2+2f+F}{4+F}\right) \tag{7.4}$$

A graphical interpretation of (7.4) is therefore shown in Fig. 7.2. Several power minimization guidelines are drawn as follows

- Overall effective fan-out $F = 1$ automatically leads to the minimum size device as the most effective one.
- Except the condition $F = 1$, other possible situations of F exist a value (asterisks in Fig. 7.2) to achieve the minimum dynamic power consumption requiring $f > 1$. In other words, the increase in gate size to some extent can reduce the dynamic power consumption.
- A tipping point reverses the power reduction tendency (marked by asterisks in Fig. 7.2). That is to say, oversizing the transistors beyond the optimal value comes at a hefty price in energy.

The square relationship between dynamic power consumption and supply voltage in (7.2) agrees as shown in (7.4). Reducing V_{dd} has therefore a quadratic effect on P_{cap}, but the voltage reduction amplitude is strictly constrained by the threshold voltage V_T. Multiple supply voltages technique and dynamic threshold voltage technique at system-level are typical cases adopting the foregoing theory as long as the performance is guaranteed to be acceptable.

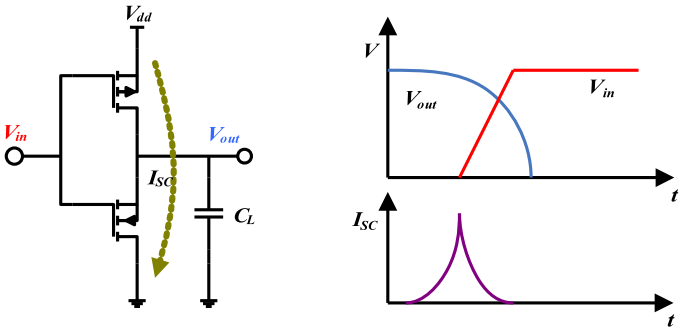


Figure 7.3: Direct path caused by short current during switching

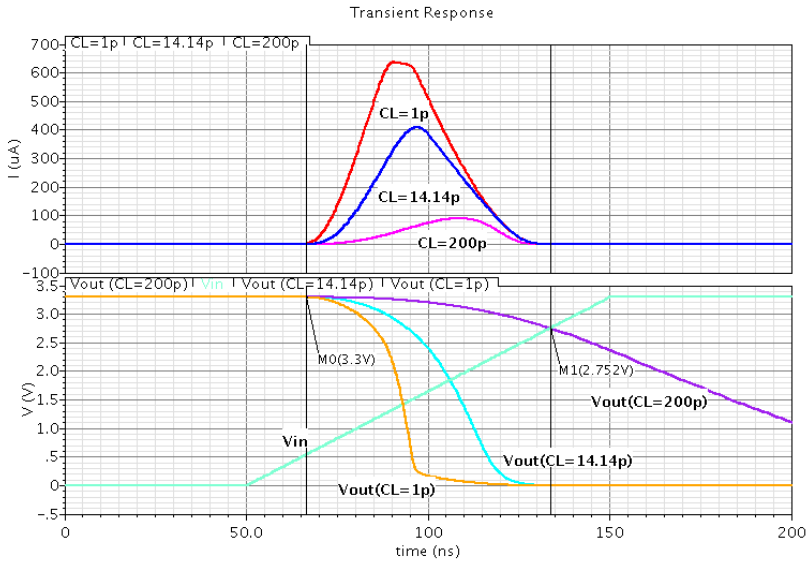


Figure 7.4: Short current through inverter as a function of load capacitance

The toggle rate f_{TR} represents the switching activity that can be instantiated by a RTL simulator. The common formats designated to EDA tools are TCF, SAIF and VCD.

Next, we will focus on the second term in (7.1). Direct path power dissipation P_{dp} is the power consumed by an instantaneous short circuit connection between the voltage supply and the ground during the gate transitions. Fig. 7.3 shows the occurrence mechanism of a direct path. A transient simulation result in Fig. 7.4 illustrates the reduction of the direct path effect as a function of load capacitance for a fixed input slope of 100ns. It indicates that larger capacitive load C_L assures lower direct path currents. This conclusion offers the similar requirements to the size of the latter gates comparable to that of the aforementioned power minimization guideline.

The static power dissipation P_{static} is usually modeled in the target library as a constant. The corresponding keyword is "cell_leakage_power ". Generally speaking, the primary source of leakage current comes from the reversed-biased diode junctions located between the source or drain and the substrate. The important source of leakage power consumption is shown in Fig. 7.5. In $AustriaMicrosystemS$ 0.35μm CMOS C35B4C3 library, cell INV0 has the leakage power of

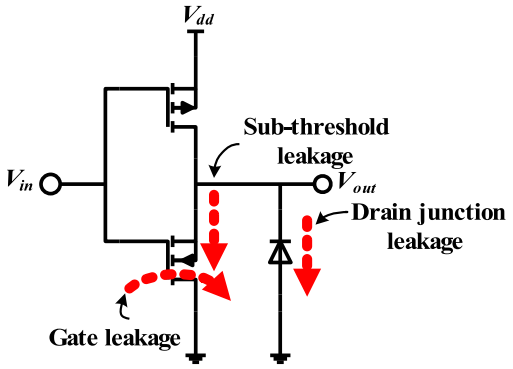


Figure 7.5: Sources of leakage power consumption

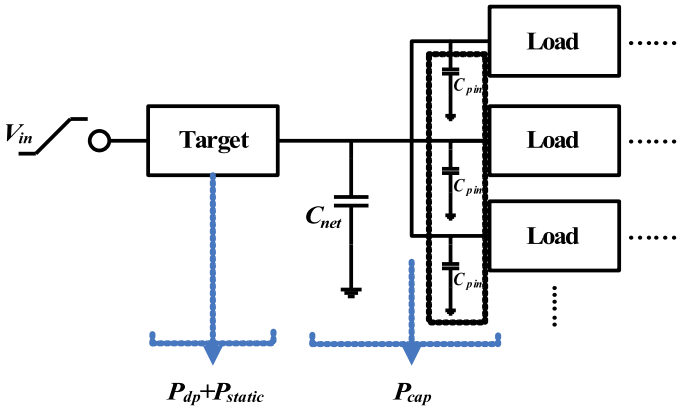


Figure 7.6: Modeling of a power dissipation module by EDA tools [from Cadence RTL Compiler manual]

33.028pW. The overall static power of a 5000 equivalent gates PID controller is estimated around 165nW. It turns into a less critical issue compared to other two power contributors.

As the analysis tools with high efficiency, mainstream EDA tools are capable of reporting the power consumption during RTL synthesis. Based on aforementioned power dissipation basis, EDA tools model a power dissipation module as shown in Fig. 7.6.

Beside of the system-level power optimization techniques such as pipelining and parallelization, power optimization can be carried out during code synthesis according to the aforementioned power sensitive factors. There are several prevalent synthesis approaches to further reduce the power consumption. Clock gating is one of effective approaches to reduce the dynamic power dissipation on sequential elements and clock circuitry. This technique is inspired by an idea that relates to item f_{TR} in (7.2). By introducing a gate to control the input clock of target module as shown in Fig. 7.7, power will not be dissipated during the idle period when the register is shut off by the gating function. However, clock gating is not always suitable for any sequential block. Fig. 7.8 gives situation that requires another prevalent power reduction technique, operand isolation. If $RegA$ and $RegB$ update once in each period, it is obvious that clock gating is not compatible with the topology. But the most power consuming block, multiplier, can be stand-by when $en = 0$. So

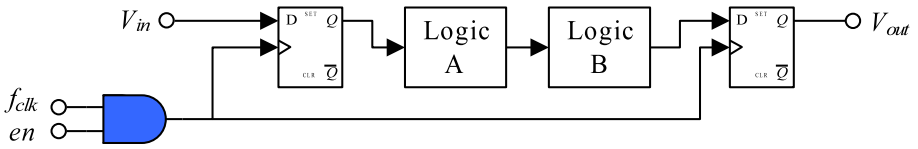


Figure 7.7: Basic clock gating principal

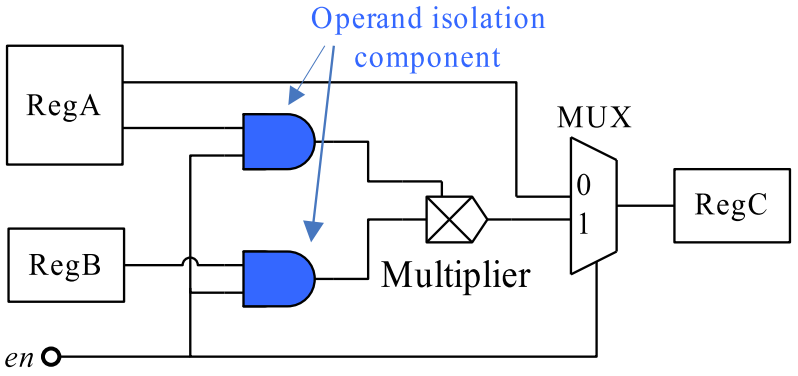


Figure 7.8: Basic operand isolation principal

the operand isolation block, normally inserted as a series of AND gates, can shut down (isolate) the function unit (operand) so that no dynamic power is dissipated when the result of the power sensitive block is not required. Normally, this technique can reduce the power dissipation in data-path blocks to the expense of the complex clock gate managements. The clock gate management draws also power and a win-win trade-off must be settled.

Both clock gating and operand isolation are feasible approaches to reduce the dynamic power that is a great part of the total power loss. Other techniques can also reduce the power consumption in (7.1) such as the multiple supply voltage design, dynamic threshold scaling, leakage power optimization and so on. Leakage current losses are another contributor to consumption. Voltage scaling down to sub-threshold range is a solution to fight leakage. Power switches are also mandatory for elimination. Unfortunately such latter solutions may not accommodate easily high frequency operations. A power consumption and controller efficiency model can be established so that an estimated power value can be obtained for each controller. A feasibility study of digital controllers for power converters compared to analog counterparts will be given in Section 7.2.

7.2 Feasible Evaluation of Power Consumption

All the experimental power consumptions are obtained by $Tektronix$ AC/DC current probe (TCP0030) and the mixed signal oscilloscope (MSO4104). Each controller has its own power supply so as to identify a correct power source.

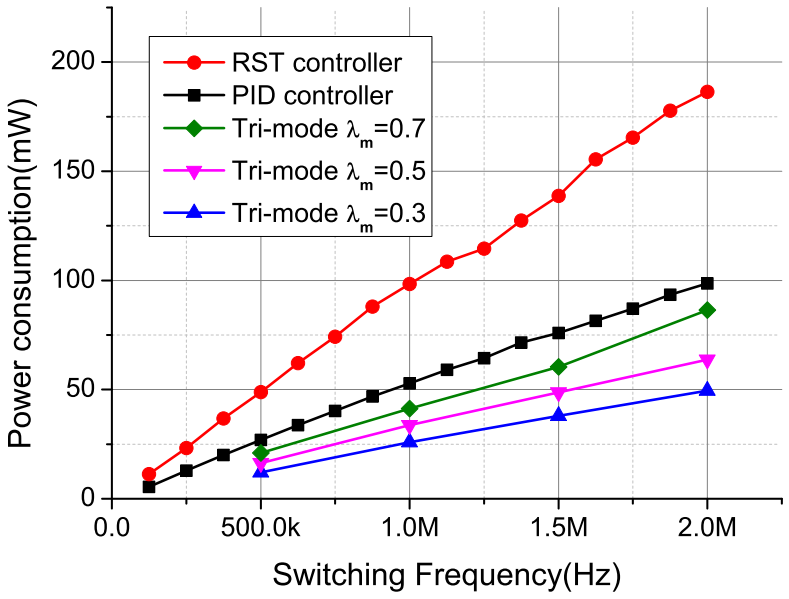


Figure 7.9: Power consumption of the proposed tri-mode controller compared to stand-alone PID and RST controllers with respect to the SMPS switching frequency

7.2.1 Power Consumption Analysis of the Power-aware Tri-mode Controller

Besides it assures acceptable steady-state and transient-state performances, power consumption of the improved power-aware tri-mode controller along with the idle-tone free Σ-Δ DPWM is another important assessment parameter that influences the overall converter efficiency. The same testbench is used to perform an experiment illustrating the power loss. Durations t_{tune1} and t_{tune2} are maintained at $40\mu s$ as described in Section 6.4. A parameter λ_m is defined here to represent the time ratio of non-stand-by operation mode, that is the total time of transient mode and steady-state mode. Fig. 7.9 shows the experimental power consumption of the improved power-aware tri-mode controller for the time ratio λ_m equals to 0.3, 0.5 and 0.7 respectively. The stand-alone PID and RST controllers are also shown here as a comparison. Here we take $\lambda_m = 0.5$ as an example, i.e. half of the operation time falls in stand-by mode. The power consumption of the tri-mode controller is only 64.55% of the one of the PID controller and 34.18% of the one of the RST controller at a switching frequency of 2MHz. That is to say 32.15mW/MHz with a supply voltage $V_{dd} = 3.3$V and output voltage $V_o = 1.5$V. The situations for $\lambda_m = 0.3$ and $\lambda_m = 0.7$ result in power consumption of 24.56mW/MHz and 42.83mW/MHz respectively.

If the power consumption of 24.56mW/MHz corresponding to $\lambda_m = 0.3$ is taken here as an example, it is possible to evaluate the range for the controller output power when a given efficiency is to be targeted. The output power is ideally given by

$$P_{out} = \frac{P_{loss}}{\frac{1}{\eta} - 1} \tag{7.5}$$

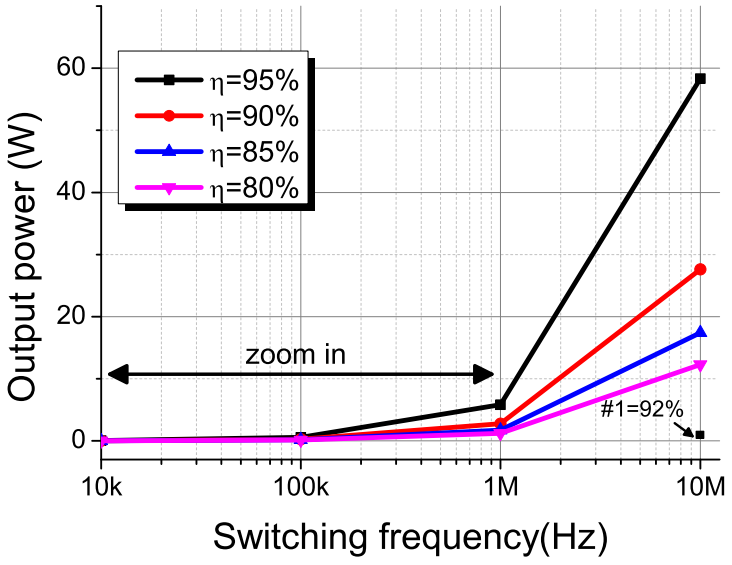
where P_{out} is the estimated output power, P_{loss} is the total amount of dissipated power consumption including power losses from the controller, drivers and power switches, η is the normalized power efficiency. According to the conclusion of [Wei 96a], we assume that the power losses of a digital controller should not account for more than 8% of the total power loss, that is $P_{loss} = 307$mW/MHz. Then the estimated SMPS output power P_{out} is shown in Fig. 7.10 with respect to the switching frequency and different global power efficiency targets (η =95%, 90%, 85% and 80%). Corresponding to the marked point #1, #2 and #3 in Fig. 7.10, [Ma 08], [Su 08] and [Zheng 11] offer a comparison of power converters' performances with analog controllers. It can be seen that the improved digital tri-mode controller is preferable for a SMPS with higher output power than the analog counterparts at the same switching frequency. Digital control is suitable for operation in medium power applications if the switching frequency is higher than 1MHz. If the switching frequency is restricted within 1MHz, a higher efficiency is anticipated for low-power applications.

7.2.2 Power Consumption Analysis of the Second Chip

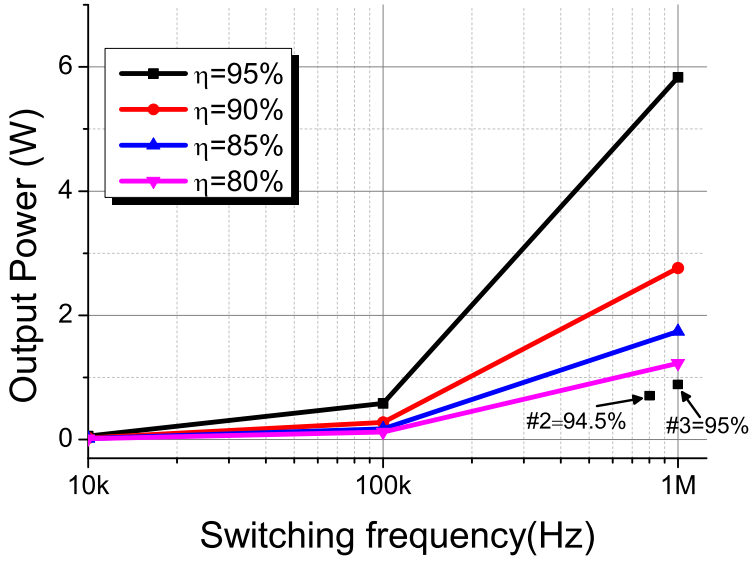
As discussed in Section 7.2.1, the stand-alone PID controller in the first chip consumes more power than the analog counterpart when operating at the same switching frequency. The tri-mode method improves the power efficiency to some extent at the expense of more silicon area. In order to further reduce the power consumption, the VHDL code is optimized in system-level to reduce the requirement for high system clock frequency. The improvements focus on how to combine possible calculation steps into one **CASE** step providing that not only the calculation delays satisfy the minimum timing requirement but also that possible timing mistakes caused by such calculation combinations are eliminated. Even the calculation of the 1-1 DMASH Σ-Δ DPWM can also be embedded into the calculation of the digital controller. Such a code optimization leads to a reduction of calculation cycle, i.e. the second chip requires 32 clock cycles instead of 128 clock cycles in the first one. According to (7.1) and (7.2), the power consumption at the same switching frequency is anticipated to consume only a quarter of the power in the first chip. In the meantime, some system-level power optimization strategies are applied, such as a reasonable clock gating, operand isolation and leakage power optimization as discussed in Section 7.1.

The experimental results demonstrate even a better power efficiency than the quarter power anticipation as shown in Fig. 7.11. The power consumption of the PID controller is 5.28mW/MHz, approximately one-tenth power of the stand-alone PID controller in the first chip. The SM controller reaches 4.46mW/MHz which gains 15.5% power of that of the PID controller in the same chip due to the simpler algorithm (referring to Table. 5.3).

The estimated output power of the SM controller can be evaluated by the approach proposed in Section 7.2.1. For the SM controller, a possible output range is shown in Fig. 7.12. Corresponding to #1, #2 and #3, the same references [Ma 08], [Su 08] and [Zheng 11] illustrate that the power consumption is significantly reduced compared to Fig. 7.10, and the power efficiency of the SM controller is comparable to that of the analog counterpart. It can apply to low and medium power applications with high power efficiency.



(a)



(b)

Figure 7.10: Anticipated output power versus switching frequency of a buck converter controlled by the improved power-aware tri-mode controller (a) with switching frequency from 10kHz to 10MHz, (b) zoom for switching frequency from 10kHz to 1MHz

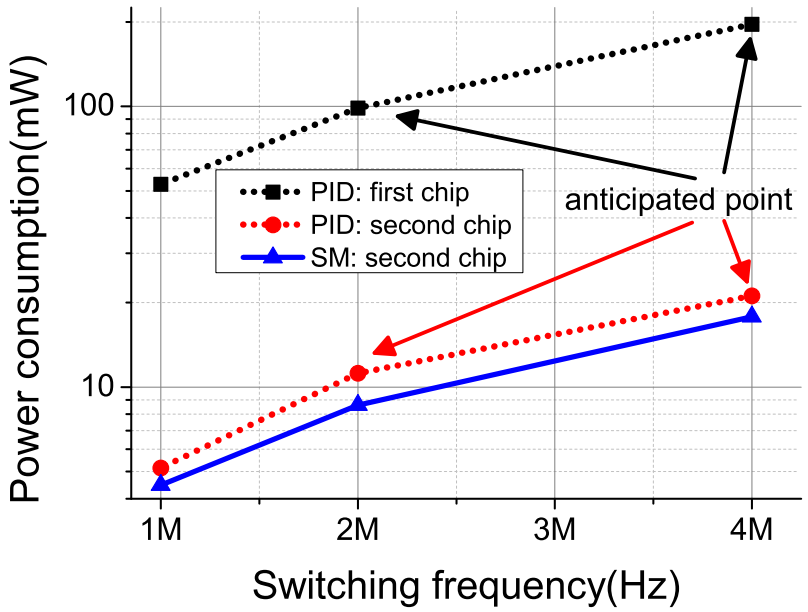


Figure 7.11: Power consumption versus switching frequency of the PID and SM controllers in the second chip compared to the PID controller in the first one

In the second chip, the power consumptions of the PID and SM controllers for the boost converter are 5.28mW/MHz and 4.79mW/MHz respectively.

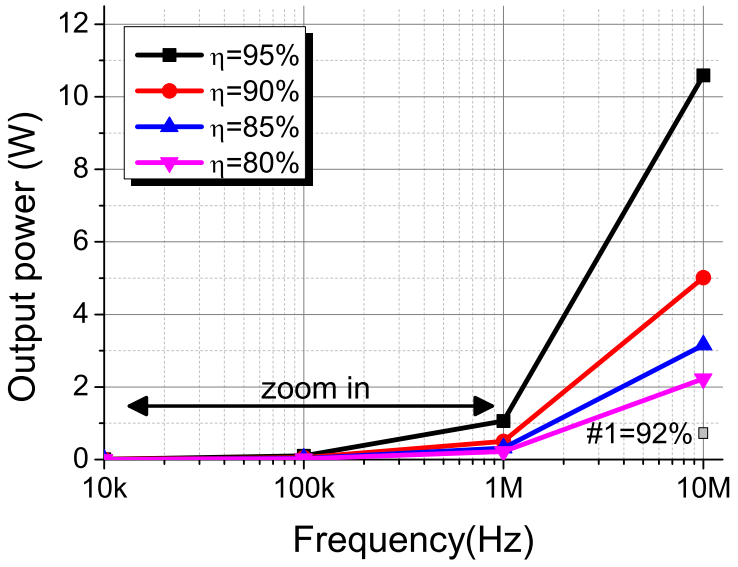
7.2.3 Power Estimation in Advanced Technologies

Aforementioned power consumption of implemented controllers is obtained in normal operating conditions with a specific CMOS technology. Benefiting from the power analysis tools and comparing to the experimental results, a general power estimation is performed to predict the power losses of a digital controller in other technologies.

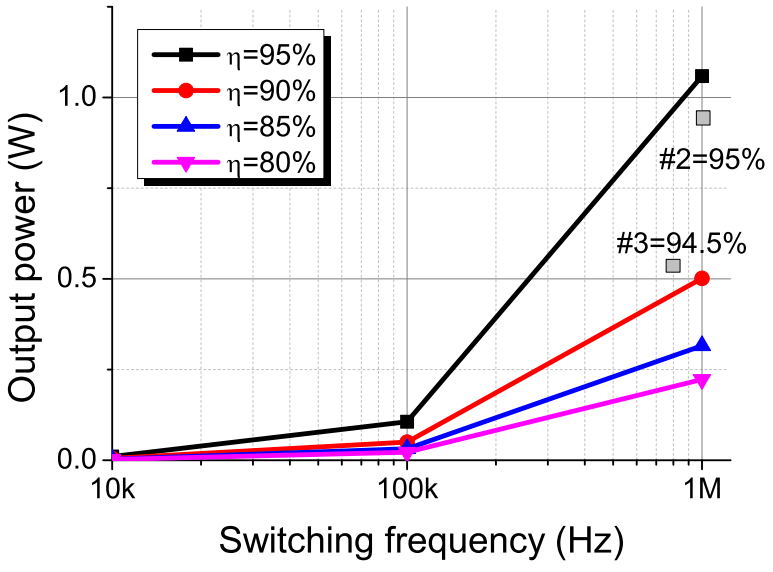
According to the simulation results of the PID controller in the first chip, the proportions of leakage power losses in advanced CMOS technologies are shown in Fig. 7.13. It takes more and more power losses with the scaling of CMOS technologies, especially in the nanometer era. Actually, the absolute value of leakage power losses for a specific case is technology dependent.

According to (7.2), when the process scales down by a factor of α, C_L is therefore reduced by α. The scaling factor of the supply voltage V_{dd} is defined as β. So the power scaling factor is $\alpha \cdot \beta^2$.

From $0.35\mu m$ to $0.18\mu m$, V_{dd} is reduced from 3.3V to 1.8V, thus power losses will be reduced by about 6.5. Referring to the stand-alone PID power losses illustrated in Fig. 7.9, the corresponding power estimation in advanced processes ($0.25\mu m$ (2.5V), $0.18\mu m$ (1.8V), $0.13\mu m$ (1.2V), $90nm$ (1.2V) and $65nm$ (1.0V)) can be obtained as the dash lines in Fig. 7.14. It is a conservative estimation because it does not take into account the possible additional power losses with parasitic losses caused by the technology scaling down. The gate-level power analysis provides an estima-



(a)



(b)

Figure 7.12: Anticipated output power versus switching frequency of a buck converter controlled by the SM controller (a) with switching frequency from 10kHz to 10MHz, (b) zoom for switching frequency from 10kHz to 1MHz

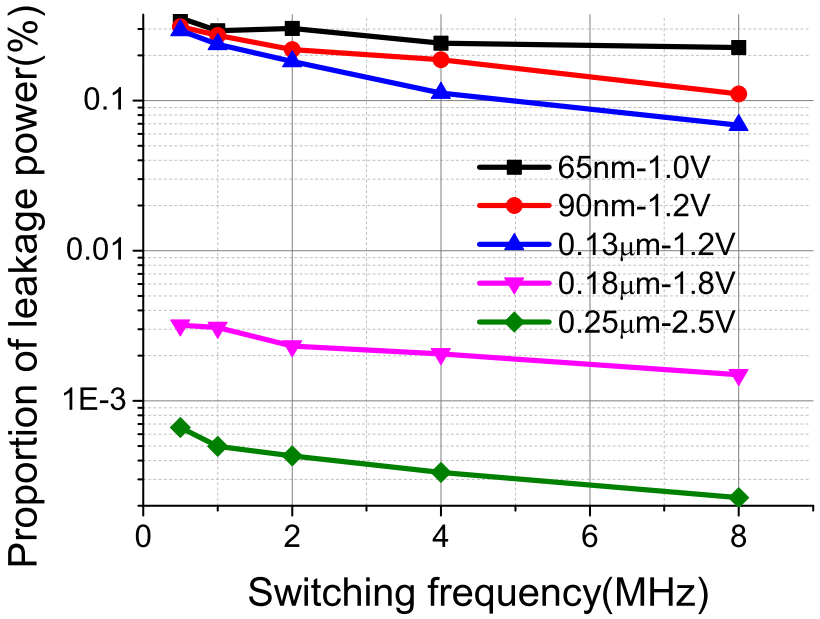


Figure 7.13: Proportion of leakage power losses from the stand-alone PID controller in the first chip with 0.25μm, 0.18μm, 0.13μm, 90nm and 65nm CMOS processes respectively

tion in extreme conditions since all combinational and sequential logic circuits are considered to work simultaneously. The corresponding simulation results are shown as solid lines in Fig. 7.14. Provided that the frequency remains the same, the power losses range between the two estimations is the practical range. With the technology scaling down, especially when the feature size comes smaller than 0.13μm, the power losses of stand-alone PID controller are foreseen as less than 50mW when the switching frequency is 8MHz. A further anticipation in Fig. 7.14 shows that the power losses can be limited to 5.0mW/MHz in nanometer-level technologies (for example 90nm). The power losses can be further reduced with the improved power-aware tri-mode controller and it is comparatively insignificant to the total power losses of a power supply-on-chip (PwrSoC) or a power IC. It assures therefore the feasibility of embedding digital control into a PwrSoC or a power IC from the viewpoint of power-aware design.

According to the discussion in Section 7.2.2, power-aware optimizations are performed in the second chip. It is therefore anticipated to exhibit higher power efficiency. Firstly, the same analysis method is adopted to the optimized PID and SM controllers for the buck converter as shown in Fig. 7.15 and 7.16 respectively. Compared to Fig. 7.14, the estimated power losses of the optimized PID controller is decreased by one order of magnitude. This conforms the results obtained from Section 7.2.2. The simulation results show a reduction of 42%. So such an optimization improves the power efficiency range from 45% (145mW $\rightarrow$ 80mW in 0.25μm)to 80% (2.5mW $\rightarrow$ 0.5mW in 65nm). Especially, the power losses are limited to 3.3mW/MHz in nanometer-level technologies (for example 90nm). It is worthwhile to notice that the absolute values of estimation deviation between the simulation results and estimated results become smaller, however, the relative deviations come much more larger when compared the two chips (see Fig. 7.14 and 7.15). It is due to

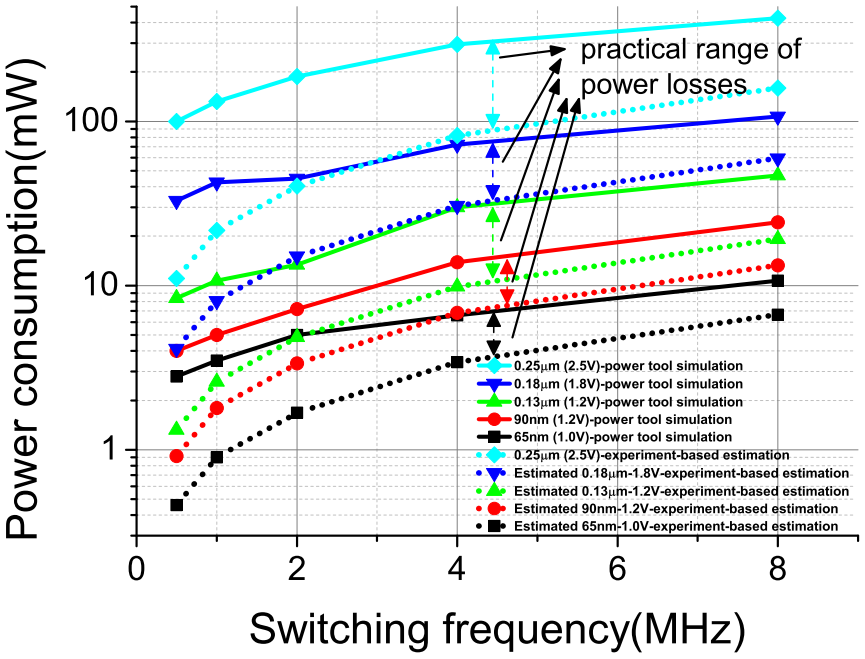


Figure 7.14: Practical range of power losses for the stand-alone PID controller in 0.25μm, 0.18μm, 0.13μm, 90nm and 65nm CMOS process respectively using a dedicated power simulation tool and extrapolation from experimental data

the derivation caused by an imperfect power model. Compared to the 13.4mW of PID controller power losses, the maximum possible power losses of the optimized SM controller in 0.13μm are 7.5mW when the switching frequency is 8MHz. The corresponding power losses are further limited to 1.8mW/MHz in the nanometer-level technologies (for example 90nm). Taking this value to estimate the possible output power range as illustrated in Section 7.2.1 gives the comparative analysis in Fig. 7.17 with [Ma 08], [Su 08] and [Zheng 11]. The compatible minimum output power is further reduced. Moreover, it can achieve even a higher conversion efficiency compared to advanced analog controllers. Regarding the steady-state and transient-state performances discussed in Chapter 6, the SM controller is anticipated to exhibit a significant good power efficiency compared to the analog counterpart.

Fig. 7.18 and 7.19 show the practical power losses ranges for the PID and SM controllers for the boost converter in several CMOS processes respectively. The corresponding power losses are 2.0mW/MHz and 1.5mW/MHz in nanometer-level technologies (for example 90nm). All the conclusions derived from the controllers for the buck converter are suitable to the boost converter.

According to above analysis, the power losses of digital controllers are anticipated to be limited to a reasonable range with advanced CMOS technologies, especially in a process of deep submicron and nanometer. Improved power-aware tri-mode and SM controllers are candidate to allow similar or less power losses than the analog counterpart when operating at the same switching frequency. Possible switching frequency range remains in the kHz to 10MHz.

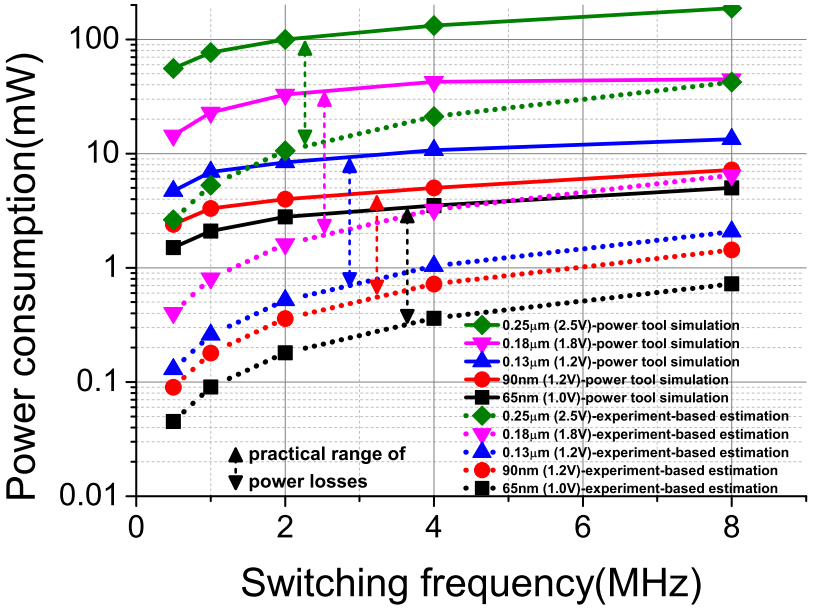


Figure 7.15: Practical range of power losses for the optimized PID controller in 0.25μm, 0.18μm, 0.13μm, 90nm and 65nm CMOS process respectively using a dedicated power simulation tool and extrapolation from experimental data

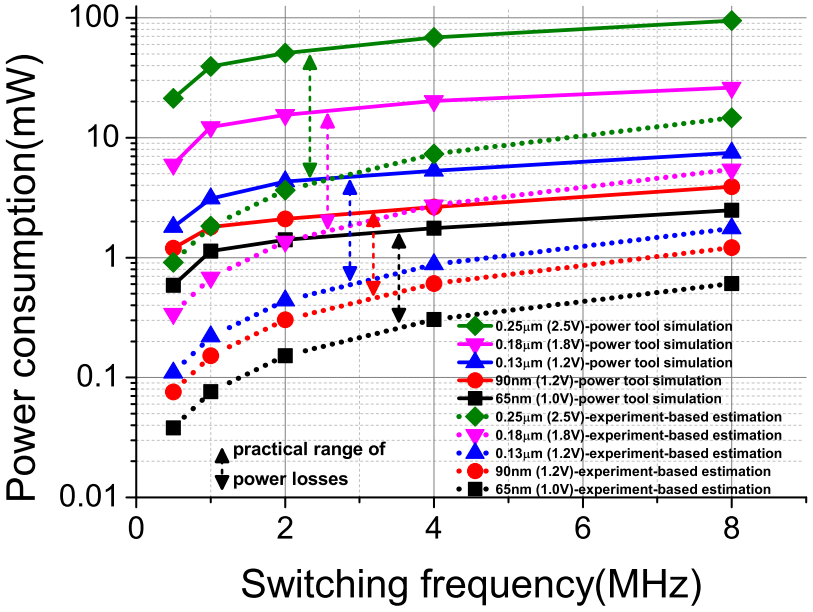
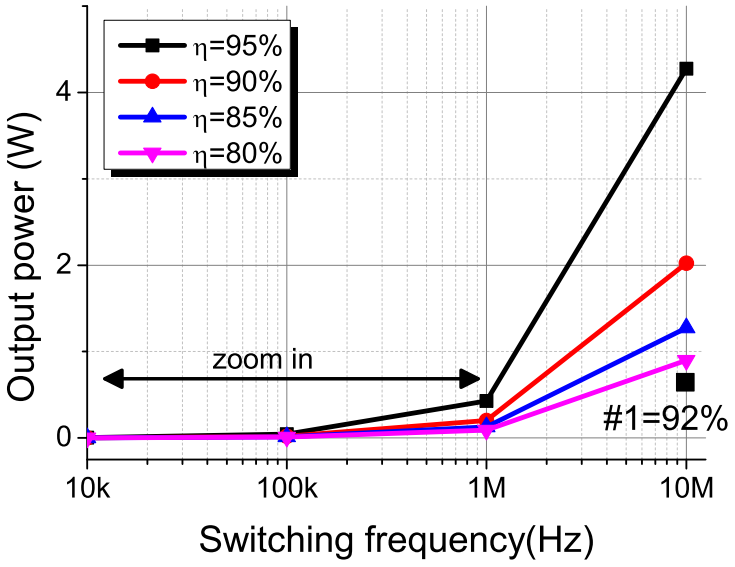
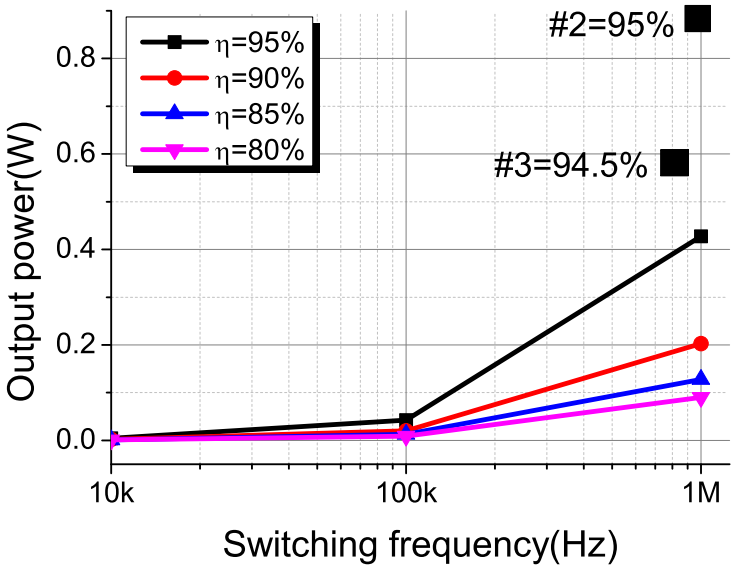


Figure 7.16: Practical range of power losses for the optimized SM controller in 0.25μm, 0.18μm, 0.13μm, 90nm and 65nm CMOS process respectively using a dedicated power simulation tool and extrapolation from experimental data



(a)



(b)

Figure 7.17: Anticipated output power versus switching frequency of a buck converter controlled by the SM controller in 90nm CMOS process (a) with switching frequency from 10kHz to 10MHz, (b) Zoom for switching frequency from 10kHz to 1MHz

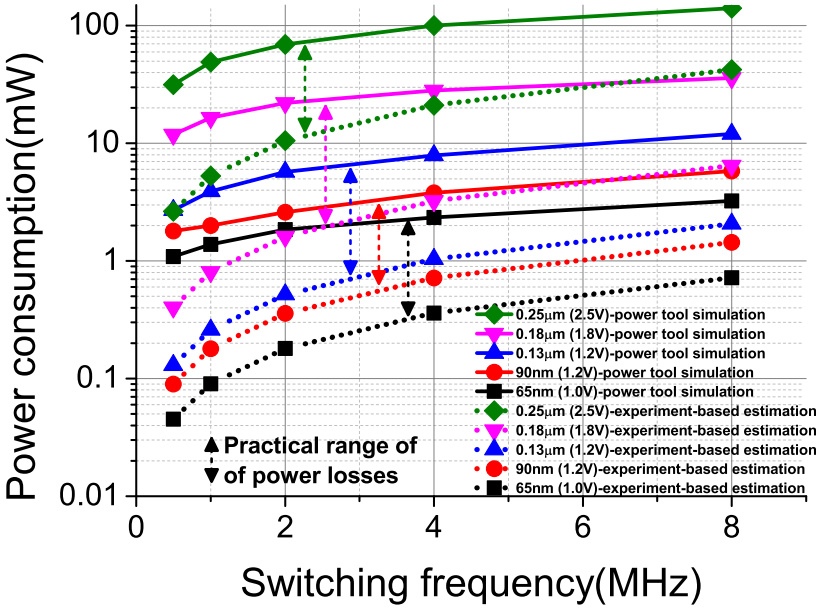


Figure 7.18: Practical range of power losses for the optimized PID controller for the boost converter in 0.25μm, 0.18μm, 0.13μm, 90nm and 65nm CMOS process respectively using a dedicated power simulation tool and extrapolation from experimental data

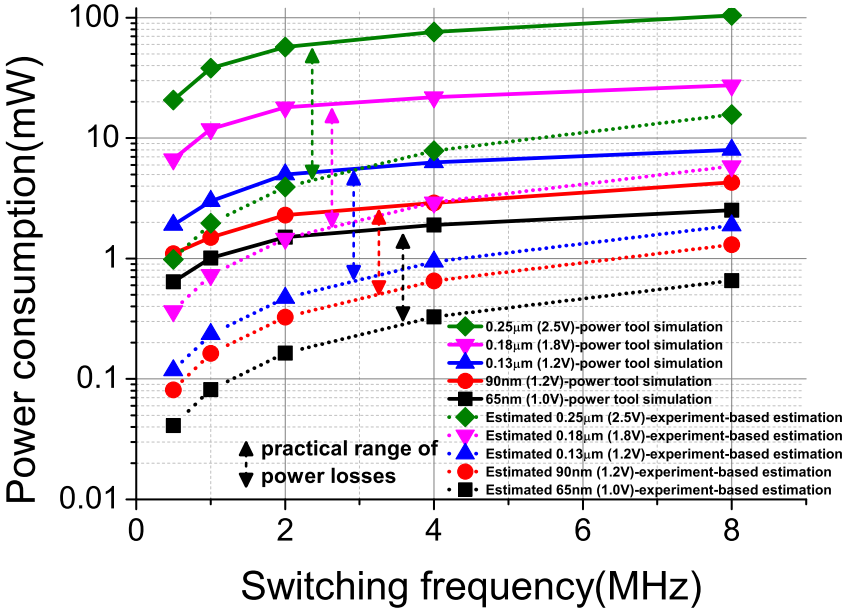


Figure 7.19: Practical range of power losses for the optimized SM controller for boost converter in 0.25μm, 0.18μm, 0.13μm, 90nm and 65nm CMOS process respectively using a dedicated power simulation tool and extrapolation from experimental data

7.2.4 A Discussion about the Power Consumptions of ADC and Necessary Peripherals

According to the experimental results, the power losses from the DPWM and controller in $0.35\mu m$ CMOS process are comparable to the analog counterpart. It even consumes less power in advanced CMOS technologies according to the proposed extrapolation approach. All above analyses do not take into account the power losses from ADC and other necessary peripherals. According to the arts reviewed in Chapter 1, the power consumption of the delay-line based and the Σ-Δ based ADCs can be restrained with in 100μA/MHz so that it only add a small additional part to the power consumption of the digital controller. The power consumption of the on-chip PLL is 4.5mW/MHz that is mainly contributed by the current-starved inverters. Some power-saving strategies and improvements will help to further reduce the PLL power losses to be more compatible with low-power design specification.

7.3 Summary

Two chips are discussed against power losses to exhibit the possible power efficiency of a SMPS with a digital controller compared to analog counterparts. Both simulation and experimental results are used to obtain practical ranges of power losses in advanced CMOS technologies. According to the analysis, the improved power-aware tri-mode and SM controllers appear good candidates with acceptable steady-state and transient-state performances, and with power losses similar or less than the analog ones when the feather size comes into deep sub-micro or nanometer and the switching frequency is limited to 10MHz. It may be concluded that SMPS of specific power capabilities and limited switching frequency can benefit from optimized digital controller to offer both

- better accuracy and flexibility;
- significant steady-state and transient-state performances;
- high efficiency.

Conclusion and Perspectives

Considering the development of modern semiconductor technology, it is possible to integrate all building blocks of a low-power DC-DC converter into a single chip including driver, power switch, passive component and controller. Accordingly, it accelerates the emergence of PwrSoC. Application covers the typical operations of battery-powered embedded system. As we get closer to PwrSoC prototypes, such a scaling of feature size is prone to improve the performances of controller from the viewpoint of digital designer. Digital control is therefore becoming a potentially attractive alternative to the analog counterpart. Compared to analog control, the digital approach is less sensitive to the external perturbations. Moreover digital control enables to implement more effective but complex control strategies to improve the dynamic performances. In addition, using available EDA tools, the design cycle of a digital controller can be accelerated. The verified digital controller code at RTL can be considered as an IP core that is reusable in different processes. However, the digital control for DC-DC converter at high switching frequency faces challenging issues. The increase in switching frequency leads to the scaling of passive components as well as the die size but results in additional losses. The research interest of the thesis is to explore practical ways of incorporating the advantages of digital control to a PwrSoC prototype while managing the energy issue. The thesis focuses on four main objectives including the high performance digital control-laws for low-power and high switching frequency SMPS, the analysis and optimization of DPWMs, the implementation of the digital controllers in FPGA and ASIC, a power assessment model of the power losses of digital controllers obtained from test chips to suggest feasible applications.

The contributions of the thesis are firstly summarized. Then the suggestions for further research are discussed as a perspective.

Contributions

Based on a literature review including the state of the art building blocks in the digital controller and the LCO effects, the thesis presents alternatives with respect to digital controller and DPWM to solve technical difficulties with respect to low-power, high switching frequency SMPS. These solutions are proposed to design a more effective digital controller leading to a regulated output with high energy efficiency. Two ASICs implement the digital controllers. The performances as well as the power losses are therefore evaluated to suggest possible applications of the digital prototypes compared to the analog counterparts.

The main contributions are

- An improved power-aware tri-mode control is proposed to achieve a trade-off between dynamic response and power losses. A robust RST control anticipates high dynamic performances and is performed in transient mode; a PID control is applied in steady-state mode; the same PID control tuned with appropriate parameters is clocked at a frequency lower than the switching frequency during stand-by mode;
- Digital PID and digital SM controllers for the boost converter are successfully designed and implemented in FPGA;
- DDP control is proposed for a high-switching frequency SMPS. The prediction of the inductor current and output voltage is performed at the same time by adding an additional control parameter to the DPWM signal that can dynamically adjust the time of the voltage events. The DDP controller preserves the merits of predictive current-mode control and allows to further enhance the dynamic performances while maintaining an excellent rejection to the power supply perturbations;
- An idle-tone detection function is presented to detect the idle-tone sensitive input binary word. The pre-verification results ensure an idle-tone free Σ-Δ DPWM;
- The proposed 1-1 DMASH DPWM takes the advantage of the noise-shaping concept and implements a MASH architecture, as well as combines a dither block in order to further eliminate the idle-tone effects;
- Embedded PLL on chip is designed to provide the clock sources for digital controllers;
- A testbench in VHDL-AMS is built to evaluate the performances of each digital controller during RTL simulation;
- A parameter read-in module is embedded into the controller to tune the parameters off-line. It guarantees a fine-tuning to offer a better rejection to perturbations, or a parameter import for higher switching frequency;
- The improved digital power-aware tri-mode controller IC for low-power, high switching frequency buck converter as well as the PID and SM controllers for buck converter and boost converter respectively are implemented in $0.35\mu m$ CMOS process;
- The control performances of implemented controllers are compared with respect to steady-state and transient-state performances;
- Based on the experimental results, the power losses of implemented controllers are evaluated to demonstrate an effective power model of target digital controllers. This model

helps to estimate the power losses of a digital controller, even suggests the power efficiency compared to analog counterpart under similar operating conditions.

Suggestions for Future Research

A few topics throughout this thesis can be extended and are worthwhile of future research as follows.

Current Estimation or Observation

The knowledge of current through passive components is a critical issue applied to the implemented controllers. Among available approaches, the on-chip sensor will introduce additional passive components and the derived analog building blocks. They will cause low power efficiency and unreliable performances due to the interferences between analog and digital modules [Man 07, Du 08]. It is beneficial to utilize solutions either based on the current variation prediction or on state observer. The current variation prediction, also known as current estimator, is a module that implements a certain algorithm based on known system variables [Foley 10, Lukic 09]. An observer, as an alternative, constructs a system model to be controlled, and observes state information from the model [Gensior 06, Luo 03, Midya 01].

Taking DDP control as an example, it is necessary to obtain the inductor current variation $\Delta I_L(k)$ over every switching period. An observer in [Gensior 06] to observe both the inductor current and load variation for the buck converter is adopted without success due to the convergence speed and the observability for load change. Moreover, it will occupy more hardware resource than the current estimators although a closed-loop observer guarantees the stability of each observed state variable. So in this thesis we use a current estimator derived from the output voltage derivation that is unstable potentially. However, more efforts should be paid to obtain an observer with satisfactory converge speed and acceptable complexity.

Current-limit Response in DDP Control

[Corradini 10] addresses an issue for significant inductor current overshoot during transient response, which may cause saturation of the inductor core and current over-stress of the electronic switches. The same situation may also occur in the proposed current-limit response in DDP control in response to a large load variation. A possible approach is to re-model the algorithm taking into account the inductor current limit issue. The state-space representation of the current-limit response expressed as the error voltage V_e versus capacitor current I_C can help to analyze the issue.

Robustness and Stability Issues

Robustness and stability issues of the implemented controllers are not discussed in this thesis. However, the robustness and stability of a control system are often extremely important and are

generally necessary conditions for dedicated controller. Further work can be focused on how to verify the robustness and prove the stability of implemented controllers, especially for the DDP control-law.

Application in DCM

A study of DCM operation in SMPS is very necessary in industrial application, and especially, it is urgently needed in some special electronics devices under the stand-by operation. In DCM operation, the transfer function of a SMPS is different from that in CCM which requires another SMPS model. In this thesis, all the implemented digital controllers operate in CCM, then it is very interesting to verify the digital controllers in DCM operation.

DDP Control On-chip for Other Power Converters

DDP control does not implement in ASIC in this thesis. It is interesting to compare the power consumption of DDP controller to other implemented controllers. The proposed DDP control is only implemented for the buck converter in this thesis. It is better to transplant this control to some non-minimum phase systems exhibiting more serious nonlinearity, such as the boost converter, in order to summarize a unified design approach of this control and to enrich the target DC-DC converters.

ADC Dedicated to Digital Controller

ADC plays an important role in digital controller with respect to steady-state error, output ripple value and LCO. The delay-cell-based ADCs are the trade-off to reduce power consumption to some extent, however, the resolution and precision require further tuning. Therefore, an appropriate method to implement the ADC dedicated to power controller is still a focus of study. In the further research, the delay-cell based ADC or other type of ADCs can be embedded into the chip to verify the performance of the controller with the aid of on-chip ADC in terms of static and dynamic performances, and power losses.

Implementation in Advanced CMOS Technologies

The test chips are implemented in $0.35\mu m$ CMOS process. Based on the simulation and experimental results, a power estimation model is obtained. Better extrapolation results are expected in advanced technologies. However, with the process scaling, especially in deep sub-micron and nanometer-level, the scaling based estimation will be influenced by the coupling effects. So the same controller in advance CMOS technologies, such as 65nm CMOS process, is suggested to be fabricated to validate or correct the power estimation model.

Digitally Controlled PwrSoC

The implemented ASIC prototypes are the controller part in a PwrSoC that is the ultimate target including not only the controllers but also the dedicated power converter. So many issues

are challenging, such as passive components compatible with PwrSoC, power devices and switches to enable PwrSoC, system architecture suitable for PwrSoC, etc. An acceptable compatibility of each part and a guaranteed stability of the PwrSoC should also be carefully considered. However, such configurable PwrSoC IP will change the traditional design of the power supply, and will bring about an increased attention on the semiconductor-driven platforms to design a re-useable power supply IP with target specifications for wide power range applications.

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Appendix A

State-space Models Dedicated to the Buck and Boost Converters

A.1 Hybrid, State-space Averaging, and Small Signal Models

A conventional way to describe the time domain behavior of a SMPS is the state space description. This represents the state of the SMPS at any time as a matrix operation. For the target converters, such as buck converter or boost converter, there are specific sets of state equations that will be discussed in this appendix. Firstly, a common state variable description of a system conforms to

$$\begin{cases} \dot{x} = Ax + Bu \\ y = C^T x + Du \end{cases} \tag{A.1}$$

For a switched mode converter in CCM, the two states are separately defined as

$$\begin{cases} \dot{x} = A_1 x + B_1 u \\ y = C_1^T x + D_1 u \end{cases} \tag{A.2}$$

$$\begin{cases} \dot{x} = A_2 x + B_2 u \\ y = C_2^T x + D_2 u \end{cases} \tag{A.3}$$

where (A.2) describing the switch closed-state, and (A.3) the switch open-state. The two equations precisely describe the switch states. It is a behavioral model so as to characterize the actual state variables. This is also the typical model adopted during target converter simulation.

In one switching period, if we define the duration of the close state as dT, while the open state as $(1-d)\,T$, an average model could be derived as

$$\begin{cases} \dot{\bar{x}} = \left[A_1 d + A_2 (1-d)\right] \bar{x} + \left[B_1 d + B_2 (1-d)\right] u = A(d)\,\bar{x} + B(d)\,u = f(\bar{x}, d, u) \\ \bar{y} = \left[C_1^T d + C_2^T (1-d)\right] \bar{x} + \left[D_1 d + D_2 (1-d)\right] u = C^T(d)\,\bar{x} + D(d)\,u = g(\bar{x}, d, u) \end{cases} \tag{A.4}$$

where

$$\begin{cases} A(d) = A_1 d + A_2(1-d) \\ B(d) = B_1 d + B_2(1-d) \\ C^T(d) = C_1^T d + C_1^T(1-d) \\ D(d) = D_1 d + D_2(1-d) \end{cases} \tag{A.5}$$

Average model is also the starting point to introduce the concept of small signal model which is a conventional approach to derive the control-to-output transfer function. Small signal is, as a matter of fact, just a limited perturbation in the vicinity of the steady-state operating point. So it obeys to

$$\begin{cases} x = X_0 + \hat{x} \\ d = D_0 + \hat{d} \\ u = U_0 + \hat{u} \\ y = Y_0 + \hat{y} \end{cases} \tag{A.6}$$

where X_0, D_0, U_0 and Y_0 represent the steady-state values, while $\hat{x}$, $\hat{d}$, $\hat{u}$, $\hat{y}$ represent small signal values. In steady state ($\dot{x}$), all the small signal values are considered to be zero. Therefore (A.2) can be expressed as

$$\begin{cases} 0 = A(D_0) X_0 + B(D_0) U_0 \\ Y_0 = C^T(D_0) X_0 + D(D_0) U_0 \end{cases} \tag{A.7}$$

(A.7) can be rewritten as

$$\begin{cases} X_0 = -A^{-1}(D_0) B(D_0) U_0 \\ Y_0 = \left[-C^T(D_0) A^{-1}(D_0) B(D_0) + D(D_0)\right] U_0 \end{cases} \tag{A.8}$$

A simple recognition about the state variable X in the steady-state is $\dot{X} = 0$, so $\dot{x} = \dot{X} + \dot{\hat{x}} = \dot{\hat{x}}$.

Around the operating point, the small signal model gives

$$\begin{cases} \dot{\hat{x}} = \left.\frac{\partial f}{\partial \hat{x}}\right|_{\substack{\hat{x}=X_0 \\ \hat{d}=D_0 \\ \hat{u}=U_0}} \cdot \hat{x} + \left.\frac{\partial f}{\partial \hat{d}}\right|_{\substack{\hat{x}=X_0 \\ \hat{d}=D_0 \\ \hat{u}=U_0}} \cdot \hat{d} + \left.\frac{\partial f}{\partial \hat{u}}\right|_{\substack{\hat{x}=X_0 \\ \hat{d}=D_0 \\ \hat{u}=U_0}} \cdot \hat{u} = A_l \hat{x} + B_l \hat{d} + P_l \hat{u} \\ \hat{y} = \left.\frac{\partial g}{\partial \hat{x}}\right|_{\substack{\hat{x}=X_0 \\ \hat{d}=D_0 \\ \hat{u}=U_0}} \cdot \hat{x} + \left.\frac{\partial g}{\partial \hat{d}}\right|_{\substack{\hat{x}=X_0 \\ \hat{d}=D_0 \\ \hat{u}=U_0}} \cdot \hat{d} + \left.\frac{\partial g}{\partial \hat{u}}\right|_{\substack{\hat{x}=X_0 \\ \hat{d}=D_0 \\ \hat{u}=U_0}} \cdot \hat{u} = C_l \hat{x} + D_l \hat{d} + Q_l \hat{u} \end{cases} \tag{A.9}$$

where

$$\begin{cases} A_l = [A_1 D_0 + A_2(1-D_0)] \\ B_l = [(A_1 - A_2) X_0 + (B_1 - B_2) U_0] \\ P_l = [B_1 D_0 + B_2(1-D_0)] \end{cases} \tag{A.10}$$

$$\begin{cases} C_l = \left[C_1^T D_0 + C_2^T(1-D_0)\right] \\ D_l = \left[\left(C_1^T - C_2^T\right) X_0 + (D_1 - D_2) U_0\right] \\ Q_l = [D_1 D_0 + D_2(1-D_0)] \end{cases} \tag{A.11}$$

If the input is assumed to be constant ($\hat{u} = 0$), then the small signal output value as shown in (A.9), (A.10) and (A.11) is synthesized as

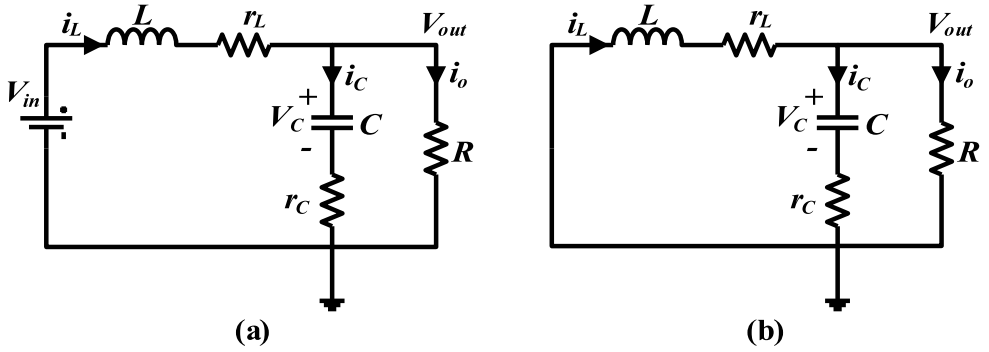


Figure A.1: Buck converter topologies in CCM to derive the corresponding state equations (a) closed-switch, (b) open-switch

$$\begin{cases} \dot{\hat{x}} = \left[A_1 D_0 + A_2 \left(1 - D_0\right)\right] \hat{x} + \left[\left(A_1 - A_2\right) X_0 + \left(B_1 - B_2\right) U_0\right] \hat{d} \\ \hat{y} = \left[C_1^T D_0 + C_2^T \left(1 - D_0\right)\right] \hat{x} + \left[\left(C_1^T - C_2^T\right) X_0 + \left(D_1 - D_2\right) U_0\right] \hat{d} \end{cases} \tag{A.12}$$

A.2 State-space Averaging for the Buck and Boost Converters

As aforementioned in Section A.1, the state-space averaging is a feasible approach to develop the transfer function for switching mode circuits. Based on the hybrid model, this section will adopt the state-space averaging method to derive the control-to-output transfer function so as to design an acceptable PID controller. Both the buck and boost converters in CCM are involved here as target inverters.

A.2.1 Derivations for the Buck Converter

Fig. A.1 shows the buck converter topologies in CCM. It is the starting point to reveal the transfer function.

According to the definition in (A.1), we assume that the variation of the load R is very slow, in other words, in a switching period, R is considered as a constant. The state vector x, the input vector u and the output variable y are represented as

$$x = \begin{bmatrix} i_L \\ V_C \end{bmatrix}, u = V_{in}, y = V_{out} \tag{A.13}$$

In the closed-switch condition, the state matrixes are

$$A_1 = \begin{bmatrix} -\dfrac{\left(R + r_L\right) r_C + R r_L}{\left(R + r_C\right) L} & -\dfrac{R}{\left(R + r_C\right) L} \\ \dfrac{R}{C\left(R + r_C\right)} & -\dfrac{1}{C\left(R + r_C\right)} \end{bmatrix}, B_1 = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}, C_1^T = \begin{bmatrix} \dfrac{R r_C}{R + r_C} & \dfrac{R}{R + r_C} \end{bmatrix}, D_1 = 0 \tag{A.14}$$

While in open-switch condition, the state matrixes are

$$A_2 = A_1, B_2 = 0, C_2^T = C_1^T, D_2 = 0 \tag{A.15}$$

Based on (A.5), the average model of the state matrixes is therefore

$$\begin{cases} A = A_1 D_0 + A_2 (1 - D_0) = A_1 \\ B = B_1 D_0 + B_2 (1 - D_0) = \begin{bmatrix} \frac{D_0}{L} \\ 0 \end{bmatrix} \\ C^T = C_1^T D_0 + C_2^T (1 - D_0) = \begin{bmatrix} \frac{R r_C}{R + r_C} & \frac{R}{R + r_C} \end{bmatrix} = C_1^T \end{cases} \tag{A.16}$$

According to (A.8), the steady-state output can be expressed as

$$V_{out} = -C^T A^{-1} B V_{in} = \frac{RD}{R + r_L} V_{in} \tag{A.17}$$

If r_L is considered as null, then (A.17) can be rewritten as

$$V_{out} = D V_{in} \tag{A.18}$$

Given (A.12), we can derive the states equation of the small signal model as

$$\begin{cases} \dot{\hat{x}} = A\hat{x} + B_1 U \hat{d} \\ \hat{y} = C^T \hat{x} \end{cases} \tag{A.19}$$

Considering the system, the Laplace transform gives

$$s\hat{x}(s) = A\hat{x}(s) + B_1 V_{in} \hat{d}(s) \tag{A.20}$$

Computation of $\hat{x}(s)$ yields

$$\hat{x}(s) = [sI - A]^{-1} B_1 V_{in} \hat{d}(s) \tag{A.21}$$

Reconsidering (A.19) and (A.21), the small signal output $\hat{y}$, here replaced by $\hat{V}_{out}(s)$, conforms to

$$\hat{V}_{out}(s) = C^T \hat{x}(s) = C^T [sI - A]^{-1} B_1 V_{in} \hat{d}(s) \tag{A.22}$$

So the transfer function of output-to-control can be expressed as

$$\begin{aligned} \frac{\hat{V}_{out}(s)}{\hat{d}(s)} &= C^T [sI - A]^{-1} B_1 V_{in} \\ &= \frac{(s r_C C + 1) V_{in}}{s^2 \left(1 + \frac{r_c}{R}\right) LC + s \left((r_C + r_L) C + \frac{r_L r_C C}{R} + \frac{L}{R} \right) + \frac{R_L}{R} + 1} \end{aligned} \tag{A.23}$$

A.2.2 Derivations for the Boost Converter

Fig. A.2 shows the boost converter topologies in CCM. It is the starting point to reveal the transfer function.

According to the definition in (A.1), we assume that the variation of the load R is very slow, in other words, in a switching period, R is considered as a constant. The state vector x, the input vector u and the output variable y is represented as

$$x = \begin{bmatrix} i_L \\ V_C \end{bmatrix}, u = V_{in}, y = V_{out} \tag{A.24}$$

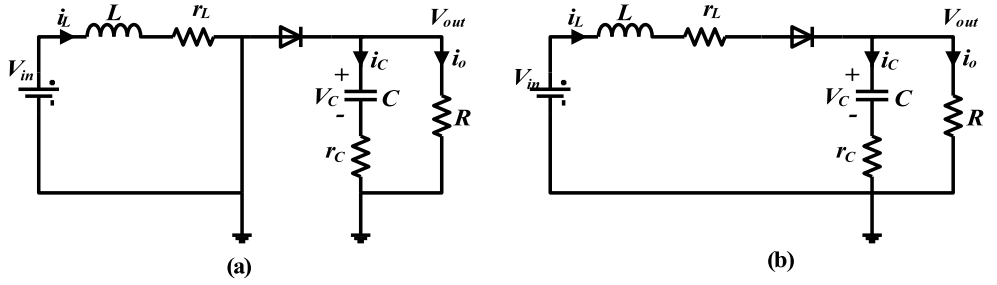


Figure A.2: Boost converter topologies in CCM to derive the corresponding state equations (a) closed-switch, (b) open-switch

In the closed-switch condition, the state matrixes are

$$A_1 = \begin{bmatrix} -\frac{r_L}{L} & 0 \\ 0 & -\frac{1}{C\left(R+r_C\right)} \end{bmatrix}, B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}, C_1^T = \begin{bmatrix} 0 & \frac{R}{R+r_C} \end{bmatrix}, D_1 = 0 \tag{A.25}$$

While in open-switch condition, the state matrixes are

$$A_2 = \begin{bmatrix} -\frac{\left(R+r_L\right)r_C + Rr_L}{\left(R+r_C\right)L} & -\frac{R}{\left(R+r_C\right)L} \\ \frac{R}{C\left(R+r_C\right)} & -\frac{1}{C\left(R+r_C\right)} \end{bmatrix}, B_2 = B_1, C_2^T = \begin{bmatrix} \frac{Rr_C}{R+r_C} & \frac{R}{R+r_C} \end{bmatrix}, D_2 = 0 \tag{A.26}$$

Based on (A.5), the average model of the state matrixes is therefore

$$\begin{cases} A = A_1 D + A_2\left(1-D\right) = \begin{bmatrix} -\frac{Rr_C\left(D-1\right) - r_C\left(R+r_C\right)}{\left(R+r_C\right)L} & -\frac{R}{\left(R+r_C\right)L} \\ \frac{R\left(1-D\right)}{C\left(R+r_C\right)} & -\frac{1}{C\left(R+r_C\right)} \end{bmatrix} \\ B = B_1 D + B_2\left(1-D\right) = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \\ C^T = C_1^T D + C_2^T\left(1-D\right) = \begin{bmatrix} \frac{Rr_C\left(1-D\right)}{R+r_C} & \frac{R}{R+r_C} \end{bmatrix} \end{cases} \tag{A.27}$$

According to (A.8), the steady-state output can be expressed as

$$V_{out} = -C^T A^{-1} B V_{in} = \frac{R\left(1-D\right)\left(R+r_C\right)}{Rr_C\left(1-D\right) + r_L\left(r_C+R\right) + \left(1-D\right)^2 R^2} V_{in} \tag{A.28}$$

Only under the assumption that both r_L and r_C are null, (A.28) can be rewritten as

$$V_{out} = \frac{1}{1-D} V_{in} \tag{A.29}$$

Given (A.12), we can derive the small signal model as

$$\begin{cases} \dot{\hat{x}} = A\hat{x} + (A_1 - A_2) X_0 \cdot \hat{d} \\ \hat{y} = C^T \hat{x} + \left(C_1^T - C_2^T\right) X_0 \cdot \hat{d} \end{cases} \tag{A.30}$$

where

$$A_1 - A_2 = \begin{bmatrix} \dfrac{Rr_C}{(R + r_C) L} & \dfrac{R}{(R + r_C) L} \\ -\dfrac{R}{C (R + r_C)} & 0 \end{bmatrix} \tag{A.31}$$

$$C_1^T - C_2^T = \begin{bmatrix} -\dfrac{Rr_C}{R + r_C} & 0 \end{bmatrix} \tag{A.32}$$

$$X_0 = \begin{bmatrix} \dfrac{(R + r_C) V_{in}}{Rr_C (1 - D) + r_L (R + r_C) + R^2 (1 - D)^2} \\ \dfrac{(1 - D) (R + r_C) R V_{in}}{Rr_C (1 - D) + r_L (R + r_C) + R^2 (1 - D)^2} \end{bmatrix} \tag{A.33}$$

Considering the system, the Laplace transform is

$$s\hat{x}(s) = A\hat{x}(s) + (A_1 - A_2) X_0 \hat{d}(s) \tag{A.34}$$

Computation of $\hat{x}(s)$ yields

$$\hat{x}(s) = [sI - A]^{-1} (A_1 - A_2) X_0 \hat{d}(s) \tag{A.35}$$

Reconsidering (A.30) and (A.35), the small signal output $\hat{y}$, here replaced by $\hat{V}_{out}(s)$, conforms to

$$\begin{aligned} \hat{V}_{out}(s) &= C^T \hat{x} + \left(C_1^T - C_2^T\right) X_0 \cdot \hat{d} \\ &= C^T [sI - A]^{-1} (A_1 - A_2) X_0 \hat{d}(s) + \left(C_1^T - C_2^T\right) X_0 \hat{d}(s) \end{aligned} \tag{A.36}$$

So the transfer function of output-to-control can be expressed as

$$\frac{\hat{V}_{out}(s)}{\hat{d}(s)} = C^T [sI - A]^{-1} (A_1 - A_2) X_0 + \left(C_1^T - C_2^T\right) X_0 \tag{A.37}$$

Since the expression of transfer function in (A.37) is too complicated, it can be obtained by modeling software such as Matlab.

Appendix B

ASIC Testbench

B.1 Packaged Chip and Pin Configuration

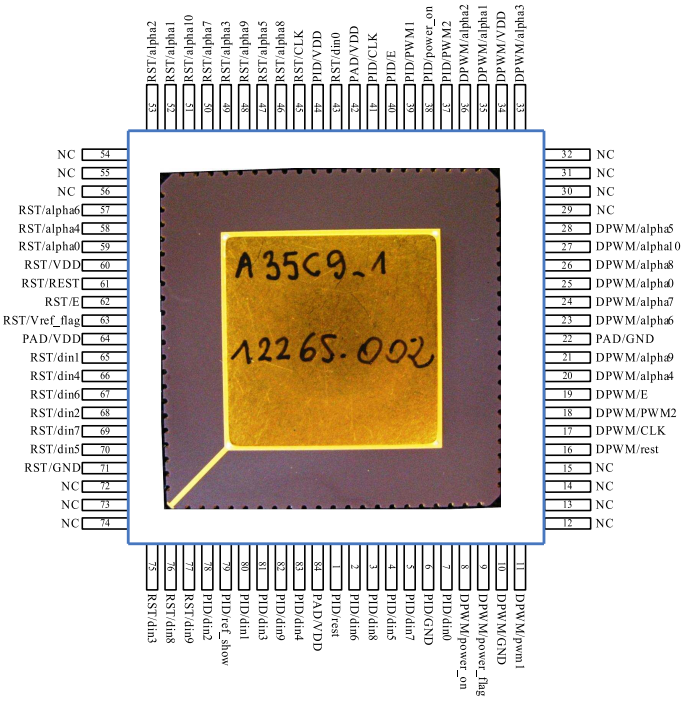


Figure B.1: Pin definition and packaged chip of the first chip

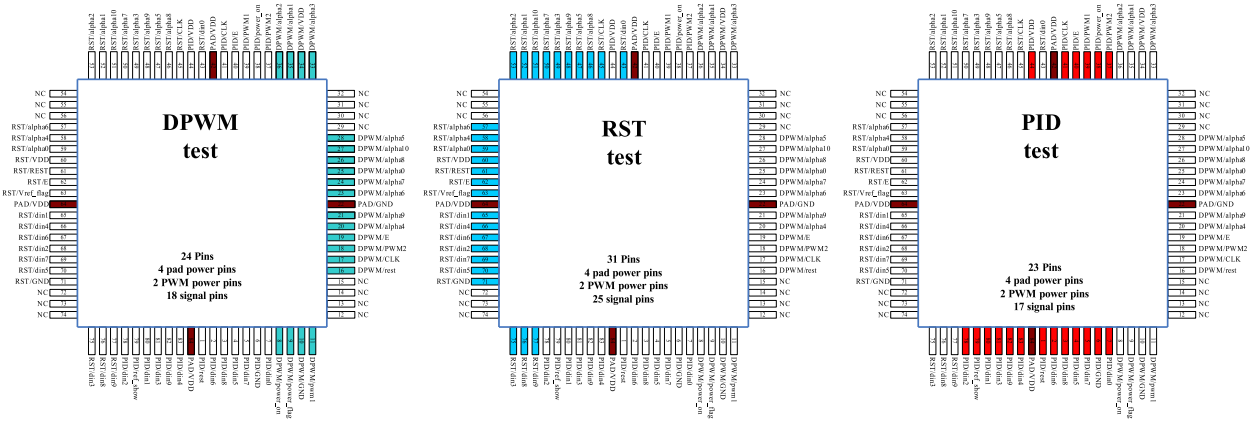


Figure B.2: Pin configuration of each test

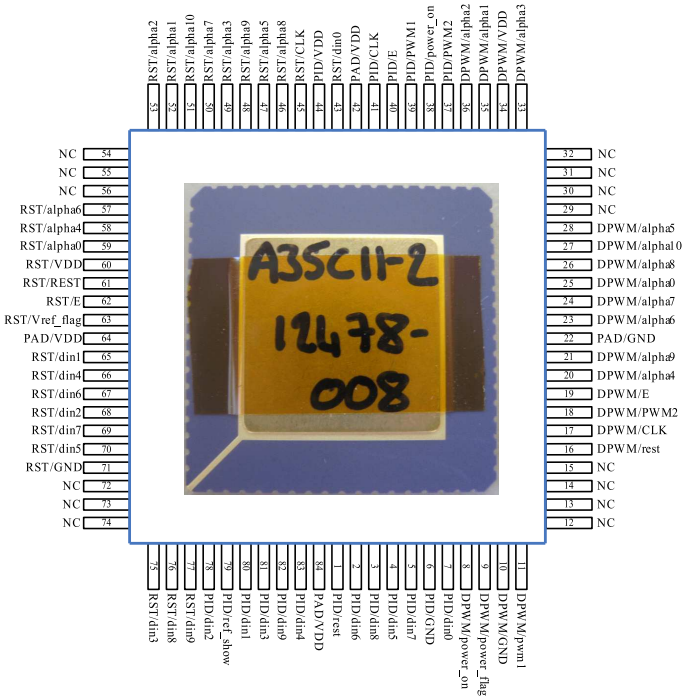


Figure B.3: Pin definition and packaged chip of the second chip

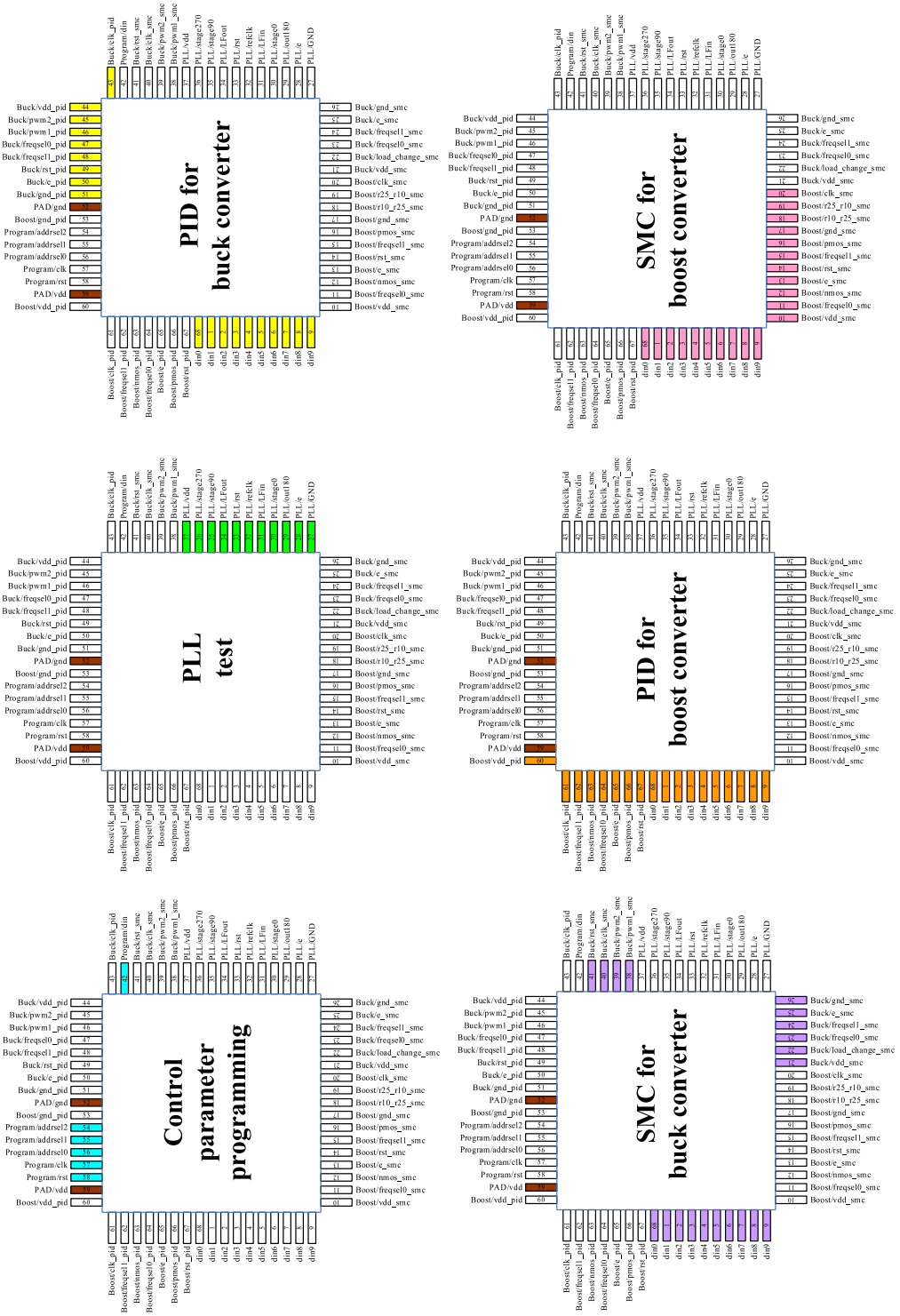


Figure B.4: Pin configuration of the second ASIC test

B.2 Testbech of the First Chip

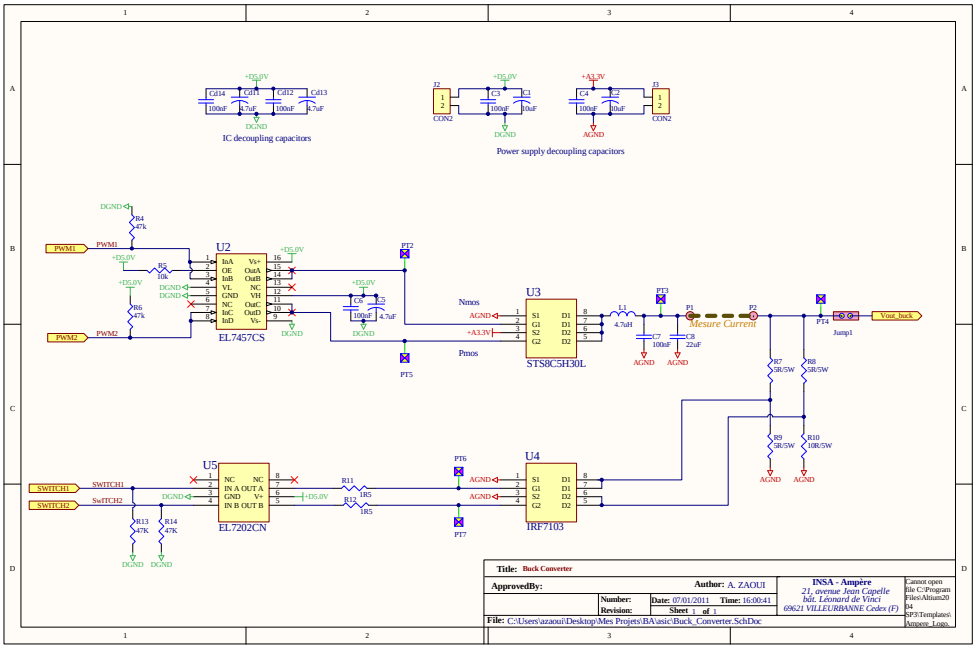


Figure B.5: Buck converter under test

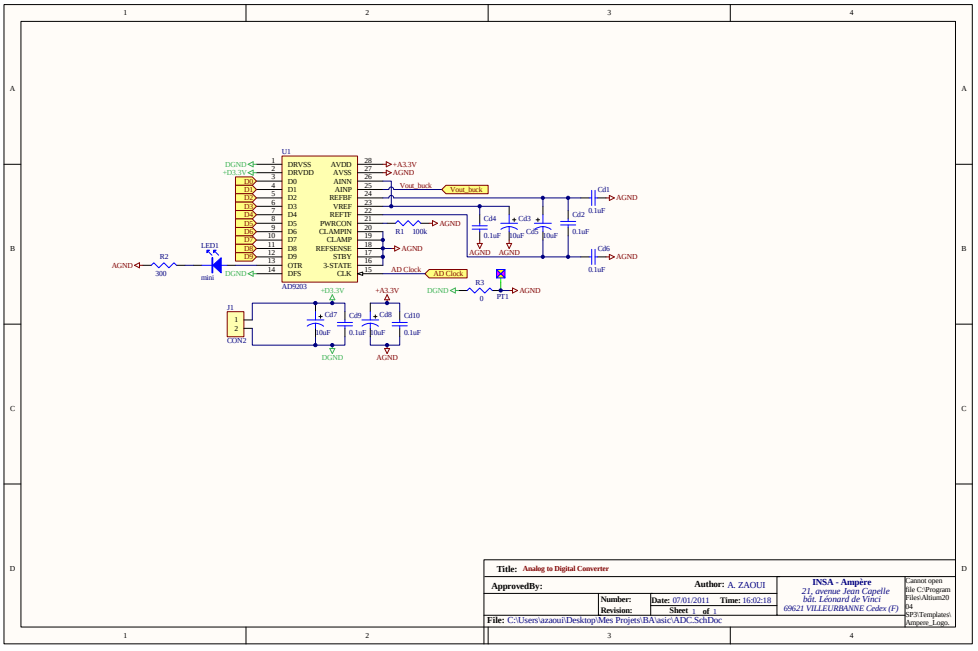


Figure B.6: ADC as output quantizer

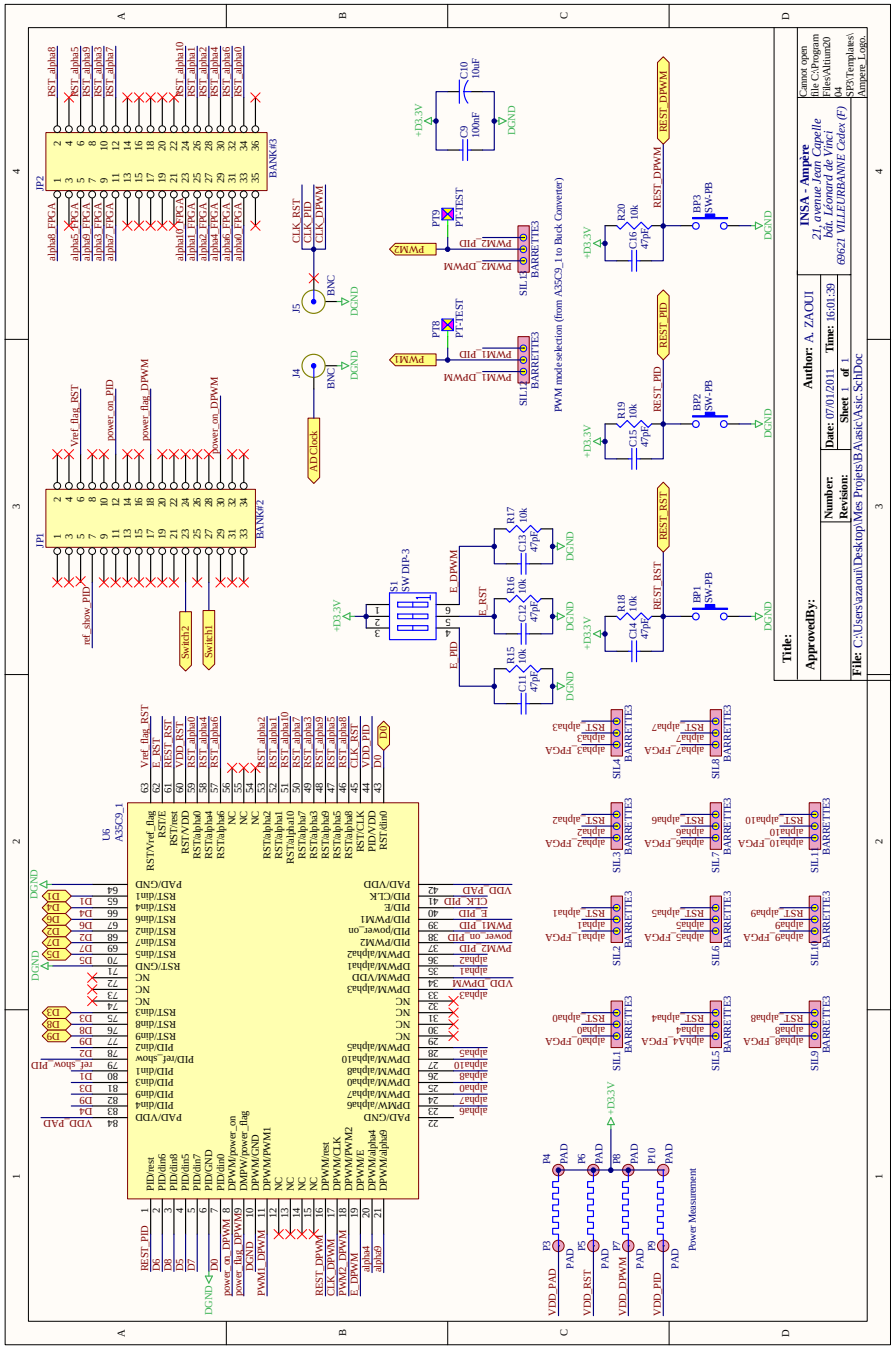


Figure B.7: Target controller ASIC and its configurations

B.3 Testbech of the Second Chip

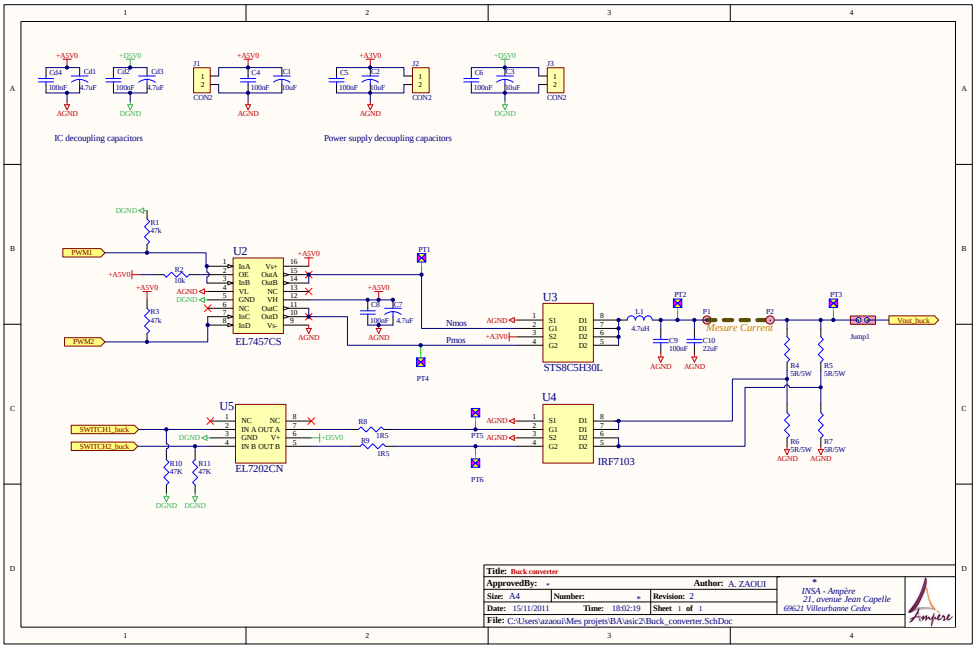


Figure B.8: Buck converter under test

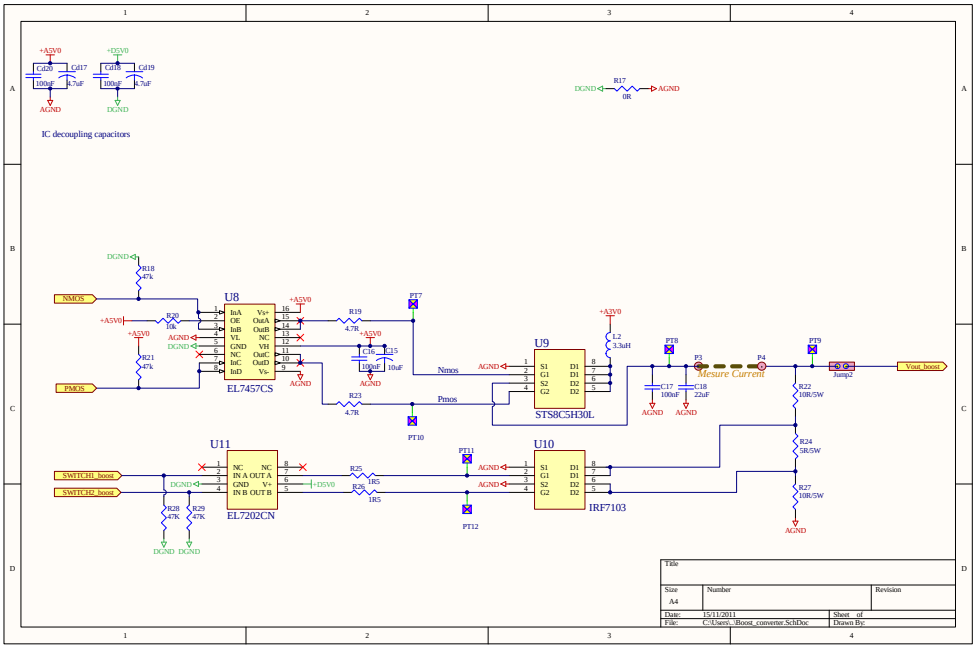


Figure B.9: Boost converter under test

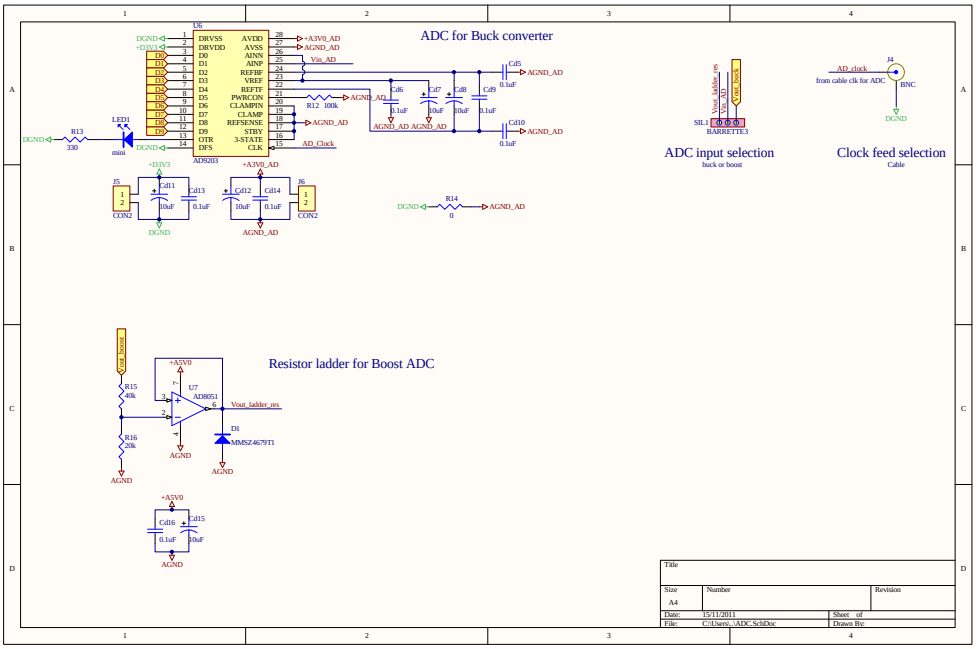


Figure B.10: ADC as output quantizer

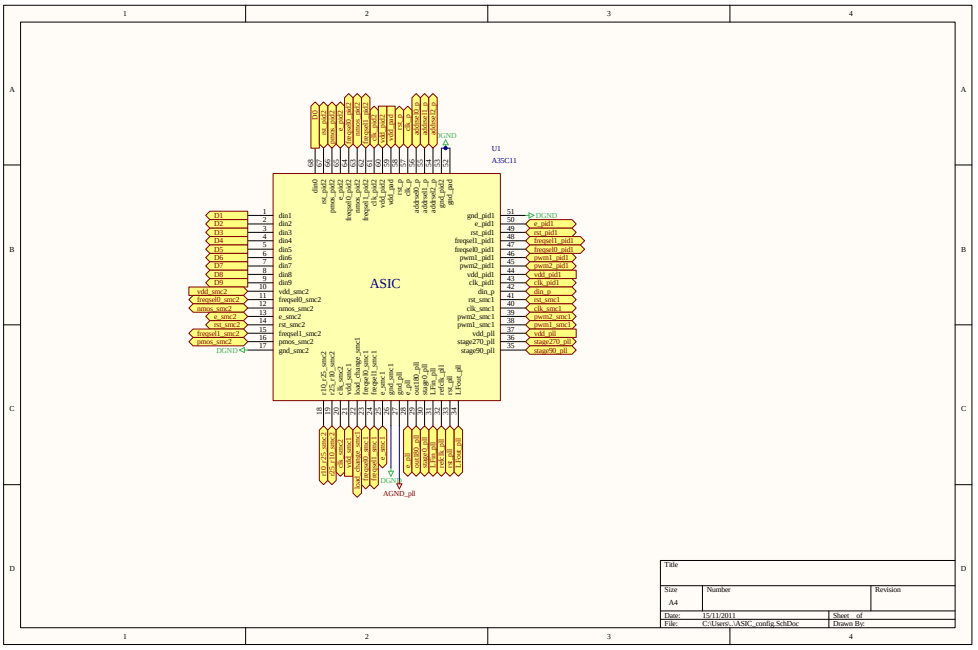


Figure B.11: Target controller ASIC

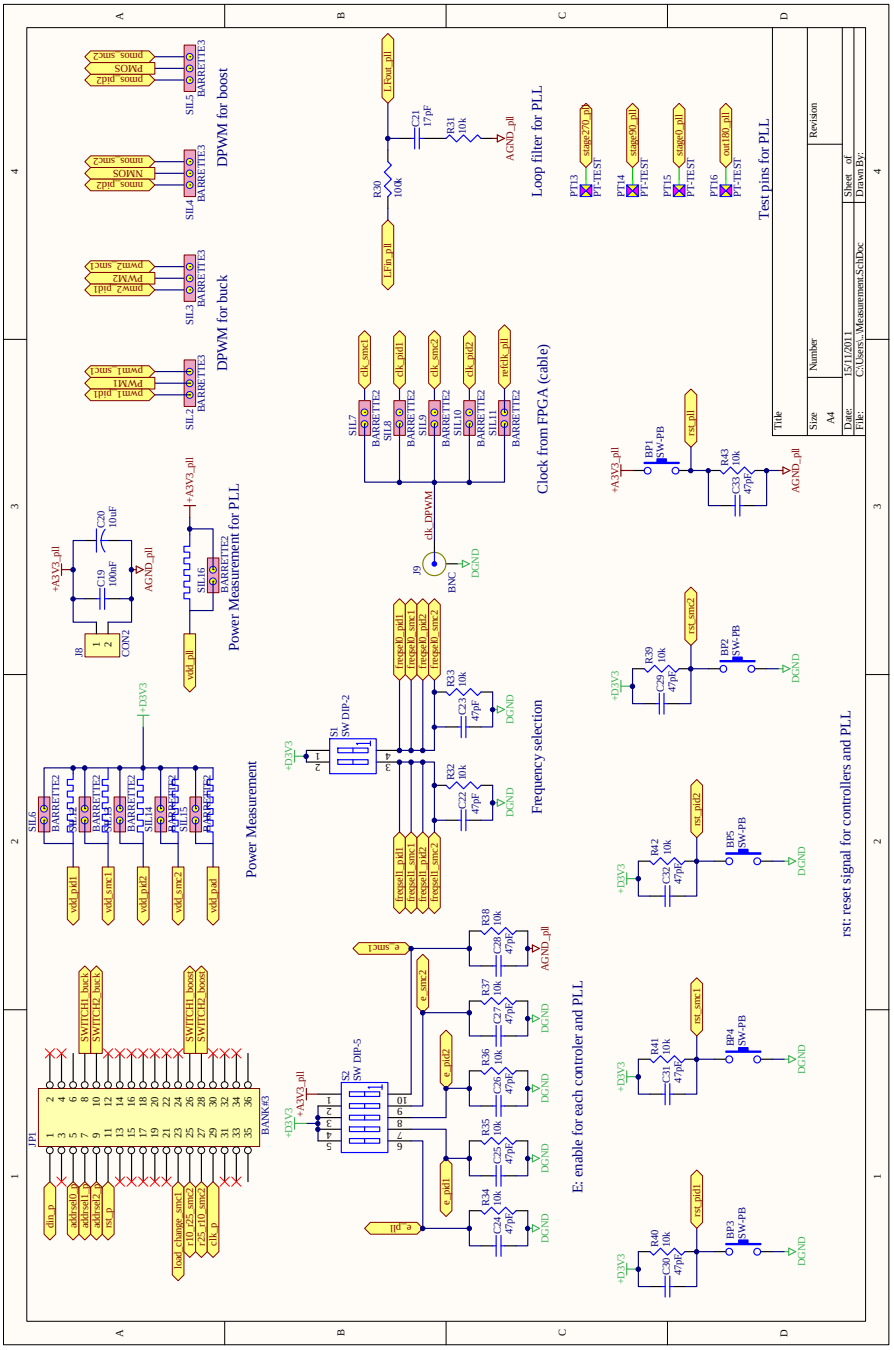
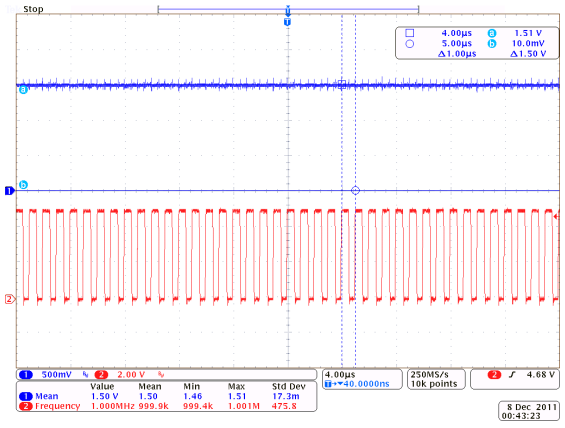


Figure B.12: Test configurations

Appendix C

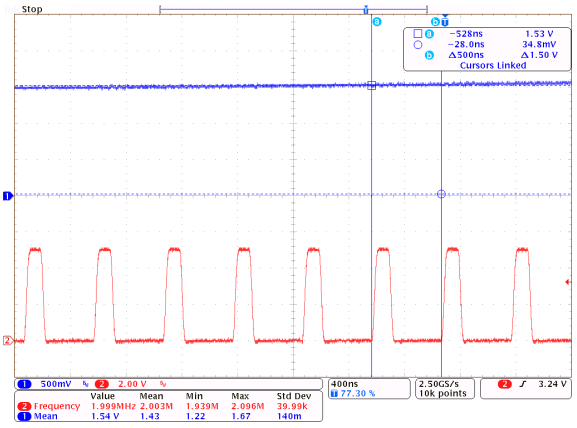
Complementary Experimental Results



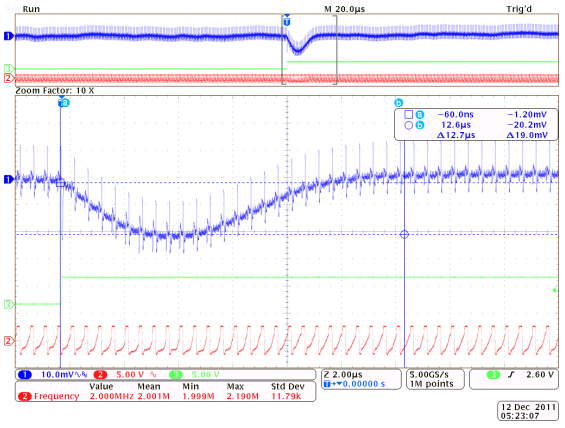
(a)

(b)

Figure C.1: SM controller for the buck converter: (a) steady state operating at 1MHz, (b) load transients from 0.3A to 0.45A (R: from 5Ω to 3.3Ω)



(a)



(b)

Figure C.2: SM control for the buck converter: (a) steady state operating at 2MHz, (b) load transients from 0.3A to 0.45A (R: from 5Ω to 3.3Ω)

Appendix D

An Example of RTL to Layout Design Flow

An example of RTL to layout design flow is introduced in this appendix. AMS design HIT-KIT v3.70 is adopted as the technology file. C35B4C3 is chosen as the premier technology during the whole design. There are some effective tools from the design-kit to accelerate the design process. We will make a brief introduction to two most important steps: synthesis and place & route. The second-order DPWM code is used here to be synthesized and then implemented into a layout prototype. Fig. D.1 shows the building blocks of the dedicated DPWM.

The following tools are used to complete the design and verification task

- Modesim ver5.8c-Mentor
- Buildgates ver05.17-Cadence
- Encounter ver6.2-Cadence
- IC ver5.1.41-Cadence
- Assura ver5.1.41-Cadence
- Spectre -Cadence

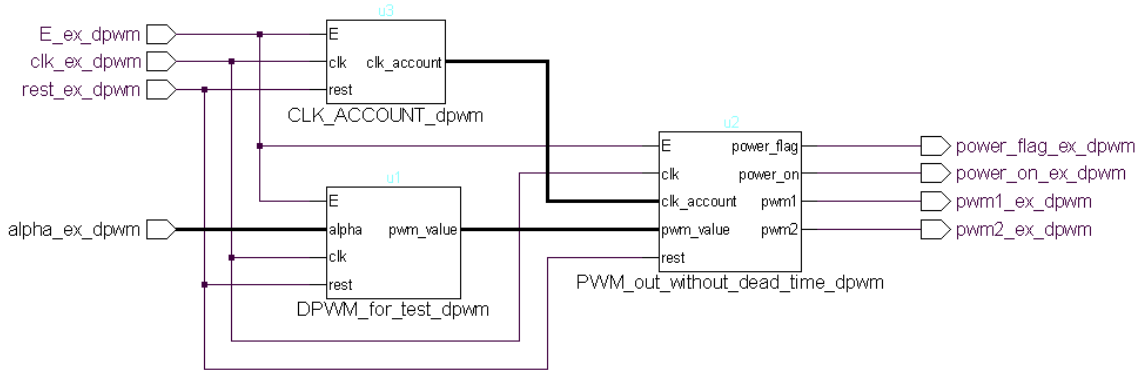


Figure D.1: Building blocks of the dedicated DPWM

D.1 Script-based Logic Synthesis Using $Buildgates$

This is a general flow to synthesis a RTL VHDL program into a gate-level netlist.
– Launch $Buildgates$;
– Environment setup;
– Import library;
– Import RTL VHDL code;
– Build generic design;
– Timing and physical constraints;
– Optimize design;
– Netlist and report generation.

Launch $Buildgates$
pks_shell -gui &
Environment setup
set_global echo_commands true
set_global fanout_load_limit 12
Import library
read_tlf $AMS_DIR/buildgates/c35_3.3V/c35_CORELIB.tlf
read_tlf $AMS_DIR/buildgates/c35_3.3V/c35_IOLIB_4M.tlf
read_symbol $AMS_DIR/buildgates/c35_3.3V/c35_CORELIB.sym
read_symbol $AMS_DIR/buildgates/c35_3.3V/c35_IOLIB_4M.sym
Set possible operating conditions
set_operating_condition -library c35_CORELIB WORST-MIL -pvt max
set_operating_condition -library c35_CORELIB BEST-MIL -pvt min
set_operating_condition -library c35_CORELIB TYPICAL -pvt typ
Set the global variables
set timing analysis mode
set_global timing_analysis_type bc_wc
set_global pvt_early_path min
set_global pvt_late_path max
set target technology
set_global target_technology {c35_CORELIB c35_IOLIB_4M}
set_global use_lef_area false
set_global fix_multiport_nets true
##for proper SDF
set_global lib_build_asynch_arc true
set_global lib_build_asynch_de_assert_arc true
Import RTL VHDL code
read_vhdl ./PWM_out_without_dead_time_dpwm.vhd
read_vhdl ./DPWM_for_test_dpwm.vhd
read_vhdl ./CLK_ACCOUNT_dpwm.vhd
read_vhdl ./top_dpwm_dpwm.vhd
Build generic design
do_build_generic -all -extract_fsm
save database for reuse
write_adb -hier netlist/top_dpwm_dpwm_presyn.adb
Timing constraints
##set up hierarchical context and timing context
set_current_module top_dpwm_dpwm

set_top_timing_module top_dpwm_dpwm
source ports
proc all_inputs {} {find -port -input -noclocks ""}*
proc all_outputs {} {find -port -output ""}*
##ideal clock definition
set_clock refclk -period 10.0 -wave {0 5.0}
##associate ideal clock with actual clock pin
set_clock_root -clock refclk {clk_ex_dpwm}
##define the delay between ideal clock and actual clock signal
set_clock_insertion_delay -source 0.2 -pin {clk_ex_dpwm}
##define early and late arrivals of a signal
set_input_delay -clock refclk -early 0.6 [all_inputs]
set_input_delay -clock refclk -late 1.0 [all_inputs]
##define external delay at an output port
set_external_delay -clock refclk -early 0.6 [all_outputs]
set_external_delay -clock refclk -late 1.0 [all_outputs]

Physical constraints

set number of external sources and sink
set_num_external_sources 5 [all_inputs]
set_num_external_sinks 5 [all_outputs]
set port capacitance
set_drive_cell -cell INV0 [all_inputs]
set_drive_cell -cell INV0 {clk_ex_dpwm}
set val [expr 10[get_cell_pin_load -cell INV0 -pin A]]*
set_port_capacitance $val [all_inputs]
set_port_capacitance $val [all_outputs]
set_port_capacitance $val {clk_ex_dpwm}
set drive resistance
*set_drive_resistance 0 [find -port -input *]*

Optimization and generation of netlist and report

##Optimize Design to AMS technology
do_optimize -effort high -flatten auto -time_budget -priority time
check_timing
check_netlist
##Generate Reports
report_timing > report/timing.rpt
report_area -hier -cell > report/area.rpt
report_hierarchy > report/hierarchy.rpt
report_power > report/power.rpt
##Save final Netlist
##export gate-level netlist for gate-level simulation and place & route
write_verilog -hier netlist/top_dpwm_dpwm_syn.v
##export post-synthesis timing data SDF including gate delays information
write_sdf netlist/top_dpwm_dpwm_syn.sdf
##export constraints in SDC format for place and route
write_sdc netlist/top_dpwm_dpwm_syn.sdc
##export ADB database for reuse
write_adb -hier netlist/top_dpwm_dpwm_syn.adb

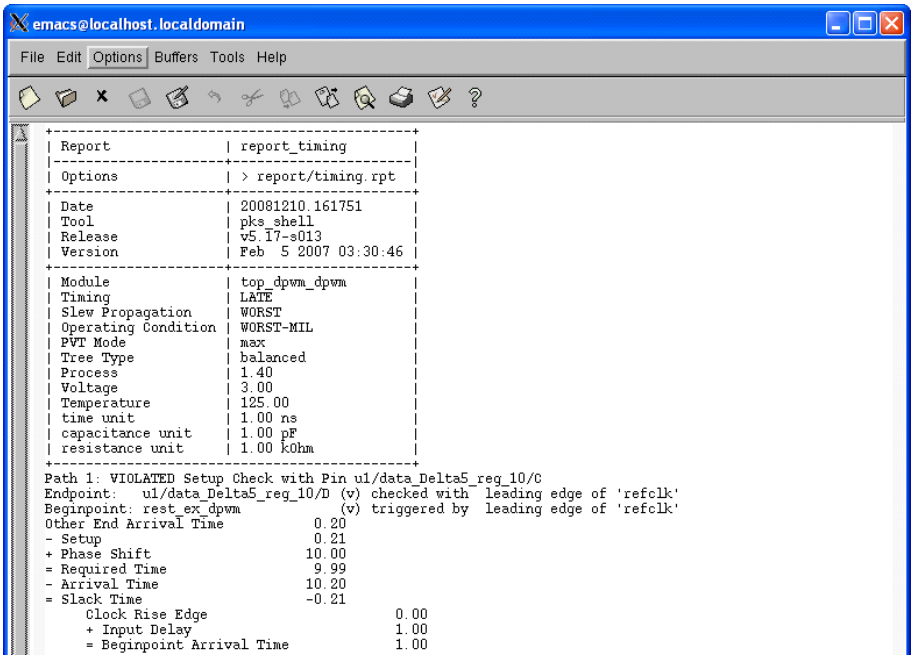


Figure D.2: Timing report after synthesis

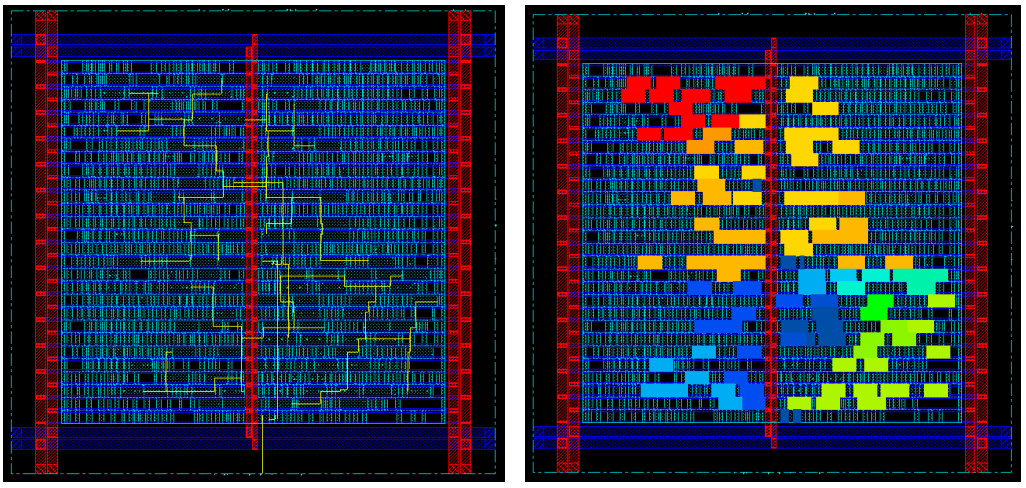
Then the reports files can be open to check area, power, hierarchy and timing characteristics as shown in Fig. D.2.

D.2 Place & Route Using *Encounter*

This is a general flow to place & route a gate-level netlist to a layout view.

– Initializing design kit
– Design import
– Connect/Define global net
– Timing analysis–>pre-placement
– CAP cell placement
– Floorplan
– Powerplan
– Place standard cells
– Timing analysis–>post-placement (IPO)
– Clock tree synthesis (CTS)
– Timing analysis–>post-CTS (IPO)
– SRoute
– NanoRoute
– Timing analysis–>post-route (IPO)
– Add core filler
– Verification
– Export data

Fig. D.3 shows the CTS analysis results. The final place & route view is shown in Fig. D.4.



(a) (b)

Figure D.3: (a) Display clock tree after CTS, (b) Display clock phase delay after CTS

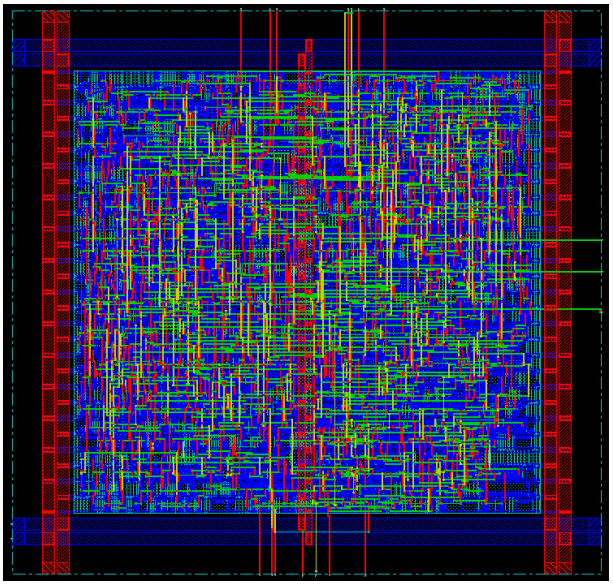


Figure D.4: Post-place-and-route layout view

FOLIO ADMINISTRATIF
THÈSE SOUTENUE DEVANT L'INSTITUT NATIONAL DES SCIENCES APPLIQUÉES DE LYON

NOM : LI **DATE DE SOUTENANCE** : 07/05/12
PRÉNOM : Bo

TITRE : Conception et test de cellules de gestion d'énergie à commande numérique en technologies CMOS avancées.

NATURE : Doctorat **NUMÉRO D'ORDRE** : 2012-ISAL-0036
ECOLE DOCTORALE : **E.E.A.** Électronique, Électrotechnique, Automatique.
SPÉCIALITÉ : Electronique de puissance et Automatique

RÉSUMÉ :
Les technologies avancées de semi-conducteur permettent de mettre en œuvre un contrôleur numérique dédié aux convertisseurs à découpage, de faible puissance et de fréquence de découpage élevée sur FPGA et ASIC. Cette thèse vise à proposer des contrôleurs numériques des performances élevées, de faible consommation énergétique et qui peuvent être implémentés facilement.
En plus des contrôleurs numériques existants comme PID, RST, tri-mode et par mode de glissement, un nouveau contrôleur numérique (DDP) pour le convertisseur abaisseur de tension est proposé sur le principe de la commande prédictive: il introduit une nouvelle variable de contrôle qui est la position de la largeur d'impulsion permettant de contrôler de façon simultanée le courant dans l'inductance et la tension de sortie. La solution permet une dynamique très rapide en transitoire, aussi bien pour la variation de la charge que pour les changements de tension de référence. Les résultats expérimentaux sur FPGA vérifient les performances de ce contrôleur jusqu'à la fréquence de découpage de 4MHz. Les comparaisons avec les commandes PID, RST et par mode de glissement montrent que le contrôleur DDP présente un meilleur compromis entre la complexité algorithmique et les performances.
Pour le convertisseur élévateur de tension où la présence de non linéarité est importante, un contrôleur PID linéaire et un contrôleur par mode de glissement non linéaire sont conçus et mis en œuvre sur FPGA afin de vérifier leur performance. Un contrôleur numérique nécessite une modulation numérique de largeur d'impulsion (DPWM). L'approche Σ-Δ de la DPWM est un bon candidat en ce qui concerne le compromis entre la complexité et les performances. Un guide de conception d'étage Σ-Δ pour le DPWM est présenté. Une architecture améliorée de architectures traditionnelles 1-1 MASH Σ-Δ DPWM est synthétisée sans détérioration de la stabilité en boucle fermée ainsi qu'en préservant un coût raisonnable en ressources matérielles. Les résultats expérimentaux sur FPGA vérifient les performances des DPWM proposées en régimes stationnaire et transitoire.
Deux ASICs sont portés en CMOS 0,35μm: le contrôleur en tri-mode pour le convertisseur abaisseur de tension et la commande par mode de glissement pour les convertisseurs abaisseur et élévateur de tension. Les bancs de test sont conçus pour conduire à un modèle d'évaluation de consommation énergétique. Pour le contrôleur en tri-mode, la consommation de puissance mesurée est seulement de 24,56mW/MHz lorsque le ratio de temps en régime de repos (stand-by) est 0,7. Les consommations de puissance de commande par mode de glissement pour les convertisseurs abaisseur et élévateur de tension sont respectivement de 4,46mW/MHz et 4,79mW/MHz. En utilisant le modèle de puissance, une consommation de la puissance estimée inférieure à 1mW/MHz est envisageable dans des technologies CMOS plus avancées. Comparé aux contrôlés homologues analogiques de l'état de l'art, les prototypes ASICs illustrent la possibilité d'atteindre un rendement comparable pour les applications de faible et de moyen puissance mais avec l'avantage d'une meilleure précision et une meilleure flexibilité.

MOTS-CLÉS : SMPS, DC-DC converter, predictive control, digital control, DPWM, PwrSoC.

LABORATOIRE DE RECHERCHES :
Laboratoire AMPERE - UMR CNRS 5005

DIRECTEURS DE THÈSE : ALLARD Bruno, LIN-SHI Xuefang.

PRÉSIDENT DU JURY : HEBRARD Luc
COMPOSITION DU JURY : ALLARD Bruno, CIRSTEA Marcian, HEBRARD Luc, LI Zheying, LIN-SHI Xuefang, MONMASSON Eric, TROCHUT Séverin.