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High-performance cooling of power semiconductor devices embedded in a printed circuit board

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Abstract

High-performance cooling of power semiconductor devices embedded in a printed circuit board

The integration of power semiconductor devices within a printed circuit board (PCB) stack is a promising solution to reduce circuit parasitics, simplifying device packaging, and lowering costs. However, the continuous reduction in the chip size of the semiconductors, combined with the low thermal conductivity of the dielectric layers of PCBs, present more thermal challenges, and require more efficient thermal management solutions.

The thermal management and cooling solutions must offer low thermal resistance between the chip junction and its environment and be capable of handling a high-power loss density at the chip level without exceeding the upper limit of the chip junction temperature. Most silicon devices are limited to 175°C to account for the temperature limits of packaging materials. The ultimate goal of this thesis is to achieve a power-loss density of 1000 W/cm² without exceeding the junction temperature limit of 175°C. This goal is constrained by other considerations such as low power consumption, compact size and weight, high reliability, low cost, and minimal maintenance. Finally, the cooling solutions studied here must be compatible with PCB manufacturing processes and embedding technology, as we aim to apply them to chips integrated into PCBs.

In this research project, two thermal management solutions are studied. First, a graphite heat spreader with high thermal conductivity (1300 W/(m.K) in-plane, and 15 W/(m.K) cross-plane) is integrated into the PCB stack. Second, a heat extraction solution based on water jet impingement cooling technique is implemented to collect heat at the PCB surface. For the heat spreading solution, the junction-to-ambient and junction-to-case thermal resistances values (R_{thJA} and R_{thJC}, respectively) of the PCB variants with embedded diodes and MOSFET chips, are reduced by up to 38 % in R_{thJA} and 30 % in RthJC. For the heat extraction solution, the presented water jet cooler (JIC) experimentally reduces R_{thJA} by 33% compared to a conventional cold plate. The effective heat transfer coefficient (HTC) of the JIC is calculated through simulations and found to be about 43 kW/(m².K) with a pressure drop of 9.7 kPa. This performance allows achieving a power loss density of 865 W/cm² without exceeding the junction temperature limit of 175°C. Increasing the thermal conductivity of the isolation layer by 10 times will allow to reach 993 W/cm² (very close to the target of 1000 W/cm²).

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Résumé

Refroidissement haut-performance de composants de puissance enfouis dans un circuit imprimé

L'intégration de dispositifs semi-conducteurs de puissance dans un circuit imprimé (PCB) est une solution prometteuse pour réduire les éléments parasites des circuits, simplifier le packaging des dispositifs et réduire les coûts. Cependant, la réduction continue de la taille des puces semi-conductrices, combinée à la faible conductivité thermique des couches diélectriques des PCB nécessitent des solutions de gestion thermique plus efficaces.

Les solutions de gestion thermique et de refroidissement doivent offrir une faible résistance thermique entre la jonction de la puce et son environnement, et être capables de gérer une densité de puissance élevée au niveau de la puce sans dépasser la limite supérieure de la température de jonction de la puce. La plupart des dispositifs en silicium sont limités à 175°C. L'objectif de cette thèse est d'atteindre une densité de puissance de 1000 W/cm² sans dépasser la limite de température de jonction de 175°C. Cet objectif est contraint par d'autres considérations telles que la faible consommation d'énergie, la taille et le poids, la haute fiabilité, le faible coût et un entretien minimal. Enfin, les solutions de refroidissement étudiées ici doivent être compatibles avec les processus de fabrication des PCB et la technologie d'intégration, car nous visons à les appliquer aux puces intégrées dans les PCB.

Dans ce projet de recherche, deux solutions de gestion thermique sont étudiées. Tout d'abord, un dissipateur de chaleur en graphite avec une haute conductivité thermique (1300 W/(m.K) dans le plan, et 15 W/(m.K) hors plan) est intégré dans le PCB. Deuxièmement, une solution d'extraction de chaleur basée sur la technique de refroidissement par jet d'eau impactant est mise en œuvre pour collecter la chaleur à la surface du PCB. Pour la solution de dissipation de chaleur, les valeurs des résistances thermiques jonction-environnement et jonction-boîtier (R_{thJA} et R_{thJC}, respectivement), des variantes de PCB avec des diodes et des puces MOSFET intégrées, sont réduites jusqu'à 38 % pour R_{thJA} et 30 % pour R_{thJC}, d'après les mesures. Pour la solution d'extraction de chaleur, le refroidisseur à jet d'eau (JIC) présenté réduit expérimentalement R_{thJA} de 33 % par rapport à une plaque froide conventionnelle. Le coefficient de transfert de chaleur effectif (HTC) du JIC est calculé par simulations et s'élève à environ 43 kW/(m².K) avec une chute de pression de 9,7 kPa. Cette performance permet d'atteindre une densité de puissance de 865 W/cm² sans dépasser la limite de température de jonction de 175°C. Augmenter la conductivité thermique de la couche isolante par un facteur de 10 permettra d'atteindre 993 W/cm² (très proche de l'objectif de 1000 W/cm²).

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Résumé en français

Chapitre 1 : Introduction et contexte

L'intégration de dispositifs semi-conducteurs de puissance à l'intérieur d'une carte de circuit imprimé (PCB) est une solution prometteuse pour réduire les parasites du circuit, simplifier le packaging des dispositifs et réduire les coûts (Figure 1.4). Cependant, la réduction de la taille des puces permise par les semi-conducteurs à large bande interdite (WBG), associée à la faible conductivité thermique des couches isolantes des PCB, présente certains défis thermiques par rapport à la soudure directe de la puce sur un substrat conducteur épais.

Les solutions de gestion thermique (refroidissement) doivent offrir une faible résistance thermique entre la jonction de la puce et son environnement et être capables de gérer une densité de perte de puissance élevée au niveau de la puce. L'augmentation des pertes de chaleur dans la puce conduit à une augmentation de sa température de jonction (T_j) qui a une limite supérieure au-delà de laquelle il y a un risque de défaillance. La plupart des dispositifs en silicium sont limités à 175°C afin de prendre en compte les limites de température des matériaux de packaging. L'objectif principal de ce travail est d'atteindre une densité de perte de puissance de 1000 W/cm² sans dépasser la limite de la température de jonction de 175°C. Cet objectif est contraint par d'autres considérations telles qu'une faible consommation d'énergie, une taille et un poids compacts, une haute fiabilité, un coût faible et un faible niveau de maintenance. Enfin, les solutions de refroidissement étudiées ici doivent être compatibles avec les processus de fabrication des PCB, car nous voulons les appliquer aux dispositifs intégrés dans les PCB.

Un système de gestion thermique commence par la puce, qui est la source de chaleur et a une surface très petite (quelques mm²). Il maximise la dissipation thermique à travers les couches de PCB. Pour atteindre un transfert de chaleur élevé, des matériaux à haute conductivité thermique doivent être utilisés pour dissiper la chaleur d'une petite source de chaleur vers une surface de refroidissement plus grande. L'augmentation de la surface d'échange thermique facilite l'extraction de la chaleur vers l'environnement par convection. Dans ce projet de recherche, deux solutions de gestion thermique sont étudiées. Tout d'abord, un répartiteur de chaleur est intégré dans le PCB. Ensuite, un échangeur de chaleur liquide est mis en œuvre pour collecter la chaleur à la surface du PCB. Les deux solutions sont conçues pour gérer une densité de perte de puissance de 500 à 1000 W/cm² au niveau de la puce et pour être compatibles avec la technologie d'intégration et le processus de fabrication des PCB.

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Chapitre 2 : bibliographie

Diffusion de la chaleur

Pour faciliter l'extraction de la chaleur, il est nécessaire de la dissiper efficacement vers une grande surface d'échange thermique où elle sera échangée avec le système de refroidissement. L'objectif est d'identifier un répartiteur de chaleur avec une conductivité thermique élevée, un coefficient de dilatation thermique (CTE) approprié, compatible avec le processus d'intégration dans les PCB, de taille compacte et de faible coût.

Le diamant est un excellent répartiteur de chaleur grâce à sa conductivité thermique élevée (2000 W/(m.K)) et son faible CTE qui correspond aux matériaux semi-conducteurs. Cependant, le coût élevé du diamant le rend inadapté aux applications électroniques de puissance destinées aux produits commerciaux. Le graphite possède une conductivité thermique élevée pouvant atteindre 2000 W/(m.K). Cependant, c'est un matériau anisotrope. La conductivité thermique est élevée dans le plan (X-Y) tandis que dans la direction Z, elle est faible (quelques watts/(m.K)). Le même comportement anisotrope se retrouve avec les valeurs de CTE.

De nombreuses études ont envisagé l'intégration de couches de graphite pour améliorer la dissipation thermique et l'uniformité de la température, tandis que d'autres ont travaillé sur l'empilement des couches de graphite de manière à ce que la conductivité thermique élevée soit dans la direction Z, où la chaleur est transférée vers le côté refroidissant du substrat. L'empilement de couches de graphite de cette manière nécessiterait de fabriquer l'empilement et de l'encapsuler dans un processus distinct, puis d'intégrer l'empilement comme une couche lors du processus de laminage des PCB. De plus, une telle disposition offre une conductivité thermique médiocre dans l'une des directions horizontales, ce qui limite la capacité et l'uniformité de la dissipation thermique.

La chambre à vapeur fonctionne comme un répartiteur de chaleur utilisant un fluide de travail sous forme gazeuse et liquide, ce qui est une technique de refroidissement intéressante. Des mises en œuvre ont été proposées en utilisant une technologie semblable aux PCB (TGP). Cependant, les limitations du flux de chaleur appliqué (pour éviter l’assèchement) et le mode de conduction imposent des contraintes à l'utilisation des chambres à vapeur. De plus, la structure de la mèche est un élément critique qui affecte la résistance thermique ainsi que la résistance à l'écoulement, ce qui nécessite plus de recherches. Les répartiteurs de chaleur à chambre à vapeur ne sont pas étudiés dans ce travail de thèse.

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Plus de recherches sont nécessaires pour tirer parti de la conductivité thermique horizontale élevée du graphite afin de dissiper la chaleur tout en réduisant sa résistance thermique dans la direction verticale. De plus, l'intégration de couches de graphite semble être compatible avec le processus de fabrication des PCB, car le graphite est disponible sous forme de feuilles. Par conséquent, le graphite est choisi pour la dissipation thermique et son intégration dans un PCB sera étudiée plus en détail.

Extraction de chaleur

Après avoir dissipé la chaleur, l'objectif est d'extraire autant de chaleur que possible de la grande surface avec la plus petite différence de température possible par rapport à l'environnement (température ambiante). La chaleur est transférée par convection via un fluide de refroidissement pour être évacuée vers l'environnement. Pour améliorer l'extraction de la chaleur, la surface de refroidissement doit être plus grande afin d'échanger plus de chaleur avec le flux de fluide de refroidissement. De plus, nous pouvons augmenter le coefficient de transfert de chaleur en choisissant un fluide de refroidissement avec une capacité thermique élevée, en augmentant la vitesse du flux de refroidissement, et en considérant le refroidissement biphasé pour profiter du transfert de chaleur latent. En outre, en se rapprochant de la source de chaleur (refroidissement direct ou refroidissement près de la jonction), la différence de température entre la jonction et l'entrée du refroidisseur ou l'environnement sera plus élevée, permettant une extraction de chaleur plus importante.

Cependant, augmenter la capacité d'extraction de chaleur d'un système de refroidissement peut nécessiter une consommation d'énergie et des coûts supplémentaires. L'augmentation de la surface d'échange thermique entraîne une augmentation de la taille et du poids, ce qui peut être un facteur limitant pour certaines applications. Augmenter les coefficients de transfert de chaleur en augmentant la vitesse et le débit du fluide de refroidissement nécessitera des pompes plus grandes et des coûts supplémentaires. Choisir un fluide de refroidissement avec une haute capacité de transfert de chaleur peut améliorer la performance thermique globale, mais il peut être dynamiquement visqueux, ce qui entraîne une plus grande perte de pression. Considérer le refroidissement biphasé peut augmenter les taux de retrait de flux de chaleur mais ajoutera à la complexité du système de refroidissement.

De nombreuses études ont été examinées pour identifier une solution de refroidissement efficace compatible avec la technologie d'intégration des PCB. Les techniques de refroidissement par air naturel et forcé sont des méthodes conventionnelles pour le

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refroidissement des électroniques de puissance, mais leur capacité de transfert de chaleur est faible, ce qui les rend inadaptées aux applications à haute densité de perte de puissance. Les techniques de refroidissement liquide et biphasé ont montré des taux de transfert de chaleur plus élevés. À partir de la Figure 2.44, Les techniques de microcanaux, jet impactant et de refroidissement par pulvérisation peuvent atteindre une résistance thermique correspondant à une densité de perte de puissance de 1000 W/cm² pour une puce de 3,3×3,3 mm² à une température de jonction limite de 175°C. Cependant, les études sur les techniques de refroidissement par microcanaux et par jet impactant montrent une résistance thermique moindres avec des performances hydrauliques comparables. Les études sur les jets impactant montrent cependant des valeurs de puissance de pompage plus élevées que celles de la technique de refroidissement par microcanaux.

En conclusion, l'impact par jet de liquide combiné à une augmentation efficace de la surface d'échange thermique, telle que les ailettes, est choisi pour augmenter l'extraction de chaleur, car il fournit une température de surface plus uniforme comparé à la technique des microcanaux.

Chapitre 3: Méthodes et outils

Ce chapitre décrit la physique des mécanismes de transfert de chaleur et leurs équations caractéristiques. De plus, les modèles analytiques utilisés dans cette thèse et les méthodes numériques sont brièvement expliqués. Les outils de simulation numérique et leurs paramètres de configuration sont détaillés ainsi que les configurations des tests expérimentaux pour la validation expérimentale.

Dans ce travail de thèse, ANSYS Workbench est utilisé pour la modélisation et les simulations. Le module ANSYS Mechanical est utilisé pour effectuer des simulations thermiques sur des modèles uniquement solides, tandis qu'ANSYS CFX est utilisé pour effectuer des simulations CHT où les domaines solides et fluides sont impliqués. Lors de la modélisation CAO, les symétries géométriques sont prises en compte chaque fois que possible afin de réduire la puissance de calcul nécessaire pour les simulations numériques. De plus, certaines simplifications sont faites pour la même raison sans affecter la configuration physique. Plus de détails sur la modélisation peuvent être trouvés dans les chapitres 4 et 6. Les propriétés des matériaux utilisés pour les simulations sont spécifiées dans Table 3.2 ([122], [123], [114]). Étant donné que la valeur de la conductivité thermique du SiC change considérablement avec la température [114] comme montré dans la Figure 3.4, la valeur est prise à 70°C, température à laquelle les tests sont effectués.

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L'objectif de ces mesures est de quantifier la résistance thermique du boîtier PCB depuis la température de jonction de la puce jusqu'à la température de référence (température ambiante, température d'entrée du liquide de refroidissement, etc.). L'impédance thermique (Z_{th}) est la différence entre la température de jonction de la puce (T_j) à un certain moment pendant le chauffage et une température de référence (T_r) divisée par la puissance d'entrée Q selon l'équation (3.47). Lorsque l'impédance thermique atteint un état stable, sa valeur devient égale à la résistance thermique.

La mesure de l'impédance thermique est effectuée à l'aide d'un analyseur thermique (AnalysisTech Phase 12 [110]). Ce système injecte automatiquement un niveau de puissance donné dans l'échantillon testé pour le chauffer, puis surveille un Paramètre Électrique Sensible à la Température (TSEP) de l'échantillon pendant la phase de refroidissement. Le système est composé de l'analyseur thermique Phase 12, d'un dispositif de test refroidi par liquide et d'un refroidisseur à recirculation (National Lab GUPCPR020.03-NED [111]). De plus, un four est utilisé pour la calibration des dispositifs à semi-conducteurs à tester avec l'analyseur thermique. La Figure 3.7 montre un schéma de l'installation expérimentale thermique.

La résistance thermique jonction-boîtier (R_{thJC}) peut être calculée en utilisant une mesure locale de la température du boîtier (à un endroit donné sur la surface inférieure de l'échantillon de PCB) comme température de référence Tr. Cependant, le boîtier n'est pas isotherme, surtout compte tenu des facteurs de forme plats d'un PCB (très fin et large, entraînant de grandes différences de température sur la surface). Dans cette thèse, nous utilisons le TDIM pour estimer le R_{thJC} des échantillons de PCB, car il ne repose pas sur une mesure de la température du boîtier. Le TDIM est décrit dans la norme JEDEC51-14 [115]. Le TDIM est une technique différentielle basée sur la mesure de l'impédance thermique Z_{th} d'un échantillon à deux reprises, avec deux TIMs différents ayant des résistances thermiques significativement différentes. La différence entre les TIMs crée un changement dans la résistance du chemin de propagation de la chaleur, ce qui entraîne une séparation entre les deux courbes d'impédance thermique. Selon la norme JEDEC51-14, le point de séparation est supposé se produire à l'interface entre le boîtier du PCB et le TIM. Par conséquent, la valeur d'impédance thermique à laquelle la séparation se produit correspond à R_{thJC}.

Concernant les mesures thermo-hydrauliques, l'objectif est de quantifier les performances thermiques du refroidisseur à jet d'eau (JIC) en termes de R_{thJA} atteint et de caractéristiques de chute de pression/débit volumétrique. Le JIC est abordé dans le chapitre 6 et remplace la plaque

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froide décrite ci-dessus dans le système complet de gestion thermique (qui inclut le répartiteur de chaleur et le JIC). Dans cette configuration, la mesure de l'impédance thermique est effectuée à l'aide du même analyseur thermique (AnalysisTech Phase 12 [110]) comme expliqué précédemment. L'eau de refroidissement circule comme illustré dans Figure 3.21 et Figure 3.22.

Chapitre 4: Diffusion de la chaleur – conception et simulations

Dans ce chapitre, une étude paramétrique basée sur un modèle analytique de transfert de chaleur est réalisée pour déterminer les caractéristiques d'une structure pouvant dissiper une densité de perte de puissance de 500 W/cm². En conséquence, une solution de dissipation thermique compatible avec les processus de fabrication des PCB est présentée. Elle repose sur une structure sandwich d'adhésif et de graphite intégrée dans un boîtier PCB.

Des boîtiers de diodes et de MOSFET avec du graphite intégré sont conçus et modélisés. Plusieurs variantes de PCB avec du graphite intégré sont comparées à des échantillons de référence sans graphite. La Figure 4.9 montre un concept de configuration de PCB permettant d'intégrer du graphite tout en assurant la compatibilité avec le processus de fabrication des PCB. Les couches de graphite sont empilées avec des couches d'adhésif pendant le processus de stratification. Des micro-vias sont percés au laser à travers l'empilement graphite/adhésif et remplis de cuivre pour fournir des connexions électriques à la puce ainsi qu'un chemin vertical à faible résistance thermique pour la chaleur dissipée. Dans cette configuration, les micro-vias remplacent les piliers en cuivre, donc la densité des micro-vias doit être suffisante pour transférer la chaleur dissipée de la puce vers le graphite avec une faible résistance thermique. La Figure 4.10 montre les étapes de fabrication d'un tel PCB avec une puce et des couches de graphite intégrées.

Les simulations numériques thermiques sont effectuées en utilisant la méthode des éléments finis (FEM) sur ANSYS Mechanical. En tirant parti de la symétrie, seul un quart de la partie active (la zone de 10×10 mm² ou 20×20 mm² contenant du graphite) des échantillons de PCB à diode unique est considéré pour limiter les calculs et le temps (Figure 4.21) sans affecter les résultats de la simulation. Pour la partie à double diode, la moitié de la structure est considérée au lieu d'un quart (Figure 4.22). Les conditions aux limites sont définies selon les mesures expérimentales. Un coefficient de transfert de chaleur (h) est utilisé au dos du PCB pour représenter le comportement du TIM et de la plaque froide.

Deux paramètres sont comparés ici : la résistance thermique jonction-ambiant (R_{thJA}, la valeur à l'état stable de Z_{th}) et la résistance thermique jonction-boîtier (R_{thJC}). R_{thJC} est calculé

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d'une manière qui imite la méthode TDIM : deux simulations thermiques transitoires sont effectuées pour chaque échantillon, avec deux valeurs différentes de *h* : 6000 W/(m².K) et 36000 W/(m².K), représentant respectivement les TIMs utilisés dans les mesures (pad thermique et eau déionisée). Pour les échantillons de PCB de 10×10 mm², les valeurs de h sont : 9000 W/(m².K) et 40000 W/(m².K). Ces valeurs de *h* sont obtenues pour que les simulations des échantillons de référence correspondent aux valeurs mesurées expérimentalement. La méthode de traitement décrite dans la norme JEDEC51-14 est ensuite appliquée. Cela nous permet de ne faire aucune hypothèse sur la distribution de la température au dos des échantillons, et fournit une valeur de RthJC qui est entièrement cohérente avec la méthode de mesure. Le Table 4.4 montre les conditions aux limites appliquées dans les simulations pour obtenir R_{thJA} et R_{thJC}.

Figure 4.25 montre les courbes d'impédance thermique et les valeurs de R_{thJA} pour toutes les variantes de PCB à diode unique obtenues par des simulations thermiques transitoires FEM. L'influence de l'intégration du graphite est évidente. Jusqu'à 51 % de réduction de R_{thJA} est atteinte dans les variantes de PCB de 20×20 mm² (de 4.27 K/W dans D22R à 2.1 K/W dans D22Ga ou D22Gb). De plus, l'augmentation de la densité des micro-vias (layout Ga ou Gb) réduit R_{thJA} d'environ 2.5 % par rapport au layout Gc sans micro-vias distribués (2.1 K/W contre 2.2 K/W). En ce qui concerne les variantes de PCB de 10×10 mm² (D11R et D11Ga), le R_{thJA} est réduit de 42.1 % (de 4.28 K/W dans D11R à 2.48 K/W dans D11Ga).

L'effet de la dissipation thermique due au graphite peut être observé en comparant D22Ga avec D11Ga (tailles de feuille de graphite de 20×20 mm² et 10×10 mm², respectivement) avec une augmentation de R_{thJA} d'environ 18.7 % dans les simulations (2.09 K/W, 2.48 K/W, respectivement). Cependant, même la surface relativement modeste offerte par la variante de 10×10 mm² (un quart de la surface des échantillons de 20×20 mm²) a déjà un effet de dissipation significatif par rapport à la variante de PCB de référence (réduction de 42.1 % de R_{thJA}). Cela signifie qu'un dissipateur thermique en graphite de 10×10 mm² peut être suffisant pour certaines applications, et que l'augmentation de la surface de graphite peut n'apporter que des gains modérés.

En ce qui concerne R_{thJC}, les valeurs sont calculées en utilisant la procédure de calcul TDIM décrite dans la norme JEDEC51-14 pour les différentes variantes de PCB, comme illustré en 3.4.2.2. Pour chaque échantillon, deux courbes d'impédance thermique sont obtenues en appliquant deux valeurs de coefficient de transfert de chaleur au bas du PCB (comme illustré en 4.2.6). Selon les simulations, les variantes de PCB avec graphite atteignent environ 25 % de

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réduction de R_{thJC} par rapport à l'échantillon de référence (Figure 4.26). Pour les échantillons de 10×10 mm², la réduction est plus modeste, 11 % pour D11Ga par rapport à l'échantillon de référence D11R (Figure 4.27). Table 4.5 montre une comparaison entre toutes les variantes de PCB en termes de valeurs R_{thJA} et R_{thJC} et la réduction obtenue par rapport aux variantes de PCB de référence.

Des variantes supplémentaires de PCB avec diodes doubles sont conçues et simulées, et le comportement de couplage thermique a été comparé. Le couplage thermique est augmenté (de 1.85 % à 11.85 %) grâce aux couches de graphite. Cela peut aider à équilibrer la température des puces, par exemple en cas de connexion en parallèle.

Chapitre 5: Diffusion de la chaleur – test et validation

Ce chapitre présente la validation expérimentale de notre dissipateur thermique en graphite intégré. Des boîtiers PCB pour diodes et MOSFET avec du graphite intégré sont fabriqués avec succès et comparés à des échantillons de référence sans graphite.

Des tests de caractérisation électrique sur 55 échantillons de diodes et 42 échantillons de MOSFET sont réalisés à l'aide d'un traceur de courbes (Keysight B1505A) et d'une station sous pointes, comme présenté dans la Figure 5.6. Une comparaison est effectuée avec les spécifications des dispositifs pour détecter tout écart pouvant avoir été causé par le processus d'intégration. Plusieurs paramètres sont testés (tels que : les courants de fuite IGS & IDS, la résistance drain-source en conduction R_{DSon}, la tension de seuil gate-source V_{GSTH}, la tension de claquage drain-source V_{BV}, etc.). En ce qui concerne les MOSFETs, les valeurs de la tension de seuil gate-source (V_{GSTH}) ainsi que la tension de claquage drain-source (V_{BV}) sont montrées dans la Figure 5.7. Pour les diodes, les valeurs de la tension de claquage (V_{BV}) à haute tension sont présentées dans la Figure 5.7. Un rendement de fabrication de 86 % pour les dispositifs semiconducteurs intégrés a été mesuré, ce qui est une valeur raisonnable pour un lot de prototypes.

Un test de convection thermique par refusion est réalisé sur certains des échantillons de PCB selon la norme IPC-TM-650. Ce test simule les cycles thermiques subis par un PCB dans des fours de brasure lors du soudage des composants électriques et des connexions, et est utilisé ici comme première évaluation du comportement thermo-mécanique du dissipateur thermique en graphite. Des mesures de profilométrie sont effectuées à l'aide d'un Nano-Point-Scanner (NPS-NP3) sur différentes variantes de PCB avant et après le test de refusion pour capturer les déformations qui pourraient avoir été causées par les cycles de stress thermique. Les Figures:

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Figure 5.11, Figure 5.12, Figure 5.13, et Figure 5.14 montrent les déformations en micromètres observées sur la surface des variantes de PCB. Les tests montrent qu'un réseau de micro-vias doit être distribué sur la surface du dissipateur pour assurer un maintien mécanique des couches de graphite et prévenir leur délaminage. Les micro-vias distribués "clouent" ensemble les couches de l'empilement du PCB, empêchant la défoliation du graphite de se propager. Bien que des tests de fiabilité à long terme soient nécessaires pour garantir qu'un tel empilement est suffisamment fiable, il semble que les vias distribués soient une solution intéressante pour stabiliser la structure du dissipateur en graphite en considérant le stress thermo-mécanique.

Des mesures et des simulations d'impédance thermique sont effectuées pour obtenir les valeurs de R_{thJA} et R_{thJC} des échantillons. Pour R_{thJC}, la méthode TDIM (décrite en 3.4.1) conformément à la norme JEDEC51-14 est implémentée expérimentalement (comme c'est le cas en simulation, voir chapitre 4).

Table 5.1 montre les valeurs expérimentales de R_{thJA} comparées aux valeurs obtenues par simulations FEM, ainsi que la réduction obtenue en R_{thJA} par l'intégration du graphite par rapport aux échantillons de référence. Les valeurs expérimentales sont la moyenne des cinq mesures, et l'erreur correspond à l'écart-type. L'impact de l'intégration du graphite est évident. Une réduction de jusqu'à 38 % de R_{thJA} est obtenue expérimentalement (jusqu'à 51 % prédite par les simulations thermiques FEM). L'intégration de deux feuilles de graphite réduit le R_{thJA} de 34 à 38 % par rapport à l'échantillon de référence D22R (2.54 K/W, 2.63 K/W, 2.72 K/W et 4.11 K/W, respectivement). Le dissipateur thermique plus petit (D11Ga) présente une R_{thJA} significativement plus élevée de 26.2 % par rapport au dissipateur thermique plus grand (D22Ga) (2.63 K/W, 3.32 K/W, respectivement). Cependant, l'échantillon de 10×10 mm² (D11Ga) montre déjà un effet de dissipation thermique important par rapport à un échantillon de référence de même taille (D11R), malgré sa surface relativement modeste. Une réduction de 24.7 % en R_{thJA} est obtenue expérimentalement (42.1 % en simulations). De ce résultat, on peut conclure qu'un dissipateur thermique en graphite de 10×10 mm² peut montrer un effet de dissipation thermique suffisant pour certaines applications.

Table 5.8 compare les valeurs expérimentales et simulées de R_{thJC} pour toutes les variantes de PCB à diode unique. Les expériences montrent une réduction de 10 à 30 % en R_{thJC} pour les variantes de PCB avec graphite par rapport à l'échantillon de référence, tandis que les simulations montrent une réduction de 25 % en R_{thJC} par l'intégration du graphite. En ce qui concerne les échantillons de 10×10 mm², la réduction obtenue en R_{thJC} est de 19 %

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expérimentalement pour D11Ga par rapport à l'échantillon de référence D11R, tandis que les simulations prédisent une réduction de 11.7 % en R_{thJC}. Une différence allant jusqu'à 31 % peut être observée entre les mesures expérimentales et les simulations thermiques FEM, ce qui suggère un écart entre les échantillons de PCB fabriqués et le modèle de simulation.

La R_{thJA} des puces emballées traditionnellement (TO-247-3) reste inférieure à celle des dispositifs PCB avec dissipateur thermique en graphite, indiquant un effet de dissipation plus efficace pour un cadre en cuivre épais que pour des couches de graphite minces. Cependant, le dissipateur thermique en graphite constitue un compromis intéressant, offrant une amélioration claire par rapport aux PCB standard sans augmentation de l'épaisseur de la carte.

De plus, les échantillons de PCB à diodes doubles sont mesurés thermiquement pour obtenir l'effet de couplage thermique du graphite dans le boîtier multi-puces PCB. Le pourcentage de couplage thermique augmente de 2.94 % dans l'échantillon PCB de référence à 8.78 % par l'intégration du graphite dans le PCB.

Chapitre 6: Extraction de chaleur

La solution de refroidissement par extraction de chaleur est composée d'une semelle en cuivre gravée chimiquement, stratifiée à la carte PCB fabriquée, qui comprend des MOSFET intégrés et des diffuseurs thermiques en graphite. La plaque en cuivre est gravée pour créer des ailettes en forme de broches de 0,5 mm de hauteur afin de maximiser la surface d'échange thermique avec l'eau de refroidissement. Cette combinaison PCB/ailettes en cuivre gravées est assemblée avec un collecteur d'eau compact de type JIC (refroidisseur à jet impactant), fabriqué par la technique d’impression 3D SLS.

Former les ailettes en cuivre à l'aide de l'attaque chimique est une solution attrayante, car il s'agit d'un processus déjà utilisé dans la fabrication de PCB. Cependant, il a été constaté que cela limite la hauteur des ailettes, car graver plus de 0,5 mm (profondeur de gravure) peut entraîner une inhomogénéité par rapport à la forme des ailettes et à la profondeur globale de gravure, car le film photosensible utilisé pour former les motifs peut se détacher des surfaces des ailettes. Former des structures plus hautes nécessiterait un contrôle minutieux du processus de gravure, car les résultats dépendent de la concentration et de la fraîcheur de l’angent gravure (ainsi que de la robustesse de la couche photosensible). Selon les simulations CHT, ces courtes ailettes n'offrent qu'une amélioration modeste des performances thermiques (réduction de 3,2 % de R_{thJA}). Le dissipateur thermique en cuivre peut être fixé (avant ou après gravure des

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ailettes) en le laminant à l'empilement PCB pendant le processus de fabrication, comme toute autre couche de cuivre.

Pour la simulation CHT, la variante de PCB utilisée avec le graphite est le M22Gc, qui n'a pas de vias micro-distribués sur la zone de diffusion. La raison de l'utilisation du M22Gc au lieu du M22Ga (avec vias micro-distribués sur la zone de diffusion), utilisé dans l'expérience, est de réduire le temps de calcul, car les deux M22Ga et M22Gc ont montré une différence de seulement 5 % en R_{thJA}, comme présenté précédemment au chapitre 4 section 4.2.7.1. La Figure 6.37a montre le R_{thJA} de la variante de PCB sans graphite (M22R) et de la variante de PCB avec graphite (M22Gc) pour une plage de débit volumétrique d'eau variant de 0,5 L/min à 2,5 L/min (2,5 L/min étant la limite supérieure pour la pompe utilisée dans notre expérience). La réduction de R_{thJA} obtenue en intégrant du graphite est d'environ 40 % à 2,5 L/min (de 2,83 K/W à 1,7 K/W). Avec un R_{thJA} de 1,7 K/W, le packaging PCB avec graphite peut atteindre une densité de perte de puissance de 864 W/cm² (90 W) sans dépasser la limite de température de jonction de 175°C. Augmenter le débit de 0,5 L/min à 2,5 L/min réduit le R_{thJA} de seulement 4,7 % pour la variante de PCB M22R sans graphite. Pour la variante de PCB M22Gc avec graphite, l'effet de l'augmentation du débit d'eau est légèrement plus important (la réduction est de 6,2 %). Cela malgré la plage de la coefficient de transfert de chaleur (HTC) correspondante d'environ ~16000–43000 W/(m².K), calculée à l'interface du dissipateur thermique, pour la plage de débit d'eau (0,5 – 2,5 L/min). En se référant également à la Figure 6.1, cela suggère que le transfert de chaleur par convection n'est pas la principale contribution au R_{thJA}. La Figure 6.37b montre l'augmentation de la chute de pression lorsque le débit d'eau passe de 0,5 L/min à 2,5 L/min. La chute de pression maximale estimée par simulation est de 9,87 kPa à 2,5 L/min.

Les mesures thermo-hydrauliques sont effectuées en utilisant la méthodologie et le montage expérimental expliqués au chapitre 3 section 3.4.3 afin de mesurer le R_{thJA} total et la chute de pression de l'eau JIC. La Figure 6.45 montre l'assemblage de la PCB/ailettes en cuivre/manifold JIC monté et connecté au montage expérimental thermo-hydraulique. La Figure 6.46a montre les valeurs de R_{thJA} pour une plage de débits volumétriques d'eau du JIC variant de 0,5 L/min à 2,5 L/min. Ces valeurs mesurées sont comparées aux résultats de simulation ainsi qu'à la chute de pression mesurée de l'eau JIC (Figure 6.46b). Comme le montre la Figure 6.46a, le R_{thJA} diminue avec l'augmentation du débit d'eau. Cette réduction est seulement de 5 % pour la variante de PCB M22R sans graphite (de 2,823 K/W à 2,684 K/W) et d'environ 6 % pour la variante de PCB M22Ga avec graphite (de 1,789 K/W à 1,685 K/W). Les valeurs de R_{thJA}

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prédites par les simulations CHT sont dans la marge d'erreur des expériences, à +5 % (comparé aux mesures) pour M22R et +1 % pour M22Ga.

Les mesures thermo-hydrauliques montrent que le R_{thJA} du M22Ga est inférieur de 37 % par rapport au M22R (de 2,684 K/W à 1,685 K/W à 2,5 L/min). Cela correspond étroitement aux 35,5 % mesurés au Chapitre 5 (section 5.4.3) lors du montage de la PCB sur la plaque froide d'eau présentée au Chapitre 3 section 3.4.1.3. Cela indique que le diffuseur thermique en graphite seul est responsable d'une réduction de 35-37 % de R_{thJA}. De plus, le JIC stratifié est responsable d'une réduction de 31-33 % de R_{thJA} par rapport à la plaque froide d'eau conventionnelle utilisée auparavant (de 3,88 K/W à 2,684 K/W pour le PCB M22R sans graphite, et de 2,5 K/W à 1,685 K/W pour le PCB M22Ga avec graphite intégré).

Le HTC du JIC est d'environ 43 kW/(m².K) à une chute de pression de 9,7 kPa. Cette performance permet d'atteindre une densité de perte de puissance de 865 W/cm² sans dépasser la limite de température de jonction de 175°C. Cependant, il est observé que la performance du diffuseur thermique en graphite se dégrade avec l'augmentation de T_j causée par l'augmentation de la puissance injectée, ce qui conduit à atteindre la limite de 175°C à seulement 787 W/cm² de densité de perte de puissance. De plus, augmenter la conductivité thermique de la couche d'isolation de 10 fois (de 2,5 W/(m.K) à 25 W/(m.K)) ne se traduite que par une réduction de 13 % du R_{thJA}. Par conséquent, la densité de perte de puissance peut théoriquement être augmentée à 993 W/cm² (très proche de l'objectif de 1000 W/cm²) sans dépasser la température de jonction de 175°C.

Chapitre 7: Conclusion générale

Dans cette thèse, des solutions de gestion thermique compatibles avec la technologie d'intégration de composants dans le PCB ont été étudiées. Des solutions de gestion thermique (diffusion et extraction de chaleur) ont été examinées afin de trouver la technique la plus adaptée pour le conditionnement et l'insertion de PCB. Deux solutions de gestion thermique ont été étudiées dans ce travail. La première consiste à insérer des dissipateurs thermiques en graphite pyrolytique (1300 W/(m.K) dans le plan X-Y et 15 W/(m.K) dans la direction Z) dans le boîtier du PCB. La seconde utilise un échangeur de chaleur à jet d'eau pour collecter la chaleur de la surface du PCB. Les deux solutions ont été conçues pour gérer une densité de dissipation de puissance de 500 à 1000 W/cm² au niveau de la puce et sont compatibles avec la technologie et les processus de fabrication des PCB.

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Pour la diffusion de chaleur, des simulations et des mesures d'impédance thermique ont été réalisées pour obtenir les valeurs de R_{thJA} et R_{thJC} des variantes de PCB. Une réduction allant jusqu'à 51 % de R_{thJA} et 25 % de R_{thJC} a été observée par des simulations thermiques par la méthode des éléments finis (FEM), comparée à une réduction de 38 % de R_{thJA} et 30 % de R_{thJC} par des mesures. Le pourcentage de couplage thermique a été augmenté (de 1,85 % à 11,85 %) grâce aux couches de graphite selon les simulations, tandis que les mesures ont montré une augmentation de 2,94 % dans l'échantillon de référence de PCB à 8,78 % en insérant du graphite dans le PCB. Cela peut aider à équilibrer la température des puces, par exemple dans le cas d'une connexion parallèle.

Pour l'extraction de chaleur, un jet de liquide combiné avec des ailettes a été choisi comme solution de gestion thermique. Il est composé d'une semelle en cuivre gravée chimiquement, laminée au PCB fabriqué, qui comprend des MOSFET intégrés et des dissipateurs thermiques en graphite. La plaque de cuivre a été gravée pour créer des ailettes de 0,5 mm de hauteur afin de maximiser la surface d'échange thermique avec l'eau de refroidissement. Cette combinaison du PCB et des ailettes en cuivre gravé a été assemblée avec un collecteur d'eau compact du JIC, fabriqué par technique SLS (fabrication additive). Le refroidisseur à jet d'eau présenté réduit expérimentalement le R_{thJA} de 33 % (atteignant 1,685 K/W à 2,5 L/min, ou 17,6 K.mm²/W) par rapport à une plaque froide conventionnelle. Le HTC effectif du JIC est calculé par simulations (environ 43 kW/(m².K)) avec une chute de pression de 9,7 kPa. Cette performance permet d'atteindre une densité de dissipation de puissance de 865 W/cm² sans dépasser la limite de température de jonction de 175°C. Augmenter la conductivité thermique de la couche d'isolation de 10 fois (de 2,5 W/(m.K) à 25 W/(m.K)) entraîne seulement une réduction de 13 % de R_{thJA}, ce qui permet théoriquement d'atteindre 993 W/cm² (très proche de l'objectif de 1000 W/cm²) sans dépasser la température de jonction de 175°C.

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1 Introduction and Context

In this chapter, an introduction to Printed circuit board (PCB) technology and its manufacturing process are presented, as well as the PCB embedding technology and the corresponding thermal challenges. Thermal management approach is demonstrated in order to improve the thermal performance of PCB-based power electronics with high power loss density.

1.1 Printed circuit board (PCB)

PCBs are used to provide electrical connections and mechanical support electrical components (both active - such as transistors - and passive - such as resistors) of an electrical circuit to achieve certain functions [1] (Figure 1.1). They consist of alternating layers of copper tracks and electrically insulating substrate material such as epoxy FR4. In addition, copper inter-layer connections (vias) provide electrical connections between different layers.

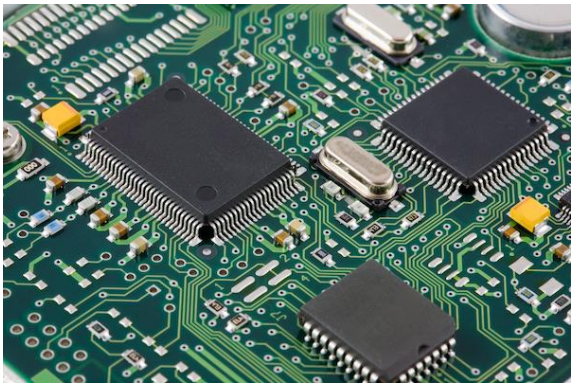

Figure 1.1 : PCB of an electronic circuit [2].

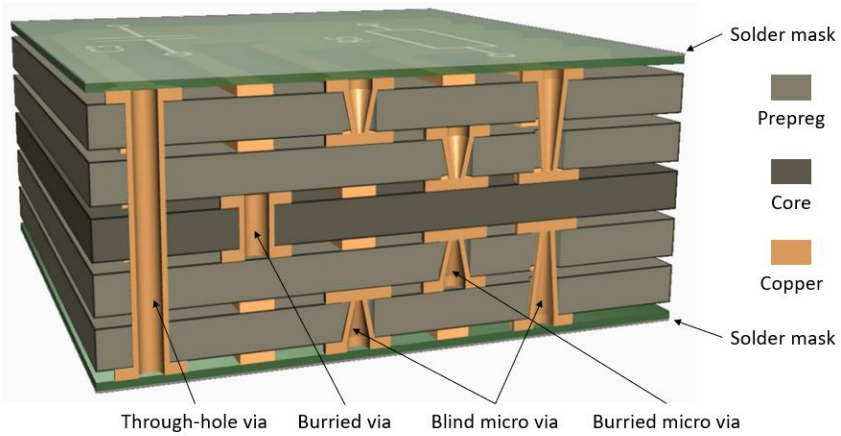

Figure 1.2 : Multi-layer PCB layers and types of vias [3].

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As shown in Figure 1.2, layers of copper and prepreg (pre-impregnated resin) are laminated together. The lamination process takes place at high temperature (190°C to 200°C) and pressure (19 bar to 27 bar), curing the prepreg layers and forming so-called laminates together with the copper. A "core" is effectively one or more prepreg laminates that laminated with copper on one or two sides to form a rigid base material. A core is used for manufacturing single sided and double-sided boards but is also used as a starting point in the production of multi- layer PCBs.

To manufacture PCBs, cores are cut, drilled, and plated to form vias (Figure 1.3). The copper layers are chemically etched to form copper tracks. Then the core is stacked with layers of prepreg and copper to form a multi-layer PCB. After that, the stack-up is laminated under high temperature and pressure as mentioned earlier. Then vias are drilled mechanically or by laser (micro vias) to create vertical electrical interconnections between copper layers, or to create a thermal path for the heat (thermal vias). In multilayer PCBs, vias can connect different layers, depending on where they are. Through-hole vias (going all the way through the board, hence connecting all layers), blind vias (drilled from one side only), and buried vias (connecting only internal layers). In all cases, vias holes are plated with copper using electroplating deposition. Once all layers have been forms, a solder mask is applied on the outer surfaces of the board. This mask is a thin layer of polymer (often green) that protects copper from oxidation and prevents solder bridges to form between solder pads that are close to each other. Finally, symbols and references are stencil-printed ("silkscreen" layer) on the solder mask to label components and to provide other information about the PCB.

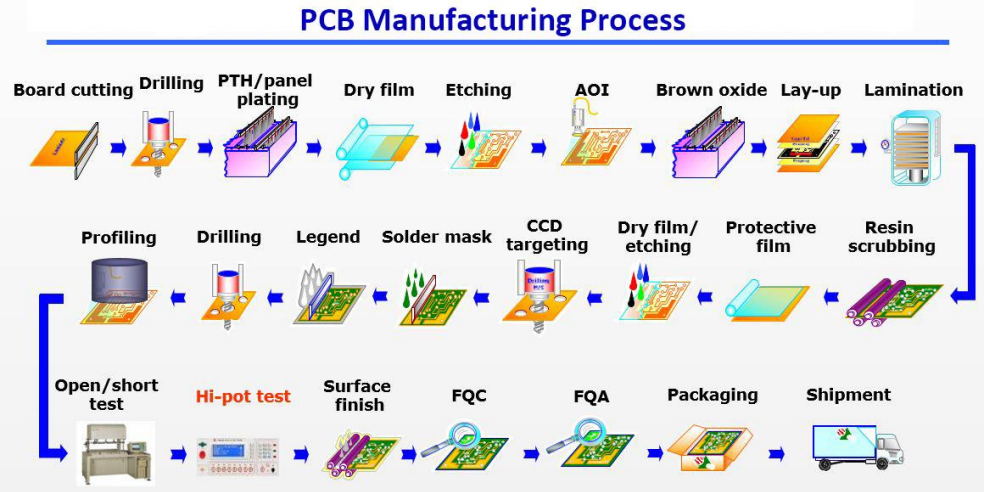

Figure 1.3 : PCB manufacturing process [4].

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1.2 PCB embedding technology

Usually, components are soldered on the external surfaces of the PCBs (“surface-mount technology”). Recently, a new approach has been emerged, especially for active power components: embedding dies within the PCB itself (Figure 1.4 and Figure 1.5). In many aspects, this is a promising technology to replace the standard power module technology with DBC (Direct Bonded Copper) substrates and wire bonding [1].

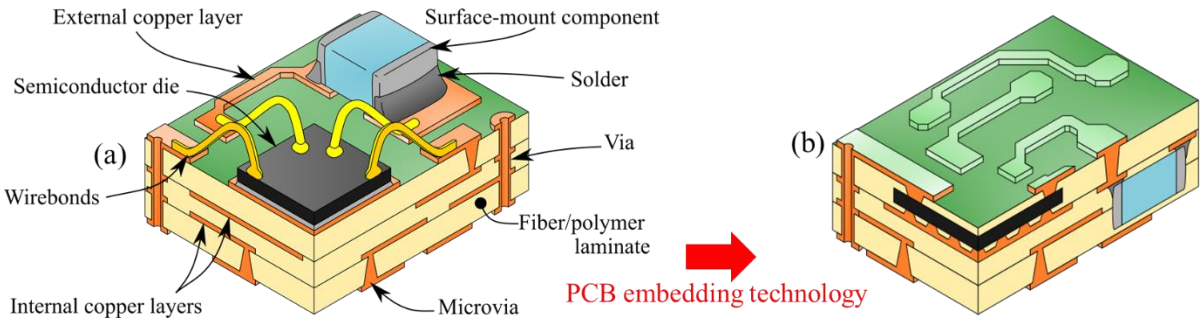

Figure 1.4: Embedding components in PCB.

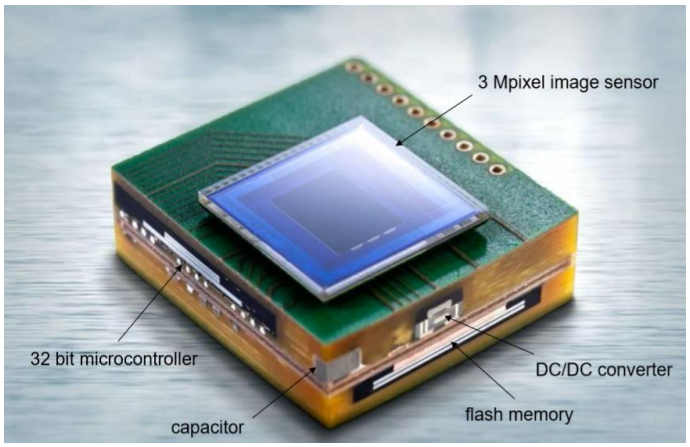

Figure 1.5 : Modular camera with integrated 32-bit image processor and memory [5].

The embedded die packaging with its low parasitic interconnection and low cost is perfectly suited for wide band gap devices such as SiC MOSFET [2]. However, performances have to come along with high reliability and good thermal management to ensure a new technology is competitive against established ones.

Despite the intrinsic low cost of PCB manufacturing, it must also offer good thermal performance so that embedded devices can be utilized to their full potential. SiC devices remains more expensive than their Si counterparts. Indeed, the SiC substrate fabrication is time

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and energy consuming. Trench type SiC MOSFETs offer the advantage of reducing the total die footprint by using a vertical channel in the semiconductor compared to the more classical planar structure, resulting in smaller dies at each new device generation. However, this footprint reduction comes with higher power loss density and a smaller area for heat extraction. Qian et al. [8] concluded in their review on IGBT power modules, that the continuous miniaturization, high voltage, high current, and increasing power ratings of IGBTs have a significant impact on power loss density and therefore, increasing total heat dissipation. The packaging solutions used for SiC devices must therefore allow to extract more heat density from a smaller area. This is, in a nutshell, the challenge which is addressed in this thesis.

1.3 Thermal challenges

Increasing heat flux leads to an increase in chip junction temperature (T_j) which has an upper limit over which there is a risk of failure. Some silicon devices are limited to 150°C and most to 175°C. Furthermore, it is often considered that component lifetime is shortened by a factor of 2:1 for every 10°C rise in junction temperature [6]. The higher the junction temperature of a semiconductor chip, the less reliable and durable it is [7]. WBG semiconductors such as SiC and GaN can in theory reach higher temperatures but in practice, they are limited to about 175°C due to constraints of available packaging technology (taking into account the considerations of structural components, solder materials, reliability and costs [8]).

Developing thermal management and packaging solutions to reduce junction temperature of electronic components, and therefore reducing their thermal resistance, has become an important issue because of increased power loss density levels with simultaneous miniaturization of the semiconductor chips. While a lot of progress has been achieved in electrical performance, cost and size of the chips, packaging and thermal management technology have not reached the same level of development. This makes it difficult to use the most advanced chip technologies available to their full potential [9].

Choosing the best suitable thermal management and cooling strategy for the PCB of a power module depends on design requirements, application constraints and working environment. For example, in aerospace applications, size and weight of the power module are very important parameters as well as cost which is a common parameter in all commercial applications such as automotive electronics to smart phones.

Therefore, to take advantage of the latest power electronics technology and achieve the highest electrical performance, thermal challenges must be overcome.

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1.4 Thermal management approach

Thermal management (cooling) solutions should provide low thermal resistance between a chip junction and its environment and be able to manage high power loss density at chip level. This main objective is constrained by other considerations such as low power consumption, compact size and weight, high reliability, low cost, low maintenance level. Finally, the cooling solutions investigated here should be compatible with PCB manufacturing processes as we want to apply them to PCB-embedded devices.

A thermal management system starts from the electronic component or chip, which is the heat source and has a very small footprint area (a few mm^2 up to a few hundreds of mm^2). It maximizes heat spreading across the substrate material (PCB layers in our case). In order to achieve high heat transfer, materials with high thermal conductivity should be used to spread the heat from a small heat source to a larger cooling surface area. Increasing the heat exchange surface area facilitates the extraction of the heat towards the environment by the means of convection heat transfer mechanism.

In this research project, two thermal management solutions are investigated. First, a heat spreader is embedded in the PCB stack. Then, a liquid heat-exchanger is implemented to collect heat at the surface of the PCB. Both solutions are designed to manage a power loss density of 500 – 1000 W/cm^2 at chip level as well as to be compatible with PCB embedding technology and manufacturing process.

1.5 Outline of this thesis

The next chapter (chapter 2) provides a state-of-the-art review of thermal management solutions for power electronics, considering both heat spreading and heat extraction solutions. The third chapter presents the analytical, numerical and experimental methods and tools used in this work. The fourth chapter demonstrates the proposed concept heat spreading, including the design of the PCB package and the numerical simulations results. The fifth chapter focuses on the experimental validation of this heat spreader, describing the fabrication of the improved PCB package, the measurement results, and a comparison with the numerical simulations. Finally, chapter 6 demonstrates the heat extraction solution, with its design, simulation, fabrication, and experimental validation. The thermal performance of the two thermal management solutions combined (spreader and cooler) is verified.

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2 State of the art

This chapter constitutes a literature survey of power electronics thermal management techniques. First, heat spreading solutions are reviewed in order to find the most suitable technique for PCB packaging and embedding technology. Secondly, heat extraction solutions are reviewed in order to identify the optimal technique with respect to overall thermal performance. Finally, a conclusion on reviewed thermal management techniques is presented.

2.1 Heat spreading

Copper is the conventional heat spreader used in PCBs. It has a good thermal conductivity of around 400 W/(m.K), but its coefficient of thermal expansion (CTE) does not match that of semiconductor chips (17 ppm/K for copper compared to 4.2 ppm/K for SiC and 5.6 ppm/K for GaN) [10]. Thermal expansion mismatching creates stress between attached layers of different CTE since they do not expand at the same rate as the other layers. CTE-mismatch and low thermal conductivity can cause reliability issues to power electronics devices. Figure 2.1 shows the thermal conductivity and the CTE of various materials.

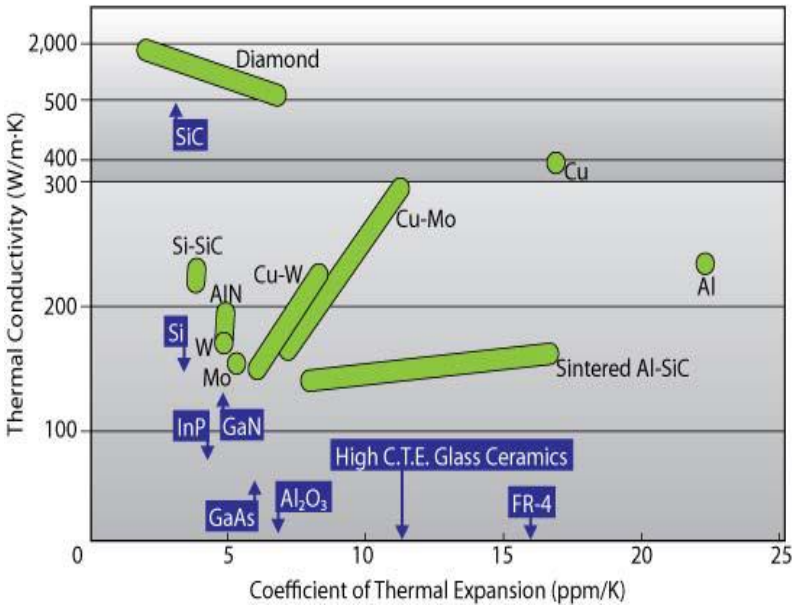

Figure 2.1 : Thermal conductivity and CTE of various materials [11].

In order to go beyond the thermal performance of copper, the only candidates are carbon-based materials, which offer high thermal conductivity. Integrated heat spreaders with thermal conductivity higher than copper and a low CTE (to match that of semiconductors) material are needed. In this section, a review on the heat spreaders is presented. Only solid-state heat

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spreaders are considered in this section, as convection-based heat spreading solutions (such as vapor champers) are considered in the “heat extraction” solutions presented in section 2.2.

2.1.1 Diamond heat spreader

Diamond is an excellent thermally conductive material. It has a high isotropic thermal conductivity which can reach up to 2000 W/(m.K), five times higher than that of copper, and a low CTE of 1 ppm/K [12]. These thermal characteristics make diamond heat spreaders attractive to use in power electronics packages. Figure 2.2 shows a metalized diamond heat spreader.

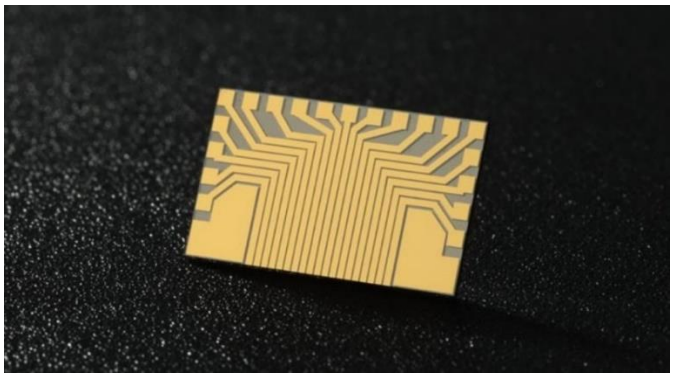

Figure 2.2 : Metalized diamond heat spreader [13].

In [14], the effect of using a diamond heat spreader between a GaN chip with eight hot spot heaters and a copper microchannel heatsink cooled by water is investigated. By applying power up to 50 W, the maximum overall thermal resistance of the whole cooling structure can be reduced by 45.2 % using a diamond heat spreader with a thermal conductivity of 1800 W/(m.K) at room temperature. In another study [15], the same concept is applied together with a hybrid microchannel/jet impingement silicon cooler. A 25 % reduction in hotspot temperature is achieved using diamond heat spreader.

Diamond particles can be used in a composite to enhance its thermal conductivity and adjust its CTE value as well. In [16], it is reported that a composite made of copper and diamond can be used in a direct bonded copper (DBC) substrate as a heat spreader as well as a buffer layer to compensate for CTE mismatch (Figure 2.3). The copper-diamond metal matrix (Cu-C) is manufactured by spark plasma sintering of powdered copper and synthetic industrial diamonds. The Cu-C-matrix is mounted between two thin copper sheets. The thermal expansion coefficient and thermal conductivity can be adjusted by varying the volumetric percentage of diamond in the Cu-C composite. With 60 % volume of synthetic diamond particles, a thermal

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conductivity of 597±50 W/(m.K) (at 20°C) and a CTE of 8.4±0.8 ppm/K (from 20°C to 250°C) can be achieved.

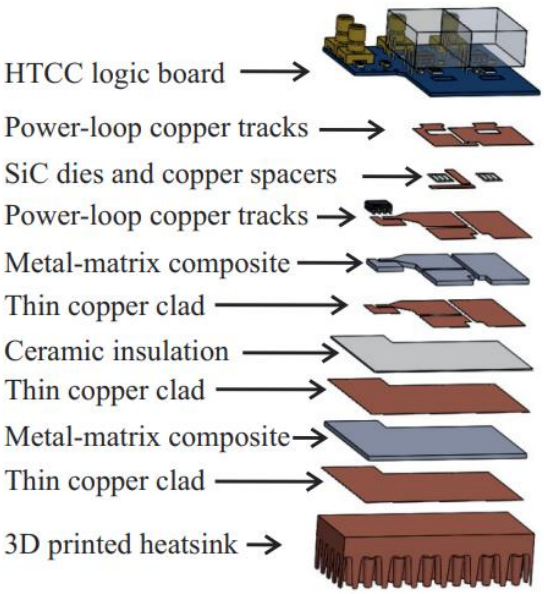

Figure 2.3 : Using copper-diamond composite layer in DBC [16].

Despite the outstanding thermal conductivity and low CTE that make diamond heat spreaders excellent for enhancing thermal performance of power electronics devices, the use of diamond in heat spreaders is limited because of its high cost. Synthetic diamond is an expensive material which can reach 2000 dollars/cm² [17], while chemical vapor deposition (CVD) diamond can reach 490 euros/cm² [12]. However, the cost is expected to be lower in copper-diamond composites.

2.1.2 Graphite heat spreader

Graphite is a crystalline form of carbon that occurs naturally and consists of stacked layers of graphene. Natural graphite is used in pencils, electrodes, and lubricants [18] (Figure 2.4a). Graphene is a single layer of carbon atoms arranged in two-dimensional honeycomb lattice structure (Figure 2.4b). Graphene has high horizontal thermal conductivity that can reach 2000–3000 W/(m.K) [19]. A multi-layer system of almost de-coupled two-dimensional graphene layers forms graphite [20].

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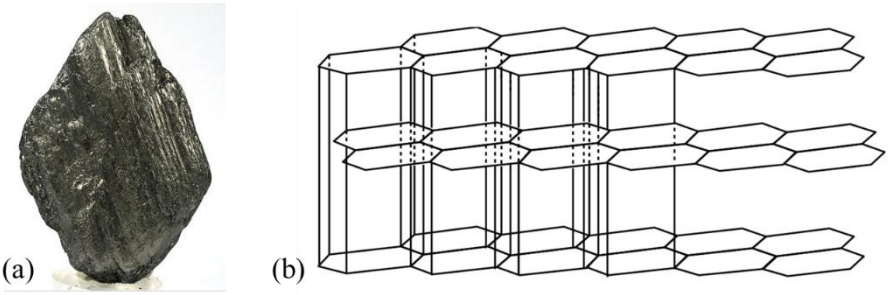

Figure 2.4 : (a) Natural graphite [21]. (b) Graphite composed of multi-layer graphene honeycomb lattice structure [22].

Bonding between graphene layers in graphite is relatively weak and based on van der Waals bonds (a distance-dependent interaction between atoms or molecules, which does not result from chemical electronic bond, and is comparatively weak). The interface between graphene layers are often occupied by gases, making graphene layers separate easily [23]. Natural graphite has many defects in its structure.

Pyrolytic graphite (PG) is a polycrystalline form of graphite that is deposited from the vapor phase by thermal decomposition of a simple hydrocarbon like methane. Pyrolytic graphite is similar to graphite except that it is a man-made material that has some covalent bonds (chemical bond by sharing electron pairs between atoms) between its graphene layers [24].

Highly oriented pyrolytic graphite (HOPG) is a highly ordered form of synthetic graphite. In HOPG, the individual graphite crystallites are well aligned with each other. HOPG is produced based on the process used to make PG, but with additional tensile stress in the basal-plane direction (basal plane is plane parallel to the lateral or horizontal axis) to improve the alignment of graphite crystallites [25]. HOPG is produced by stress annealing at about 3300 K [26].

Annealed Pyrolytic Graphite (APG), also known as Thermally Annealed Pyrolytic Graphite (TPG) is a form of synthetic graphite that has excellent in-plane thermal conductivity (can reach 1700 W/(m.K)). APG is produced in a process like HOPG process, where a hydrocarbon gas is heated until it breaks down into carbon. PG is then grown on plates using a chemical vapor deposition (CVD) process. The PG is then annealed at high temperature to form the more planar and more uniform carbon structure of APG. The primary difference between the HOPG and APG production methods is that the APG annealing process does not require the use of induced stresses, resulting in a more affordable and practical bulk material for production use [27].

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Figure 2.5: Pyrolytic graphite sheet (PGS) [22].

Graphite sheets are used to reduce hot spots and to achieve more uniform chip temperature. Pyrolytic graphite sheets (PGS), produced by Panasonic industries (Figure 2.5), are available in thicknesses ranging from 17 µm to 100 µm with very high in-plane thermal conductivity that can reach five times that of copper (Figure 2.6). However, they have a low cross-plane thermal conductivity (15 W/(m.K)) [22].

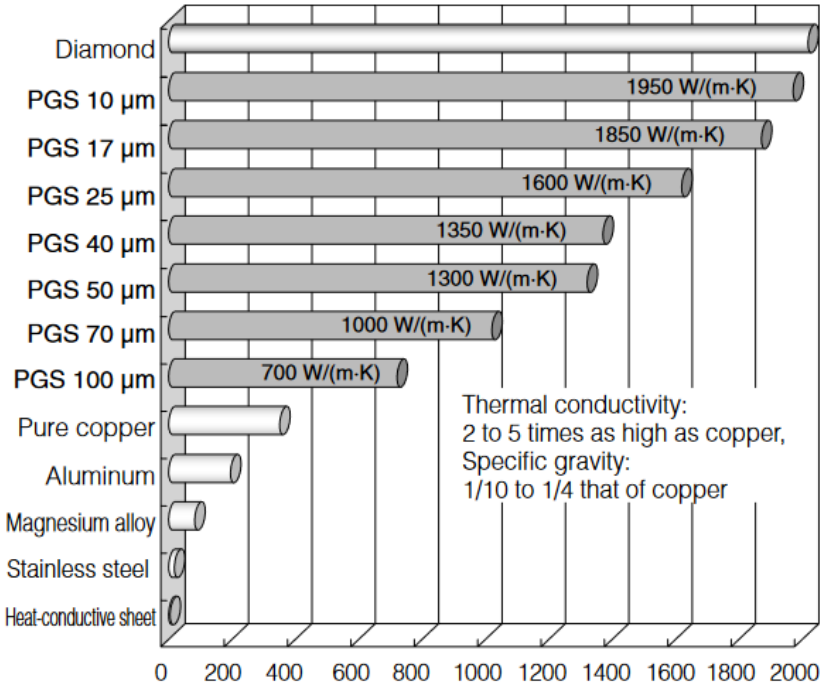

Figure 2.6: Pyrolytic graphite sheet (PGS) thermal conductivities compared to other materials [22].

In [28], the thermal performance of a Graphene-based films (GBF) heat spreader applied in a 3D through-silicon-via (TSV) packaging environment is numerically investigated (Figure 2.7). GBF were fabricated using a chemical conversion process and film formation by vacuum filtration. The thermal conductivity of such films can reach 1430 W/(m.K). It is found that by using GBF of 20 µm thickness, the temperature of on-chip hotspots can be decreased by about

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5°C at a heat flux density of 416 W/cm² compared with chips without any GBF heat spreader. Also, the temperature distribution of chip surface with a GBF heat spreader is more uniform.

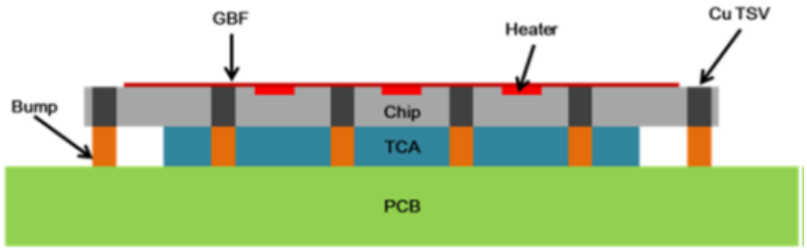

Figure 2.7 : Schematic of 3D TSV model with GBF heat spreader (not scale). [28]

Graphite can be used as heat spreader to spread the heat to a larger surface area, or in an arrangement of materials or composites to maximize thermal performance and reducing overall thermal resistance. In [29], the use of high thermal conductivity graphite spreader below a single-sided PCB is explored to enhance heat transfer. A thin graphite layer of 0.05 mm thickness and 0.02 mm combined adhesive and encapsulant are used in the study. The overall effective graphite thickness is 0.07 mm. The effective conductivity used is 1214 W/(m.K) in the in-plane direction and 0.5 W/(m.K) in the cross-plane direction. The steady state junction temperature with the spreader behind the PCB is reduced by 3.9°C, decreasing from 110.1°C to 106.2°C (4.5 % reduction with respect to ambient compared to the same configuration without the spreader).

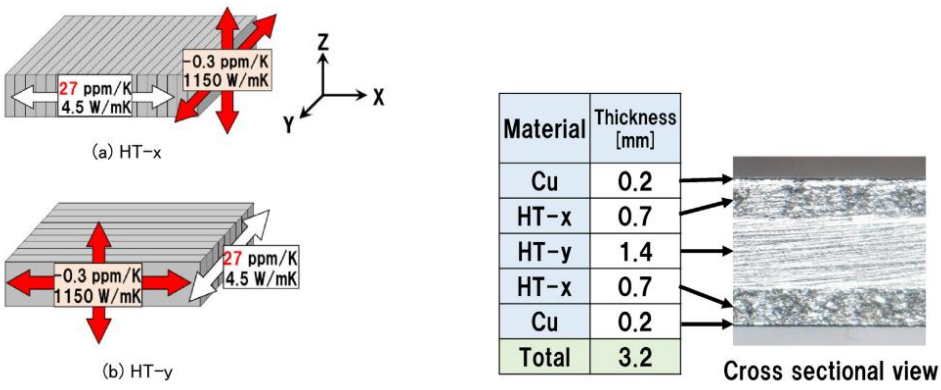

Figure 2.8 : Arrangement of graphite sheets and lamination structure [30].

To take advantage of the high in-plane thermal conductivity of graphite, graphite sheets are arranged vertically in [30] to form larger plates, so that the highest thermal conductivity is in the vertical direction. Then, three plates of graphite are stacked, between two layers of Cu, with 90° rotations since the thermal conductivity is high and the CTE is low in the Y and Z directions,

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with the opposite being the case in the X direction (Figure 2.8). A 15 % reduction in thermal resistance is achieved compared to using copper only. It is remarked that despite high thermal conductivity of the graphite, this arrangement of graphite can have disadvantages in terms of high fabrication cost.

Thermally Annealed Pyrolytic Graphite (TPG) offers in-plane thermal conductivity of more than 1500 W/(m.K) as reported in [31] where TPG is encapsulated between Cu (Cu/TPG/Cu), with a TPG ratio of 68 %. The TPG sheets are arranged vertically in a way that orients the high thermal conductivity in the vertical direction (Figure 2.9). With such an arrangement, an equivalent thermal conductivity of 760 W/(m.K) in vertical direction is achieved. A reduction of 17 % in thermal resistance is obtained compared with conventional DBCs, and less thermal cross-coupling heat transfer between MOSFETs is observed providing they are arranged along the direction with poor thermal conductivity.

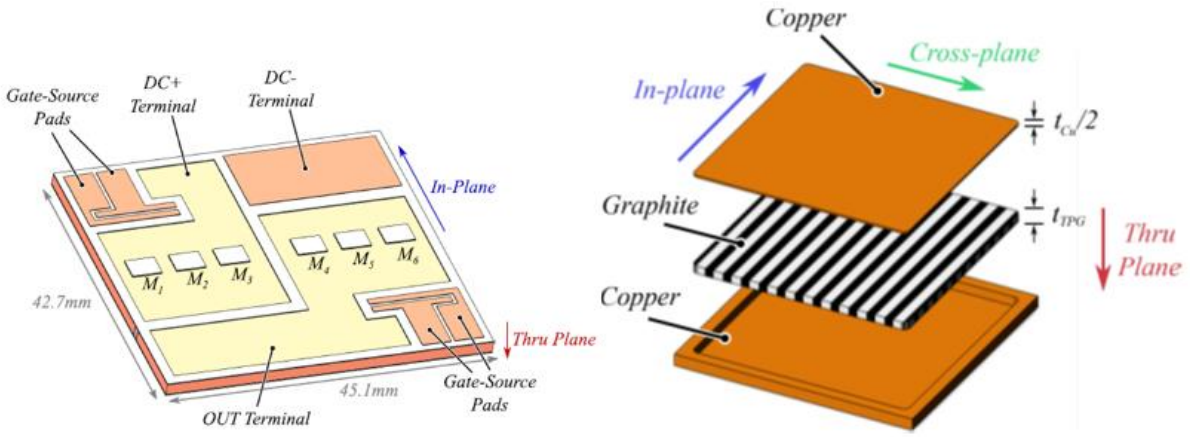

Figure 2.9 : TPG-embedded structure with copper encapsulant [31].

Composites of graphene and some other conductive materials can be used to reach good thermal conductivity as well as improving mechanical and electrical properties of the heat spreader. In [32], the impact of using copper foams coated with graphene by chemical vapor deposition is investigated. Improvements in electrical, thermal, and mechanical properties are observed. The equivalent thermal conductivity of the composite is increased by 17 % and the CTE is reduced by 61 % compared with copper. In [10], various heat spreader materials are studied to be integrated in radio-frequency (RF) systems which can operate in very challenging conditions, in military and aerospace applications. A composite material that has less weight, lower CTE (compatible with semiconductor chips), good thermal conductivity and is compatible with PCB manufacturing process in terms of the sheet size and thickness, is needed.

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The Cu-MetGrafTM-7 copper-graphite composite is selected for evaluation and manufacturing process development due to its low value of CTE (7 ppm/K) which is tailored to meet different requirements. Copper-graphite sheets are manufactured successfully in the sheet size required for PCB fabrication, with thickness of 0.51 mm. Also, a model to determine the effective thermal conductivity for a PCB sample containing a single layer of Cu-MetGraf-7-300 is developed. Model results for a thirteen-layer PCB showed an overall PCB effective thermal conductivity of 87.5 W/(m.K). Experimental results give 89 W/(m.K) [10].

Graphite is a very suitable material for heat spreading because of its high in-plane thermal conductivity. However, it lacks high thermal conductivity in the cross-plane direction which increases the resistance for the heat to cross graphite sheet. More work is needed to maximize thermal performance of graphite-based heat spreaders by finding out an arrangement that improves its cross-plane effective thermal conductivity. In addition, finding a way of embedding graphite sheets in a PCB near the chip, compatible with the existing PCB fabrication process, can improve heat spreading and reduce chip junction temperature and hot spots.

2.2 Heat extraction

Once the heat dissipated by the small semiconductor chip has been spread over a larger surface, it is more easily removed by convection heat transfer. The objective is to remove as much heat as possible to the ambient or the surrounding medium for a given temperature difference between components and ambient. The standard approach to achieve that is to enlarge the heat exchange surface area in contact with the cooling fluid by using heat sinks with fins and channels (equation (2.1), where A_s is the heat exchange surface, Q is the dissipated heat, h is the heat transfer coefficient, and ΔT is the temperature difference). Many geometries have been used to enlarge the heat exchanging surface area of the heat sink such as straight fins, pin fins, microchannels in different shapes.

$$Q = h \times A_s \times \Delta T \tag{2.1}$$

Convection heat transfer depends on the properties of the cooling fluid (dynamic viscosity, thermal conductivity, density, specific heat capacity), the properties of the flow (velocity, flow type - laminar or turbulent - and its direction - parallel or perpendicular to the heat exchange surface - as well as the properties of the solid surface (geometry and roughness). For example, the specific heat capacity of water is almost four times that of the air (4.182 kJ/(kg.K)) for water compared to 1.005 kJ/(kg.K) at constant pressure). Also, the thermal conductivity of the water is 25 times that of the air.

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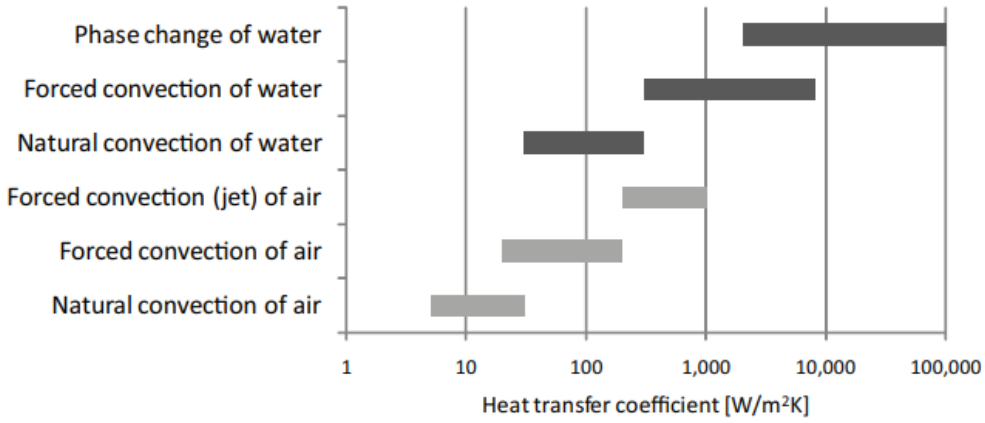

Figure 2.10 : Heat transfer coefficient of air and water in various flow conditions [33].

It can be noticed in Figure 2.10 that phase change heat transfer can reach even higher values of heat transfer coefficient by taking advantage of latent heat transfer regime at constant temperature, especially in the phase change from liquid to gas used in cooling solutions such as two-phase microchannel, spray cooling, and vapor chamber.

The higher the power loss density of the heat source the more need there is for high heat transfer coefficients to be achieved (Figure 2.11). Getting closer to the heat source, by embedding heat extraction solution nearer to the heat source, or even placing it in direct contact with the source, improves heat extraction. That is because the heat is exposed directly to the coolant, which eliminates all the thermal resistances of intermediate layers.

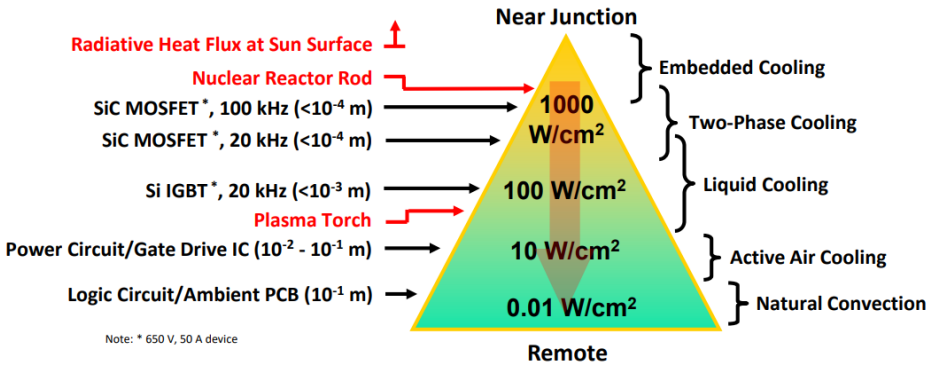

Figure 2.11 : Near junction cooling technique for higher power density [34].

The following sections present a review of different convection heat transfer cooling techniques starting by air cooling, liquid cooling, and two-phase cooling solutions.

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2.2.1 Air cooling

Air cooling can be considered to cool a low power loss density system that dissipate low heat flux. It is simple and cheap in its both forms, natural and forced air convection.

2.2.1.1 Air natural convection

Natural convection occurs when density of air in proximity to hot heat exchange surface decreases due to an increase in air temperature, resulting into the hotter lighter air to rise, replaced with cold air. This density difference in combination with the gravity force results in circulating flow. Since there is no external driving force, it is called natural convection. The heat transfer coefficient for natural convection in air is generally low, of the order of 10 W/(m².K), resulting in a heat flux of only ~0.01 W/cm² for a typical temperature difference of say 10°C.

In order to increase convection heat transfer, the heat exchange surface must be increased. This can be seen in heat sinks where fins and different shapes are made to increase the area of heat exchange surface and therefore, increasing convection heat transfer. Natural air cooling can be considered to cool a system that dissipates very low heat flux. It is the simplest and the cheapest thermal management technique.

2.2.1.2 Air forced convection

Air forced convection occurs by forcing air towards the heat exchange surface with a certain speed using an external device (Figure 2.12). The higher the air speed, the higher the heat transfer coefficient. A heat sink can always be used to maximize heat exchange surface and therefore increasing heat dissipation.

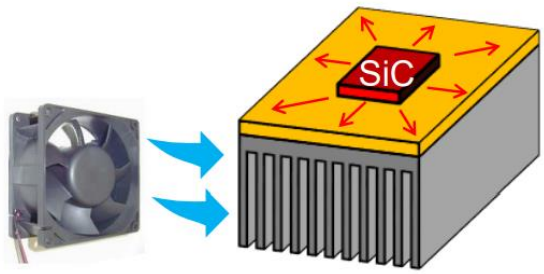

Figure 2.12 : Air forced convection [34].

A fan is the conventional way to speed up the air to cool a heat-exchange surface. For example, it can be found in the thermal management system of our computers. Fans have rotating parts which make them noisy and they need some level of maintenance. In addition,

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fans cooling system can take a large volume as they are usually associated with a heat sink. The heat transfer capability can deal with power loss densities in the range of tens of W/cm² [7].

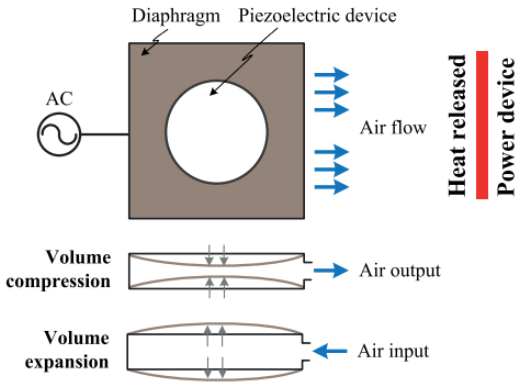

Figure 2.13 : Dual-piezoelectric cooling jet (DCJ) [7].

An example of fan suited to very small (embedded) thermal management solutions is the Dual-piezoelectric cooling jet (DCJ). It is more compact, has less power requirements and produces less acoustic noise. DCJ is composed of two piezoelectric metal plates mounted on diaphragm (Figure 2.13). When applying an AC voltage to piezoelectric materials, the structure is compressed to blow the air and expanded to suck the air in continuous motion. Piezoelectric devices can deal with heat fluxes in the range of ~1 W/cm² [7]. In [35], the concept of integrated thermal management system is investigated by embedding heat pipes, graphite sheet and DCJs in a low power PCB (40 W) with five MOSFETs using additive manufacturing. It was found that adding three DCJs reduce thermal resistance by almost 50 % [35].

Air jet impingement is another air forced convection cooling technique where air is pumped into single nozzle or multi-nozzles system to impinge air on a heat exchange surface with higher velocity than conventional fans, and therefore higher heat transfer capability. Dissipated heat flux can reach ~60 W/cm² [36]. Air jet impingement systems have external parts, such as an air pump, which can require some regular maintenance. In [37], air jet impingement directed at a heat sink attached to a vapor chamber for the thermal management of a high power SiC chip at a power loss density of 500 W/cm². Air is delivered using an air blower to provide a constant inlet volume flow rate of ~0.01 m^3/s at a temperature of 38°C. Air then passes through a screen mesh and then a honeycomb structure to straighten the airflow before the orifice which is the air jet (Figure 2.14).

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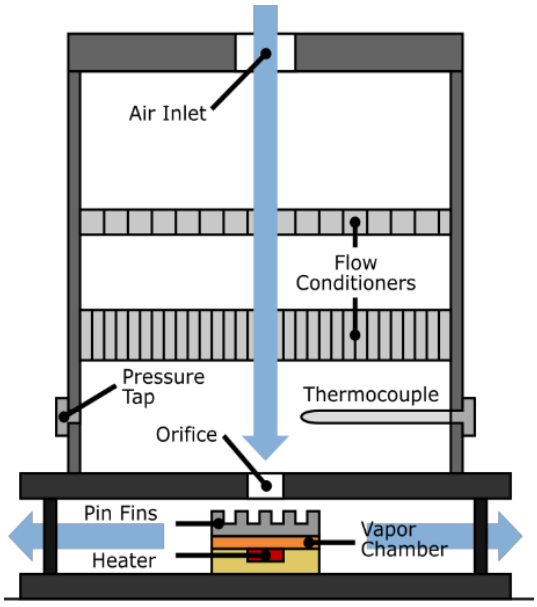

Figure 2.14 : Air jet impingement [37].

Air cooling techniques are the best established techniques for power electronics cooling. However, their heat removal capabilities are limited which makes them suitable for low power density losses only.

2.2.2 Liquid cooling

Liquid cooling techniques are more suitable for high power loss density applications (500-1000 W/cm²) due to their high specific heat capacity. Therefore, liquids have the capability to transfer more heat from heat exchange surface which will help decreasing thermal resistance. However, liquids have higher density than air which will cause an increase in pressure drop requirements to pump the same volume flow rates. The increase in pumping power requires larger pump which will add to volume, weight, cost, and maintenance level.

There are various implementations of liquid cooling. The basic technique is forced convection between the liquid and the heat exchange surface. The heat exchange surface could be a base plate in contact with the flowing liquid. This technique is called cold plate cooling and it can remove heat fluxes in order of tens of W/cm² [7]. By increasing the surface area of the heat sink cold plate (straight fins, pin fins, metal foams, microchannels, etc.), the heat transfer capability increases.

In [38], the thermal performance of a metal foam heat sink is studied numerically. Metal foam has advantages such as light weight (since most of the volume is formed with voids), large heat exchange area per unit volume, and complex path for the fluid (which enhances fluid

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mixing and improves heat transfer). Using metal foam is compared to pin fins, and a hybrid heat sink with metal foam and embedded pin fins (Figure 2.15).

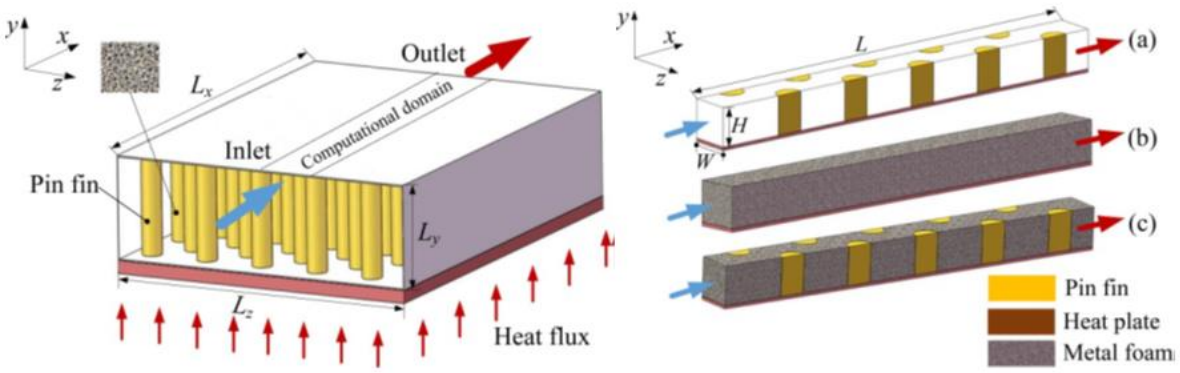

Figure 2.15 : Metal foam and pin fin heat sink [38].

At a power loss density of 100 W/cm², the thermal performance of the hybrid heat sink is found to be 266.6 % and 36.3 % higher than that of the traditional pin fin heat sink and metal foam heat sink respectively. However, it must be also noted that a larger pressure drop is observed for the hybrid heat sink, due to the increase in friction in the hybrid heat sink. In addition, it is found that this pressure drop is sensitive to the pore density and that metal foam porosity and pores density influence the thermal performance [38].

2.2.2.1 Microchannel heat sink

The microchannel cooling technique is a development of the conventional cold plate cooling, with channels made on the heat exchange surface having a hydraulic diameter in the order of micrometers. Microchannels provide enhancement by increasing the surface area in contact with the coolant, which improves heat flux dissipation (can reach 1000 W/cm² [7]) and reduces the overall thermal resistance.

In [39], the performance of a water microchannel heat sink made of silicon (Si) is studied experimentally by dissipating 1250 W over six chips of 0.5 cm² each, corresponding to a heat density of 417 W/cm². The junction-to-coolant inlet thermal resistance obtained is about 16.2 K.mm²/W (0.324 K/W). In [40], an integrated microchannel heat sink cooled with water is developed by fabricating microchannel directly on the back-metallization of a DBC or active metal braze (AMB) ceramic substrate populated with two diodes and two IGBT, producing a total heat of about 1320 W (power loss density of 604 W/cm²). The microchannel heat sink is able to achieve a junction-to-inlet water thermal resistance of about 17 K.mm²/W for the IGBTs and 14 K.mm²/W for the diodes.

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Furthermore, in [42], a near-junction silicon straight microchannel cooler is fabricated in a silicon and studied experimentally. The design is compact (Figure 2.16) with power loss density of 127 W/cm² dissipated from a 1 cm² SiC MOSFET. The junction-to-water inlet thermal resistance is found to reach about 0.15 K/W using water as a cooling fluid.

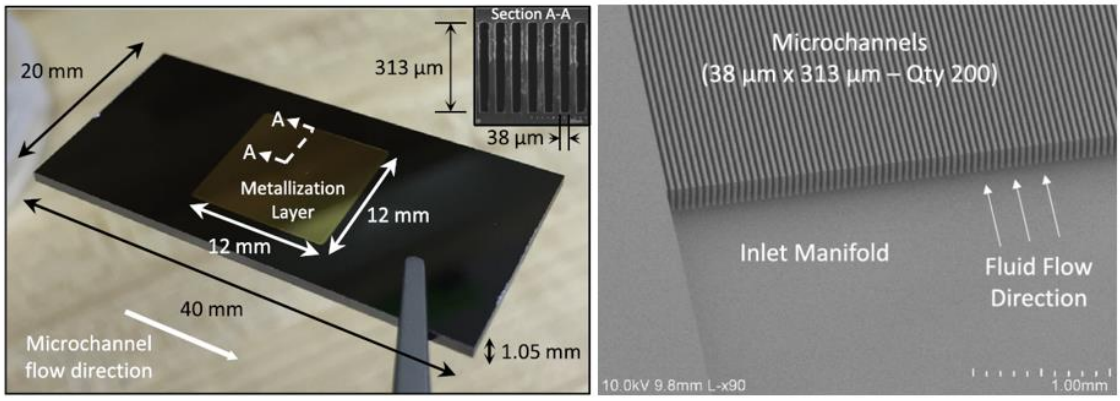

Figure 2.16 : Microchannel heat sink [42].

Getting closer to the heat source by making microchannels directly on the chip improves heat transfer efficiency further. In [41], ultra-thin water cooled microchannels are etched in a silicon chip. The microchannel heat sink demonstrates good thermal performance under a power loss density of 700 W/cm², achieving a thermal resistance between chip junction and water inlet temperature of 9.3 K.mm²/W.

Using coolants other than water can improve cooling performance by achieving higher heat transfer coefficient. For example, nano fluids can increase the heat transfer capability of water by adding nano particles of another material to water. The nanoparticles can be made of metals, oxides, carbides, or carbon nanotubes, while the base fluids can be water, ethylene glycol, and oil [43].

Figure 2.17 : Nano fluid of TiO_2 in different concentrations [44].

In [44], the effect of using a nano-fluid as a coolant for a microchannel heat sink is experimentally investigated. Titanium dioxide (TiO2) is used with different concentrations in water up to 1 % mass fraction (Figure 2.17). Using nanofluids instead of water as the coolant

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decreased the substrate temperature by up to 18.5°C and reduced the thermal resistance by as much as 42.4 %. The 0.5 % TiO2 nanofluid increases the heat transfer capacity by up to 38.6 % compared to using water for the tested conditions. Thermal resistance decreased by increasing TiO2 mass fraction (Figure 2.18). It is concluded that using nanofluids instead of water as the coolant significantly improves thermal performance particularly for high ambient temperatures [44].

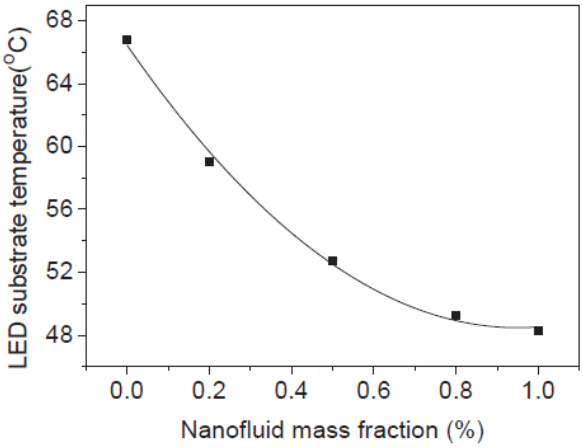

Figure 2.18 : LED substrate temperature variation with nanofluid mass fraction [44].

Despite the advantages of microchannel cooling, the reduction of microchannels hydraulic diameter leads to an increase in pressure drop which results in larger pumping power requirements and higher cost. In addition, the coolant will need filtering to prevent clogging in microchannels, which adds to the complexity of the cooling system [45].

2.2.2.2 Jet impingement

Liquid jet impingement cooling is based on hitting a hot surface normally with a flow of liquid at a suitable flow rate and temperature. This flow then spreads on the hot surface providing convective heat transfer between the coolant and the surface. Liquid jet impingement cooling techniques can achieve high heat transfer capacities enabling cooling of high-power density applications, up to 2000 W/cm² [46] [45].

Jet impingement cooling systems can contain a single jet or multiple jets arranged in arrays to cover the cooled surface. Jet impingement cooling depends on several parameters, such as jet nozzle diameter, jet velocity, distance from jet nozzle to the surface and flow properties. This makes such systems complex to design. Liquid jet impingement cooling can be combined with a microchannels structure for cooling enhancement or other forms of heat sinks fins, as will be seen in the following review.

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In [47], a jet impingement cooling system is designed (with 50 % – 50 % mixture by volume of water-ethylene glycol as a high temperature coolant at 70°C) on a copper base plate and numerically investigated with and without micro-finned enhanced surfaces, and a plastic fluid manifold. It is compared with conventional channel flow heat exchangers. A heat density of 275 W/cm² is applied to four diodes. Numerical results indicate that the jet-based heat exchanger reduce thermal resistance by up to 45 %, increase in power density by 79 %, and increase specific power with respect to the baseline channel-flow heat exchanger by 118 % [47].

Surface enhancement improves flow conditions for better heat transfer capacity as well as it increases heat exchange surface area. Coolant jet is impinged on a surface with microchannels, pin fins or other forms of surface enhancements. In [48], jet impingement with water is numerically studied to cool under a heat density of 500 W/cm² with (Figure 2.19). It is found that convex dimples show the best cooling performance, with respect to the configuration without dimples, with mixed dimples, and with concave dimples. The convex dimple structure can effectively reduce the flow resistance when the mass flow rate is high and, therefore, reduce the pressure drop.

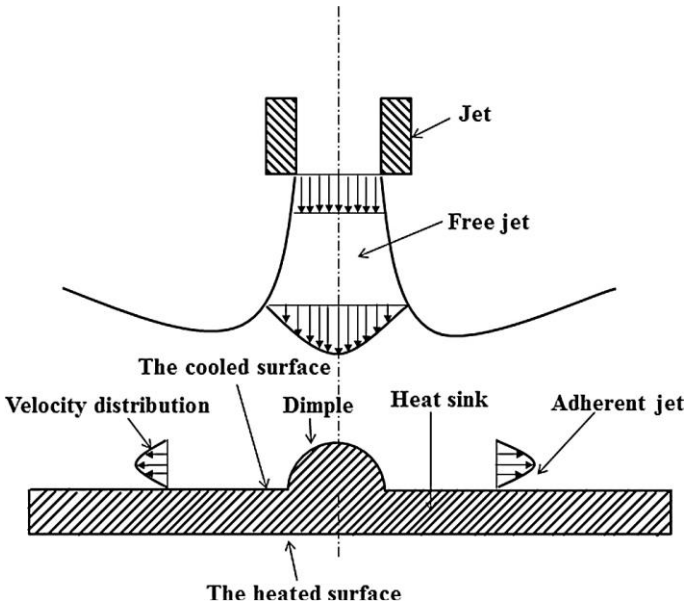

Figure 2.19 : Jet impingement on surface with dimples [48].

In another study [49], a jet impingement cooling system with micro-pin fin heat sink designed and simulated numerically. Every inlet nozzle is surrounded by four outlet nozzles. Several configurations with different pin-fin and nozzle geometries are investigated and compared. A total thermal resistance of 9.37 K.mm²/W is achieved and a maximum dissipated

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heat flux of 700 W/cm² with only 2.33°C of temperature nonuniformity of the heating surface. It is concluded that the jet impingement cooling system with micro-pin fin heatsink shows good temperature uniformity and high heat flux cooling [49].

In [42], a near-junction jet impingement, enhanced with microchannels is fabricated and studied experimentally on a silicon chip (Figure 2.20). The chip-size cooler is able to dissipate up to 1.02 kW/cm² over a 0.25 cm² area. A maximum average heat transfer coefficient of 120.2 kW/(m².K) and a pressure drop of 81.2 kPa are achieved at a 0.45 L/min water volume flow rate and an inlet temperature of 50°C. It is concluded that near-junction cooling technologies can enable a considerable reduction in power package size (5 to 10 times) when compared with traditional indirect and remote cooling strategies [42].

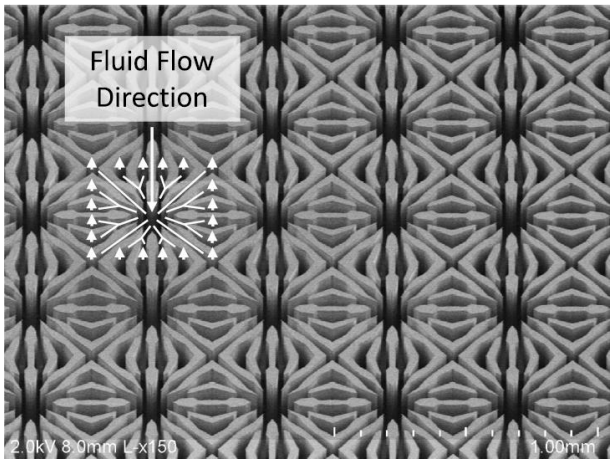

Figure 2.20 : Near junction jet impingement on a silicon unit cell. [42]

The heat exchange performance at the solid/liquid interface is not the only parameter affecting thermal resistance. The composition and structure of the material stack located between the heat source and the solid/liquid interface are also very important. The closer the coolant to the heat source, the better the cooling capacity achieved since thermal resistance is reduced by eliminating TIMs and other layers in the way that have low thermal conductivity. In [50], the effect of direct water, single nozzle jet impingement on the thermal performance of the cooling system of a MOSFET with a power density of 127.5 W/cm² is investigated . The results show a thermal resistance of 110 K. mm²/W in the case of direct cooling with no TIM, and 165 K.mm²/W in the case of indirect cooling with TIM, achieving 30 % reduction in thermal resistance (Figure 2.21). The TIM material with a thickness of about 200 μm is found to significantly contribute to the total thermal resistance. The heat transfer coefficient achieved is 12000 W/(m².K) in the case without TIM, and 6000 W/(m².K) in the case with TIM. This

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result shows the importance of “direct” liquid jet impingement cooling, i.e. to have a very short path between the power sources and the cooling surfaces [50].

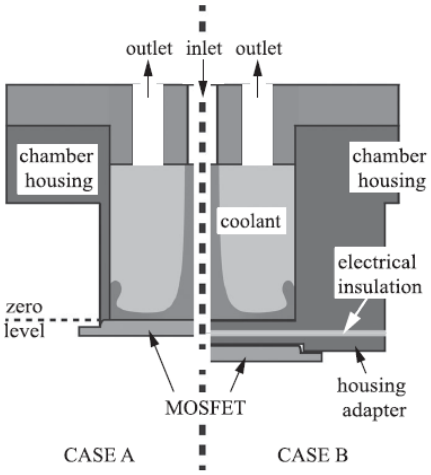

Figure 2.21 : Single jet impingement with direct and indirect cooling configurations [50].

For more heat removal, an immersed direct jet impingement cooling device (with distributed returns between jets to prevent interference between adjacent jets) is designed, fabricated, and tested [51]. In that design (Figure 2.22), the chip is immersed in dielectric water and the water is impinged on all chip surfaces providing full chip cooling. The maximum effective heat transfer coefficient achieved is 41377 W/(m².K) at 160 W/cm² heat density. It is concluded that full chip cooling can provide high heat dissipation and is useful for high power density [51].

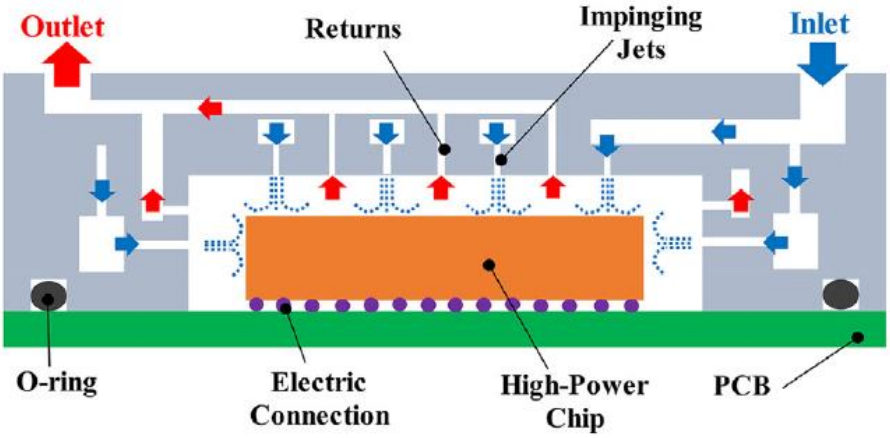

Figure 2.22 : Immersed direct jet impingement [51].

In [52], the thermal performance of a liquid jet impingement cooling system with multi-micro nozzle is investigated numerically for a Si-IGBT power module. The effect of coolant mass flow rate and ratio of the micro-nozzle (the ratio between the inlet and the outlet diameters of the nozzle) at a range of heat flux up to 250 W/cm² on the cooling performance and pumping

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power are investigated. The results show that a power density of 250 W/cm² and an operating temperature of 117°C can be reached with nozzle ratio of 0.45 at a volume flow rate of 0.57 L/min, and a pumping power of 0.25 W [52].

In [53], a multi-jet impingement cooler based on cost-efficient polymer fabrication techniques is studied numerically and experimentally for high-power applications. With a 4×4 nozzle array, it can achieve heat transfer coefficients of up to 62500 W/(m²·K) with a pumping power as low as 0.3 W. The multi-jet layout results in a lower thermal resistance and a better temperature uniformity for the same volume flow rate compared with a single-jet design. It is concluded that direct cooling on the backside of the semiconductor device is more efficient than cooling the substrate or the base plate. Also, the simulations show that thermal conductivity of the cooler's material has a negligible impact on the chip temperature distribution over a wide range of flow rates and chip power values as shown in Figure 2.23 [53].

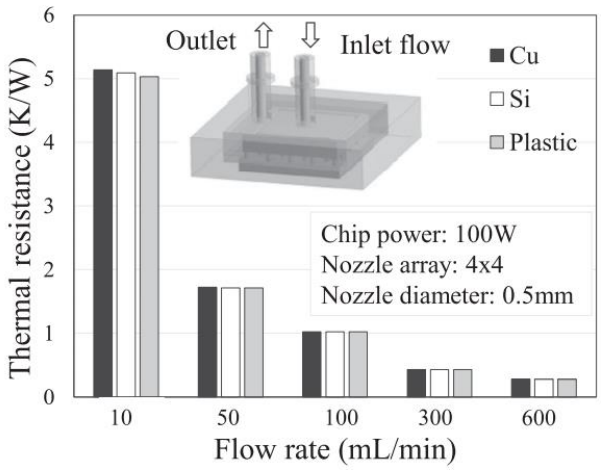

Figure 2.23 : Thermal resistance variation with flow rate and cooler material [53].

In a further study [54], a 3-D printed package-level polymer jet-impingement cooling system is investigated numerically and experimentally using deionized water on a 23×23 mm² thermal test chip with 1-kW power dissipation. The experimental results show that the measured average chip temperature increase is 65°C with a cooler pressure drop of 0.15 bar. A 2-stage manifold, with an additional flow redistribution layer having 3×3 nozzles before the 11×11 impingement nozzles (Figure 2.24), is found to improve chip temperature uniformity. The chip temperature gradient is reduced by a factor of 4 and 2.3 for a volume flow rate of 0.5 and 3 L/min, respectively, while no significant impact on the cooler pressure drop is measured. The numerical studies predict an additional 15.4 % improvement in thermal performance by decreasing the nozzle pitch from 2 to 1 mm, for a volume flow rate of 3 L/min. It is also

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concluded that bare die direct cooling without lid and thermal interface material (TIM) shows better cooling performance than the lidded package.

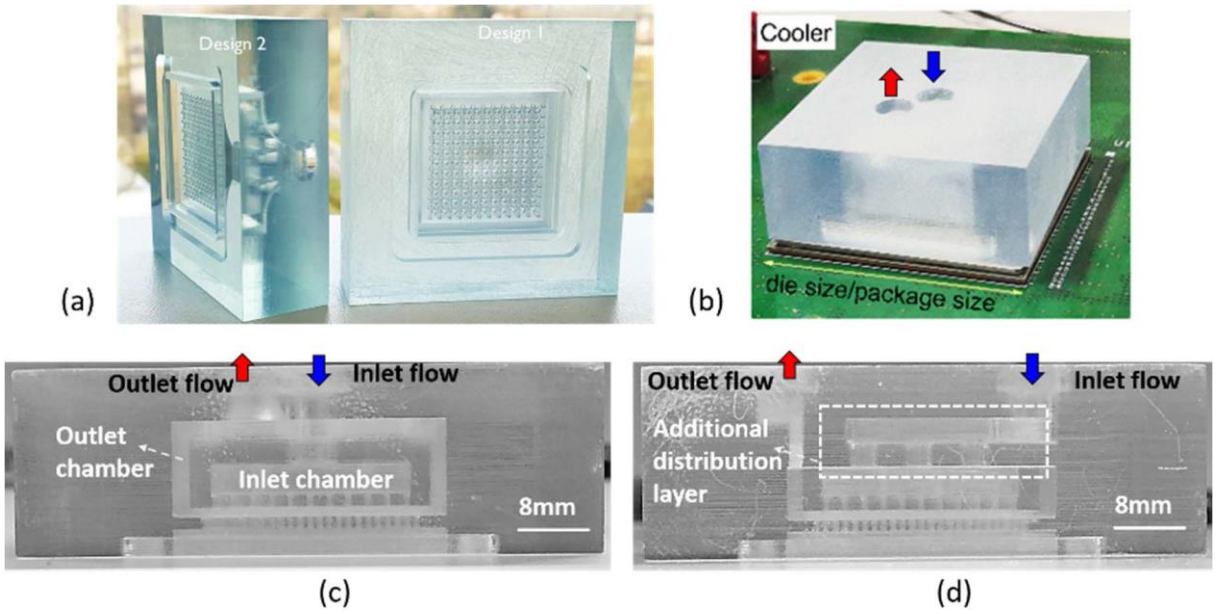

Figure 2.24 : 3-D printed package-level polymer jet impingement cooling system [54].

Clearly, the direct cooling is more performant thermally than the indirect cooling. However, high voltage isolation requirements should be taken into consideration, since the application of power electronics studied in this thesis often operate at relatively high voltages.

Liquid jet impingement can achieve high heat transfer coefficient values (can reach ~60000 W/(m²K)), which makes it suitable for high power loss density applications. However, it depends on many geometrical and fluid parameters which complicate its design. An efficient design is needed to optimize for less pressure drop requirements to circulate the liquid while maintaining high thermal performance.

2.2.3 Two-phase cooling

Two-phase cooling means that some or all of the cooling fluids change phase in the heat exchange. When enough heat is delivered to a liquid coolant, boiling starts to take place and vaporization changes the phase of the coolant from liquid to gas (vapor) at a constant temperature (latent heat transfer) (Figure 2.25).

Two-phase cooling improves the heat transfer performance compared to single-phase cooling due to the latent heat transfer mechanism where liquid evaporates at constant temperature [7][8][45]. This means that lower flow rates are required to dissipate the same amount of heat. In addition, isothermal heat transfer enhances temperature uniformity of the

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cooling surface. A two-phase flow is less viscous than a purely liquid flow, which means pressure drop is lower at the same volume flow rate. That can save some pumping power in addition to size, weight, and cost since smaller pump and reservoir are going to be needed. According to [7], the main disadvantage of two-phase cooling systems can be their complexity.

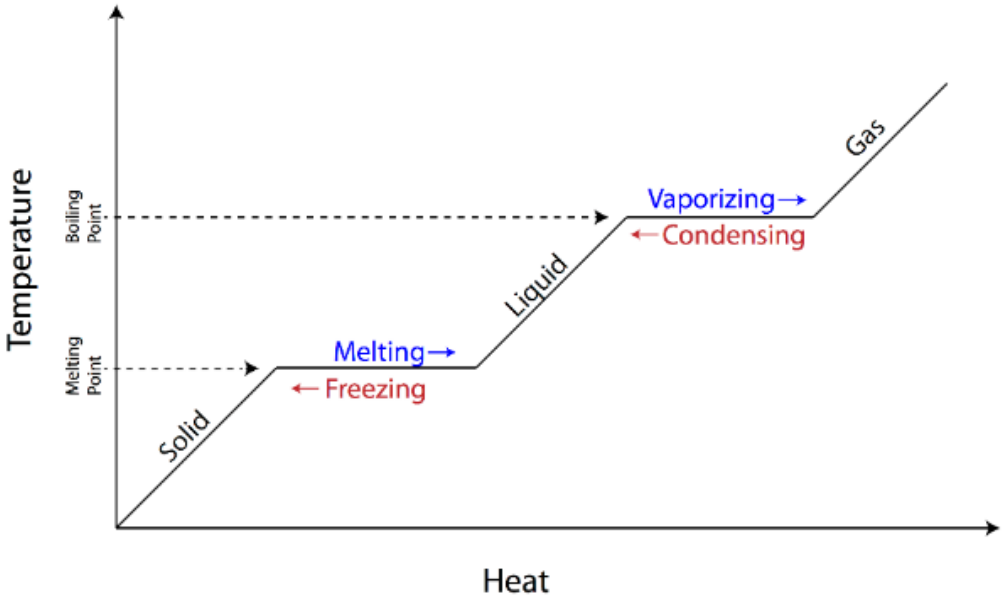

Figure 2.25 : Phases change for water [55].

Two phase cooling can be applied to many configurations seen before for single-phase cooing, such as cold plate heat sink, or microchannel. It can also take place from solid to liquid using phase change materials to absorb heat for thermal management. Despite the good thermal performance, two-phase system can have some drawbacks, such as flow instability issues and difficulty in predicting flow behavior, and still require more investigations [45].

2.2.3.1 Phase change material (PCM) cooling

In [56], the thermal performance of phase change material (PCM)-based cascade cooling systems with an integrated heat sink is evaluated experimentally. Paraffin waxes are used as PCM, in between the fins of a heatsink. As illustrated in (Figure 2.26), the PCM with a specific heat capacity of 2.9 kJ/(kg.K) absorbs heat from the hot surface until it reaches its melting point at 330 K, at which point it starts absorbing latent heat (Figure 2.26-a). When the PCM is liquified, the heat is extracted to the ambient by natural convection. Multi-stage PCMs can be used with different melting points to absorb more heat (Figure 2.26-b). Results show a reduction in fin peak temperature from 123.4°C to 107.2°C in one heat-supply cycle. The peak temperature is reduced by 13.1 % compared to natural convection. In addition, the time to reach

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the maximum allowed peak temperature is reduced by 45 %, which can increase lifetime of the system and prevent failure as concluded in [56].

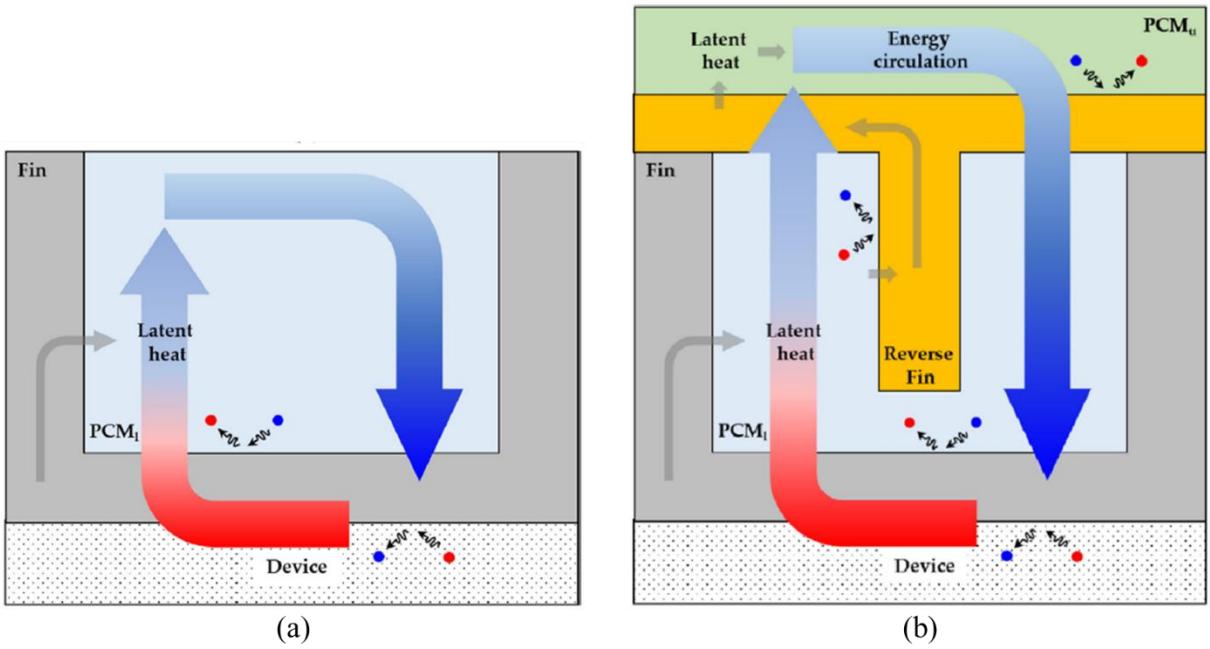

Figure 2.26 : Schematic illustration of thermal energy transport of a PCM-based cascade cooling system (a) between multi-stage PCMs and (b) through single-stage PCM [56].

2.2.3.2 Two-phase microchannel

Two-phase cooling can be applied to a microchannel heat sink. The thermal performance of two-phase cooling of a silicon microchannel heat sink cooled by refrigerant R236fa is studied in [57]. With a power density up to 255 W/cm², the chip temperature can be maintained below 52°C for a coolant inlet temperature of 10°C. It is concluded that two-phase cooling can keep the chip at a temperature 13°C lower than single-phase liquid cooling at the same pumping power and a heat flux of 350 W/cm².

In another study [58], a reduced order single/two phase thermal-fluidic model is developed to study the thermal performance of microchannel heat sinks and investigate the effect of micro-channel geometric parameters, packaging materials and flow conditions. By applying a power loss density of 1000 W/cm², it is found that single-phase flow using water performs worse than two-phase flow using R245fa. In addition, embedded cooling reduces conduction thermal resistance and provides a shorter path for the coolant flow which reduces pressure drop. The proposed embedded micro-channels with 3D-manifold with R245fa working fluid has the potential to achieve a low thermal resistance of about 0.07 K/W.

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Furthermore, in [59], a microchannel thermal management systems with two-phase flow is studied experimentally using the refrigerant R1234yf with low boiling point (-29°C) and low global warming potential. The results show that the thermal management system can dissipate a heat flux of 526 W/cm² while maintaining the junction temperature below 120°C. The system is expected to manage a heat flux as high as about 750 W/cm² for SiC MOSFETs with a junction temperature of 175°C [59].

The previous studies show that applying two-phase cooling on microchannel heat sinks can lead to higher heat dissipation and thermal performance than single-phase cooling as well as lower pressure drop and power consumption.

2.2.3.3 Spray cooling

In spray cooling, the nozzle sprays liquid droplets of the coolant on a heated surface (Figure 2.27). These droplets form a thin fluid film and exchange heat with the heated surface by convection. If the film starts vaporizing, then two-phase cooling takes place. Two-phase spray cooling takes advantage of latent heat transfer to achieve high heat flux dissipation that can reach up to 1200 W/cm² with proper surface roughness [60].

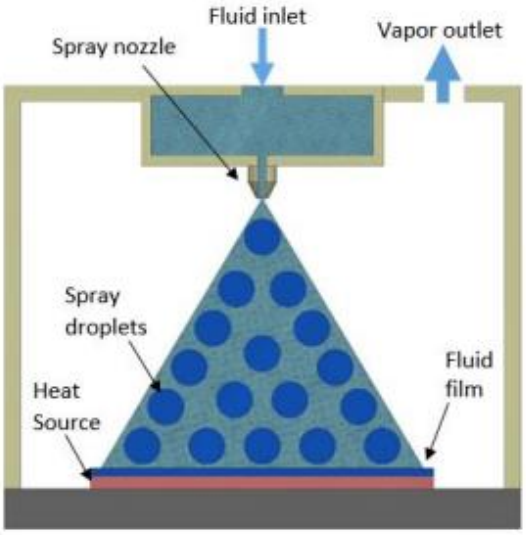

Figure 2.27 : Spray cooling chamber [45].

To generate spray droplets, there are two mechanisms [45]:

- Pressure spray: injecting the liquid at high pressure through a nozzle, resulting in a liquid breakup into droplets. It depends on one working fluid (no air flow is required) which simplify the cooling system.

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- Atomized spray: injecting the liquid with a high-speed flow of air breaks up the liquid into droplets. It generates smaller droplets at lower flowrates which improves heat removal and power consumption [61].

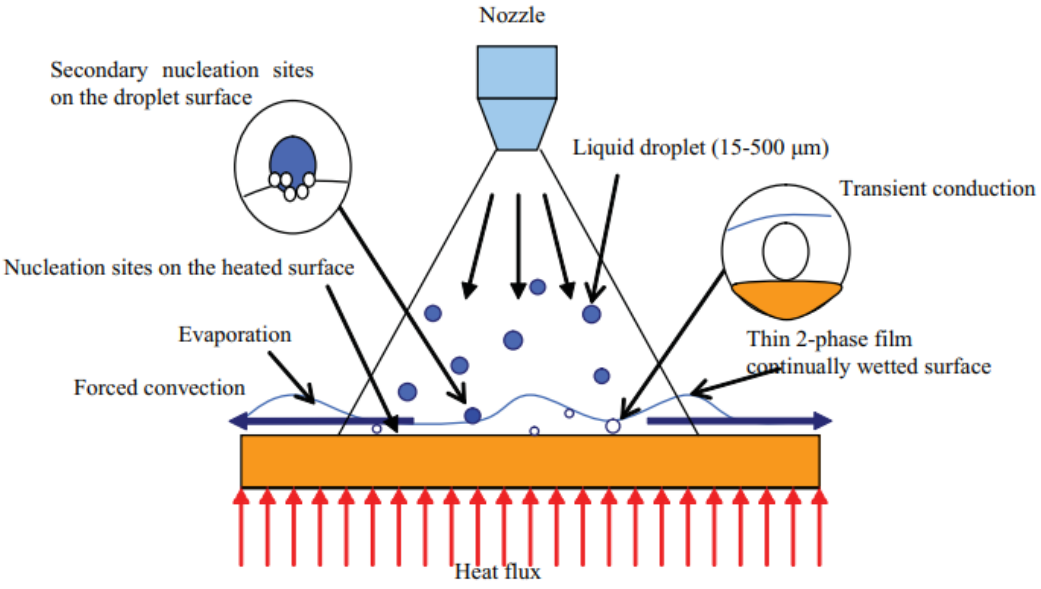

Figure 2.28 : Heat transfer mechanisms of spray cooling [62].

Once the liquid droplets hit the heating surface, there are four major heat transfer mechanisms (Figure 2.28) [60] [63] [64]:

- Evaporation from fluid film surface.
- Forced convection due to droplets impingement on the heated surface.
- Nucleation on the heated surface.
- Secondary nucleation on the surface of spray droplets.

The spray cooling technique enhances heat transfer by providing an increase in heat exchange area between fluid and hot solid surface by distributing the droplets over a larger surface as well as high uniformity in droplets distribution on the heated surface which improves temperature uniformity on the surface [61]. In [65], the viability and the implementation a two-phase spray cooling solution for hybrid vehicles electronics is studied in a power loss density range of 200 W/cm². Commercial coolants are investigated with respect to thermal performance, environmental impact, safety, and material compatibility. By using integrated models in a systematic methodology to predict cooling performance, and by experimental

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validation, it is concluded that HFE-7100 is the optimum coolant and that two-phase spray cooling is an effective cooling technique for hybrid vehicle electronics.

In [66], the standard heat sink (cooled by 25°C coolant) of a 3-phase inverter (12 IGBTs), used in an automotive application, is replaced with a pressure-atomized evaporative spray nozzle array with 50/50 mixture of cooling water and propylene glycol (WPG) at 100°C which is the temperature of the automotive application environment. The objective is to resolve the issue of overheating of IGBTs chips when working in automotive environment at 100°C with standard heat sink coolant. The results show that the IGBTs can work at 140 W/cm² with spray cooling system compared to only 43 W/cm² in the case of normal single-phase convective cooling, and without exceeding a junction temperature of 125°C. The increase in IGBTs power loss density means an increase in inverter power load from 45 kW to 153 kW and even 180 kW at 127°C junction temperature and 165 W/cm² power loss density. These results are compared to another study from the same authors [67], this time comparing spray cooling systems using water at 95°C instead of WPG at 100°C. It shows that water spray cooling achieves an IGBTs junction temperature about 10°C lower than WPG spray cooling, with a substantial improvement over standard single-phase convective cooling. It is also concluded from these studies that using a high-temperature coolant allows for a reduction in condenser size, weight and cost.

In [68], a spray cooling system is developed and experimented for the cooling of power inverter modules used in automotive applications (Figure 2.29). Two IGBTs with power loss density of 400 W/cm² are cooled by two pressure atomized nozzles using antifreeze coolant that boils at 90°C and freezes at -25°C. The heat transfer coefficient fat the spray surface id found to reach 280000 W/(m².K), with good temperature uniformity.

In [69], the effect of the spray cone angle on thermal performance of two-phase spray cooling system is studied experimentally at a power density of 138 W/cm² on a heated surface using dielectric refrigerant R134a as a coolant. By testing three different types of nozzles designs for different flow rates, it is found that when decreasing the spray cone angle, there is a delay in the onset of the nucleated boiling regime which results in a reduction in thermal performance. Also, by decreasing the spray cone angle, the film thickness increases in the nucleated boiling regime.

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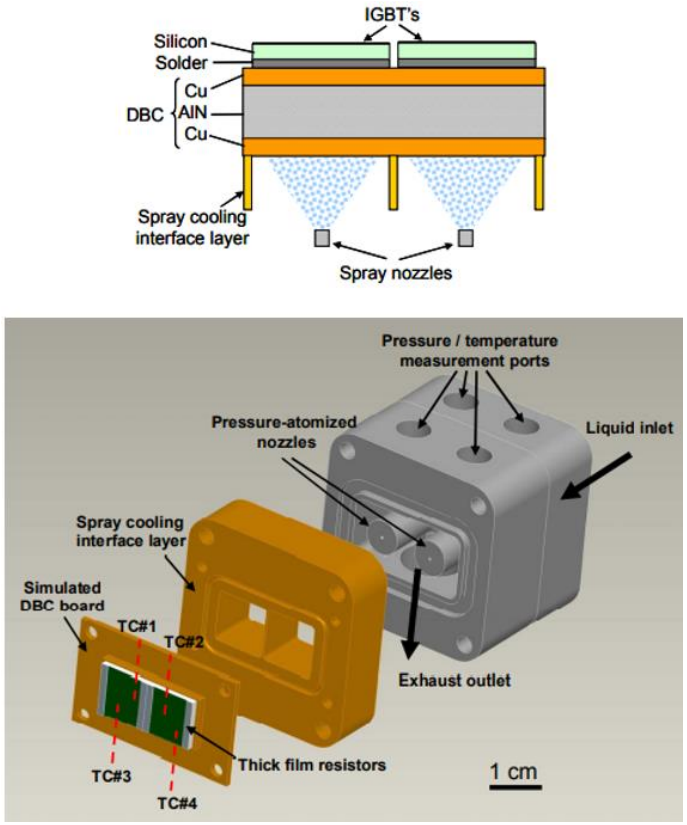

Figure 2.29 : Spray cooling system for two IGBTs [68].

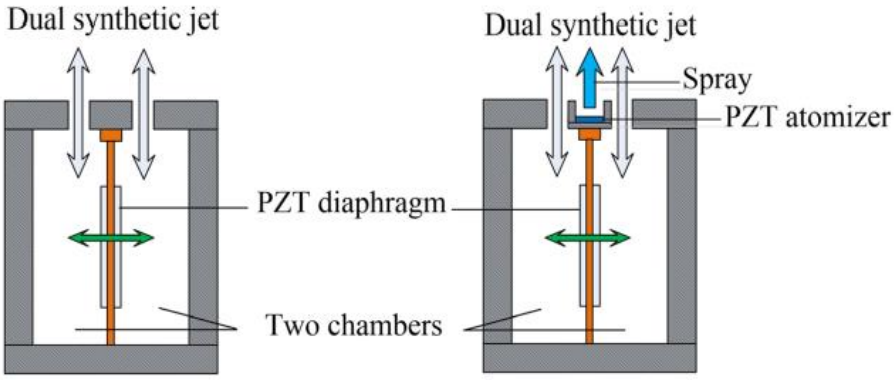

Figure 2.30 : Spray cooling device based on a dual synthetic jet actuator integrated with a piezoelectric atomizer [70].

In [70], a spray cooling device based on a dual synthetic jet actuator integrated with a piezoelectric atomizer (which breaks down the liquid flow into droplets is designed and investigated experimentally (Figure 2.30). It is found that by changing the driving voltage and driving frequency, the spray angle can be adjusted from 20° to 74°, which increases the spray direct impingement area leading to higher thermal performance. The experiments show that

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spray cooling by a synthetic jet actuator has many advantages such as easy controlling, high cooling efficiency and fast response.

Despite the spray cooling advantages and high thermal performance, some disadvantages might affect the choice of using this cooling technique. A high pressure drop is usually required to break droplets up (up to 310 kPa [71]), in addition, spray cooling is a complex technique concerning fluid behavior as well as its dependence on many parameters such as nozzles type, diameter, spacing, coolant density, distance to cooled surface, spray cone angle, and droplets volume.

2.2.3.4 Vapor chamber

Vapor chambers and heat pipes take advantage of the two-phase regime of boiling to maximize heat transfer by evaporating a liquid near the heat source. Vapor champers and heat pipes have the same concept; the vapor transfers the heat by convection to the cold side where condensation takes place. The condensed liquid returns to the evaporator side by capillary forces of the wick structure (Figure 2.31). The two-phase passive circulation of the fluid transfers the heat from evaporator to condenser without having to use external pumps. Heat pipes are used to transport heat from a point to another in the system while vapor champers spread the heat in an uniform manner (3D) which makes it suitable for heat spreading in power electronics. Vapor chambers can dissipate several hundreds of W/cm² power loss density [7] with no power consumption. In addition, its compact size makes it compatible with a PCB stack scale, and hence suitable for PCB embedding technology.

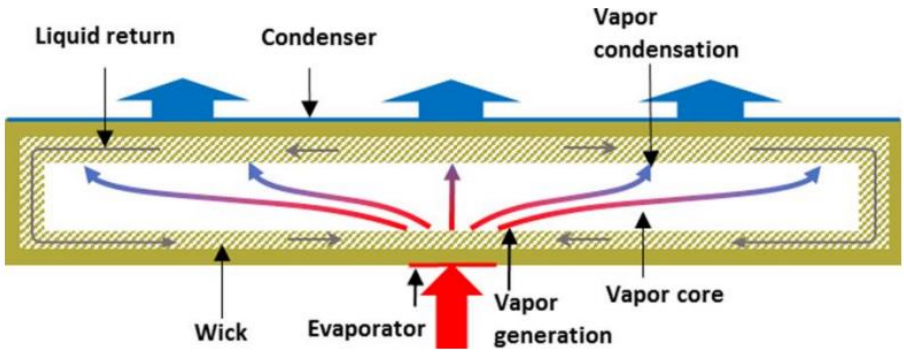

Figure 2.31 : Vapor chamber operation technique [72].

The wick structure is the most important element in vapor chamber [73], since it produces the capillary forces which carry the working fluid from the condenser to the evaporator. As shown in [72], several types of wick structures can be used, such as sintered wick, mesh or grooved wick, and screen wick.

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Many researches and studies are performed to investigate the potential vapor chambers. In [74], a hybrid cooling solution combining two phase micro-channel and a vapor chamber is studied to reduce spreading thermal resistance (Figure 2.32). Furthermore, the integration of a vapor chamber in the DBC (direct bonded copper) substrate of an IGBT power module cooled by water pin-fin heat sink is studied numerically and obtained an improvement in thermal performance with a reduction of 2.5°C in junction temperature as presented in [75].

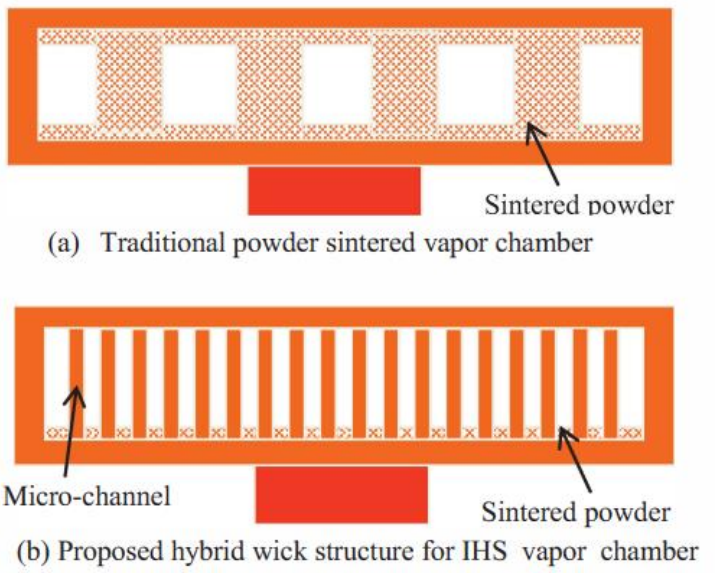

Figure 2.32 : Traditional vapor chamber and hybrid vapor chamber with microchannel [74].

In [76], an integrated heat sink with vapor chamber is developed (Figure 2.33) to improve the thermal management of high-power light-emitting diodes (LEDs). The wick is made of parallel and orthogonal microgrooves using the micro-milling method. Embedding the vapor chamber in the aluminum substrate of a heat sink helps achieving a more uniform distribution, and the junction-to-ambient thermal resistance is reduced by 16.5 % [76].

In [77], a numerical model to study heat transfer in vapor chambers is developed and compared to experiments. It is found that vapor chambers have lower thermal resistance as well as lower weight than copper and the performance is better under gravity-assisted orientation. In addition, imperfections in thermal contact of vapor chamber can lead to a thermal resistance higher than that of solid copper which suggests more optimization in the thermal path, particularly at the interfaces.

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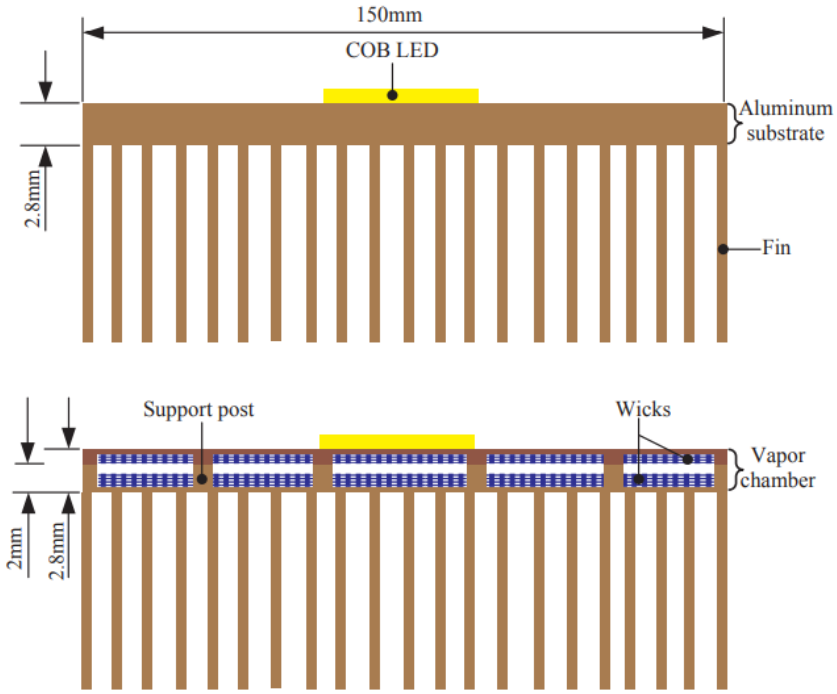

Figure 2.33 : Vapor chamber integrated in the substrate of an aluminum heat sink. [76]

The vapor chamber thickness is being reduced to decrease thermal resistance and have a more compact size, which more suitable for PCB embedding. In [78], the thermal performance of an ultra-thin vapor chamber (1 mm thickness), also called thermal ground plane (TGP), is studied numerically and experimentally as a function of wick and vapor core thicknesses, with water as a working fluid. The effect of boiling in the wick structure on thermal performance is considered. It is found that when the vapor core thickness is in the range of 0.2 – 0.4 mm, the vapor space causes a significant thermal resistance. By varying the wick thickness between 0.05 to 0.25 mm, it is concluded that 0.05 mm is the optimum thickness for low heat flux less than 50 W/cm², while the best performance is obtained at higher heat fluxes (higher than 50 W/cm²) for a thickness of 0.1 mm. It is noted that the vapor chamber performs better as a heat spreader than a solid block only at higher heat fluxes (>100 W/cm²) for the given geometry and surface temperature (in order to reach to the nucleate boiling phase). At these heat fluxes, nucleate boiling occurs in the wick structure, leading to a decrease in its thermal resistance. The wall of their vapor chamber is made of a copper-molybdenum-copper (CuMoCu) layered structure (13 % Cu, 74 % Mo, and 13 % Cu) to provide an acceptable CTE-match (5.6 ppm/K) with semiconductors [78].

The Defense Advanced Research Project Agency (DARPA) has initiated a collaboration between many research groups to examine TGPs [79], with the objective of achieving

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extraordinary lateral thermal conductivities with a thickness of 1 mm or less, in the range of 10–20 kW/(m.K). This is approximately 25–50 times greater than copper and 10 times higher than synthetic diamond (Figure 2.34).

From the DARPA project, it is concluded that:

- CTE matching is critical for direct attachment and TIM removing or reducing its thickness as a stress buffer layer.
- The evaporator (heat source) has the most thermal resistance since the local heat flow levels are highest and the surface area is small.
- Thick wick reduces fluid flow resistance which allows for larger maximum heat flux.
- Thin wick reduces significantly thermal resistance.
- It is important to encourage boiling in the wick by starting the process with as little heat flux as possible.
- The wick should not hold vapor, to prevent dry-out at higher heat fluxes.
- TGP thickness is important because it is the dimension utilized to calculate effective thermal conductivity. A thickness less than or equal to 1 mm is considered thin.

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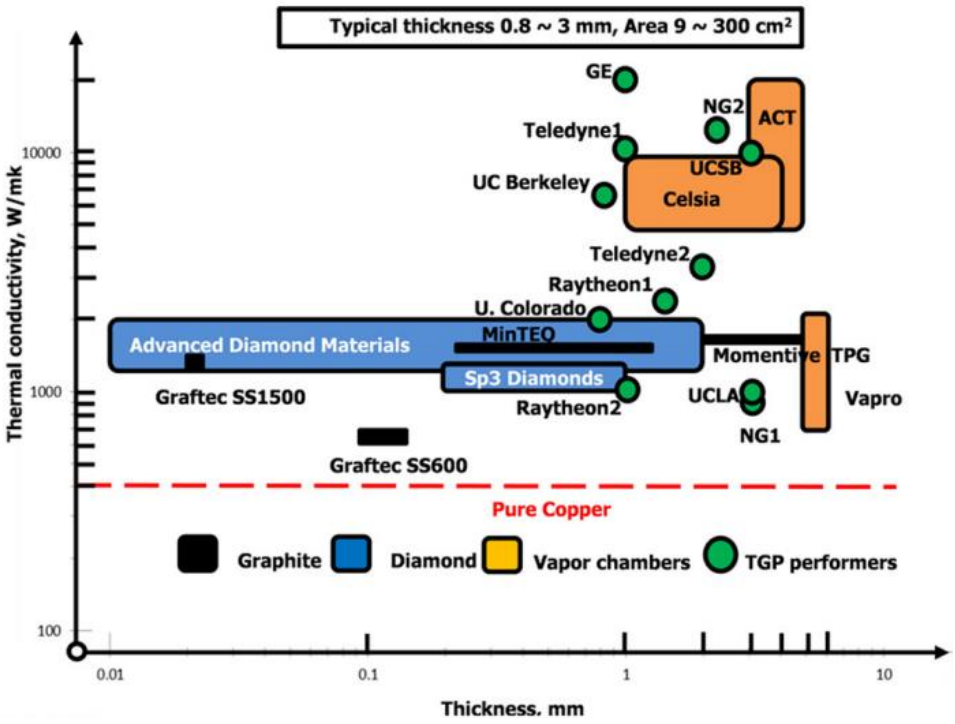

Figure 2.34 : Effective thermal conductivity of phase III TGPs of DARPA's project [79].

In [80], a flexible TGP is designed and fabricated using PCB technology. Mechanical flexibility of TGP can be required in some applications to be integrated in power electronics. The casing is made of copper-clad polyimide sheets, and the wick is made of three layers of thin copper mesh that are electroplated or sintered together and coated with atomic layer deposited TiO2 (Figure 2.35). The vapor transport layer is made of a coarse nylon or polyether ether ketone (PEEK) mesh, with water used as the working fluid. The TGP is heat-sealed with fluoroethylene propylene (FEP), a flexible material that creates a near-hermetic seal for several months. It is found that the measured thermal resistance is reduced by about 50 % compared to an equivalent layer of copper at heat fluxes of 3-6 W/cm². In addition, the flexible TGP showed a bendability reaching 90° while maintaining the good thermal performance and durability.

Despite their thermal performance, vapor chambers have limitations on heat flux applied and temperature to prevent dry-out of working fluid. The capillary limit of the wick structure normally set the maximum heat transfer allowed through vapor chamber [73]. To avoid this capillary limit, a thick evaporator wick structure is needed [81].

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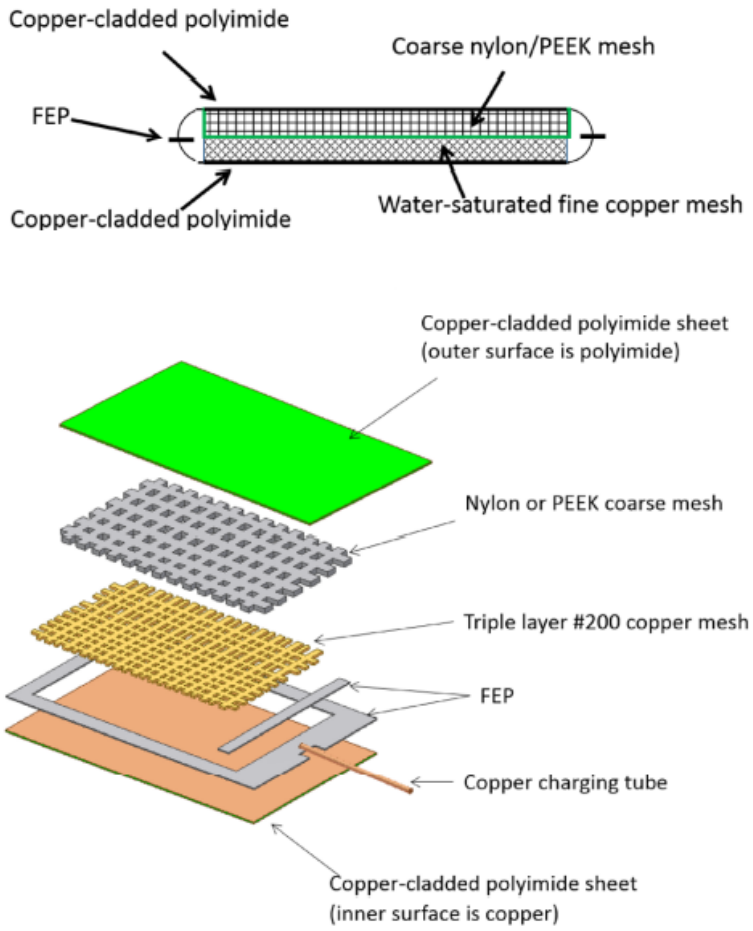

Figure 2.35 : Composition of copper-cladded polyimide flexible TGP [80].

The design of the evaporator wick is important under high heat flux, since boiling causes high fluid flow resistance [82]. Using a thin wick structure reduces thermal resistance but with an increase in fluid flow resistance. Therefore, at high heat fluxes over large areas, the evaporator wick should minimize junction temperature and thermal resistance as well as fluid flow resistance during boiling [37].

The two-layer evaporator wick [83] separates liquid and vapor paths to reduce fluid flow thermal resistance as well as the thermal resistance of the wick structure. This hybrid structure is composed of a thin wick layer for boiling and a thick wick layer on top of it (Figure 2.36). The thin wick is fed vertically by the liquid from the thick wick while vapor extraction is easier through the thick wick layer during boiling. The two-layer evaporator wick structure allow high heat flux dissipation (~485 W/cm²) at a low thermal resistance (0.052 K/W) [84].

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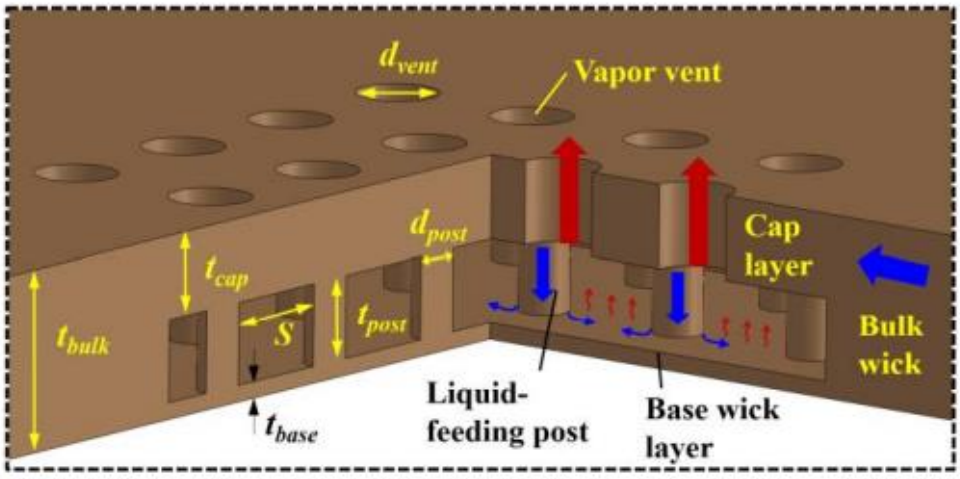

Figure 2.36 : Two wick structure concept [83].

In [37], the thermal performance of a vapor chamber with a two-layer evaporator wick is investigated (Figure 2.37). A 50×50×5.5 mm^3 vapor chamber with pin-fin heat sink cooled by air jet impingement is evaluated for a 1 cm2 area heat source. At a power loss of about 500 W, the air-cooled two-layer wick vapor chamber shows a 12 % reduction in thermal resistance compared to traditional monolayer wick. However, the two-layer wick vapor chamber shows a maximum dry-out heat flux of 451 W/cm² while the monolayer extends that value to reach 513 W/cm². It is concluded that more work is needed for the two-layer wick design to obtain higher maximum dry-out heat flux while keeping thermal resistance at low levels.

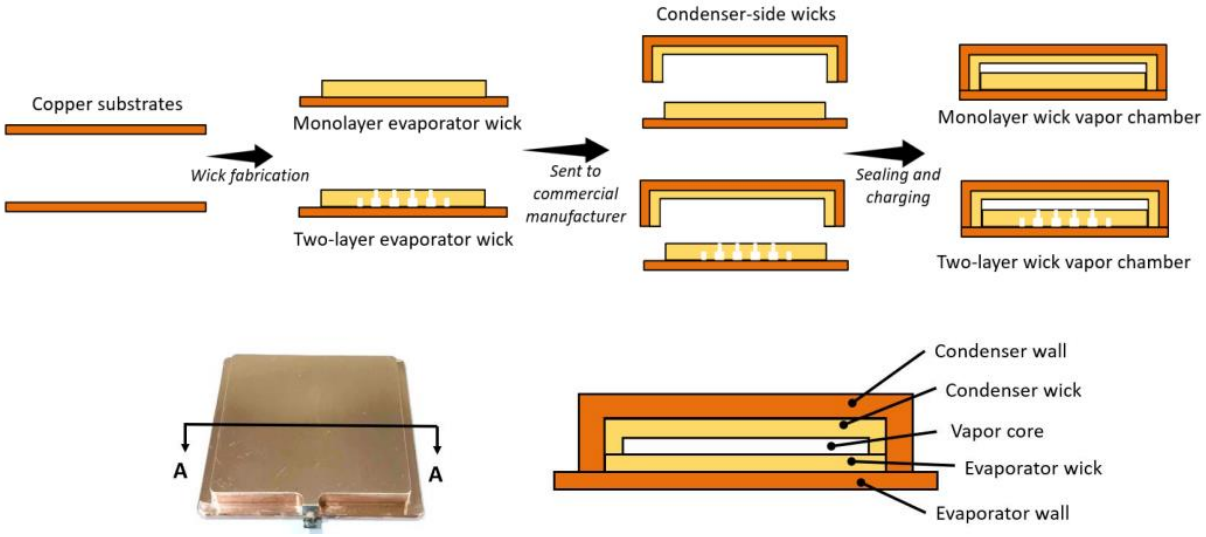

Figure 2.37 : Two wick vapor chamber fabrication process [37].

To achieve more reduction in thermal resistance using a vapor chamber, it is found that the thermal resistance of a commercial vapor chamber can be significantly reduced by embedding

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an intermediate heat spreader between the heat source and the vapor chamber as presented in [81]. The thermal resistance of a vapor chamber is reduced by embedding an intermediate vapor chamber, with multiple small vapor cores and thin wicks, between the heat source and the main vapor chamber (Figure 2.38).

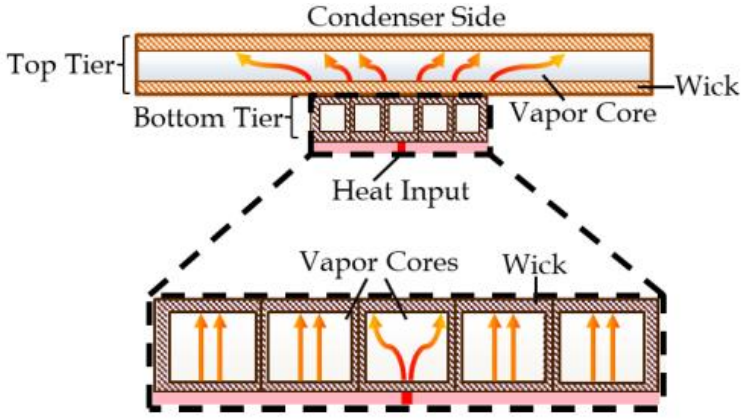

Figure 2.38 : Cascaded Multicore Vapor Chambers [81].

The intermediate vapor chamber spreads the heat from small hotspots, resulting in a low hotspot thermal resistance. The proposed architecture can damp the hot spots before reaching the main vapor chamber with larger core and thicker wicks to handle high heat flux. For a total heat load of 476 W having a background heat flux of 75 W/cm², with hotspots of 800 W/cm² over a 1 mm² area, the proposed vapor chamber architecture shows a thermal resistance of 0.66 K/W compared to 1.76 K/W with a conventional, single-stage vapor chamber. The significant reduction is owed to the reduction in the conduction thermal resistances across the internal wicks [81].

2.2.4 Cooling enhancement

In addition to the reviewed heat extraction techniques, some more enhancement can be implemented in order to improve cooling capability, such as: the shape of the heat sink fins, double-side cooling, direct liquid cooling, and heat transfer control by using metamaterials.

2.2.4.1 Fins shape

As stated previously, increasing the surface of the heat exchange surface will increase the convection heat transfer capability. However, this can increase the pressure drop (and therefore, the pumping power) needed to drive the coolant through the fins of the heat sink. Finding the optimum shape of the fins can help maximizing the thermal performance while reducing pumping power requirements, hence the cost.

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In [85], the effect of microchannel shape on the thermal performance is analytically studied and compared to that of a copper heat sink with micro-pin-fins (Figure 2.39). It is found that at water mass flow rates lower than 60 g/min, the convection thermal resistance of the micro-pin-fin heat sink is higher than that of the microchannel heat sink (lower convection heat transfer). However, at a mass flow rate higher than 60 g/min, the micro-pin-fin shows lower convection thermal resistance (higher convection heat transfer). In terms of pressure drops, the micro-pin-fin heat sink shows higher pressure drops over the whole range of water mass flow rate [85].

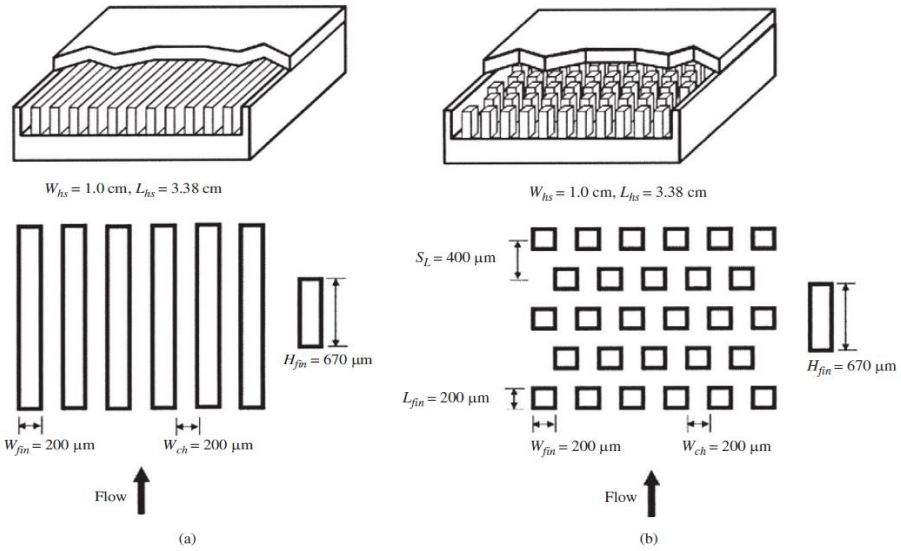

Figure 2.39: Microchannel heat sink compared to micro-pin-fin heat sink [85].

In [86], the thermal performance and the hydraulic performance of a twisted offset strip fin (square fins) heat sink cooled by water is numerically investigated at a power loss density of 100 W/cm². The twisting angle is varied from 10° to 120° (Figure 2.40). It is found that the thermal performance of twisted fins is improved compared to the baseline fins (untwisted fins). However, this improvement came at the cost of reduced hydraulic performance. At twisting angle of 120°, the total thermal resistance is reduced by 14.75 %. However, the pressure drop is increased by 39 % compared to the baseline fins [86].

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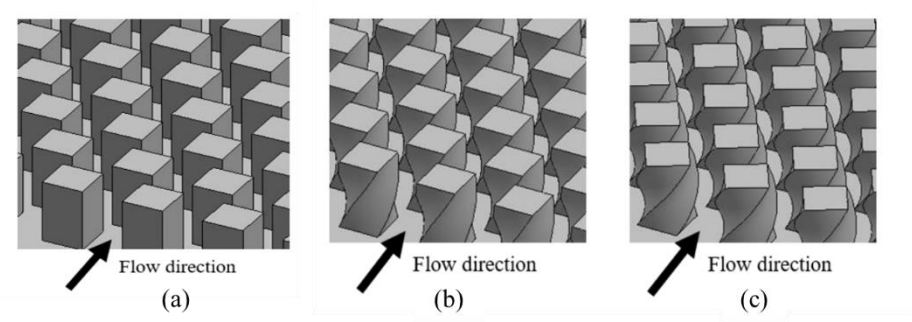

Figure 2.40: Offset strip fins (a) untwisted, (b) twisted 90° (c) twisted 120° [86].

The pin-fins can take various shapes: circular, rounded rectangle, airfoil (also called "water drop" if the airfoil is symmetric), hexagonal, and so on. Channel-fins can also take various shapes: rectangular, airfoil, arc, zig-zag, etc. In [87], the convective heat transfer performance of airfoil heat sinks fabricated by selective laser melting is studied experimentally and compared to circular and rounded rectangular heat sinks. As shown in Figure 2.41, the heat sink is 50×50 mm² with fins height of 25 mm. the heat sink is cooled by air at constant pumping power of 10 W. Two airfoil shapes are studied: NACA0024 (symmetric) and NACA4424 (cambered). The thermal performance of both airfoil heat sinks are comparable and show 29 % increase compared to circular pin-fin heat sink. The rounded rectangular heat sink outperforms the airfoil heat sinks at Reynold's numbers higher than 10,000. The thermal performance of the airfoil heat sinks is increased by increasing the angle of attack (Figure 2.42) which create vortices that enhances fluid mixing which improves heat transfer [87]. These findings agree with results of [88], where it is found that rounded rectangular pin-fins heat sink performs better thermally compared to the airfoil pin-fin heat sink by using water as a coolant. However, airfoil pin-fins decrease the pressure drop. Increasing the angle of attack enhances the thermal performance, with the penalty of a higher pressure drop than zero angle of attack airfoil.

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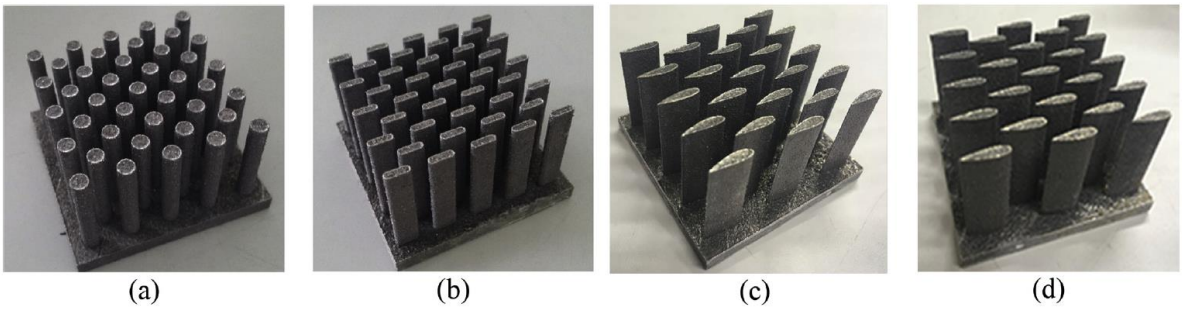

Figure 2.41: (a) circular fins (b) rounded rectangular fins (c) NACA4424 fins (d) NACA0024 fins.

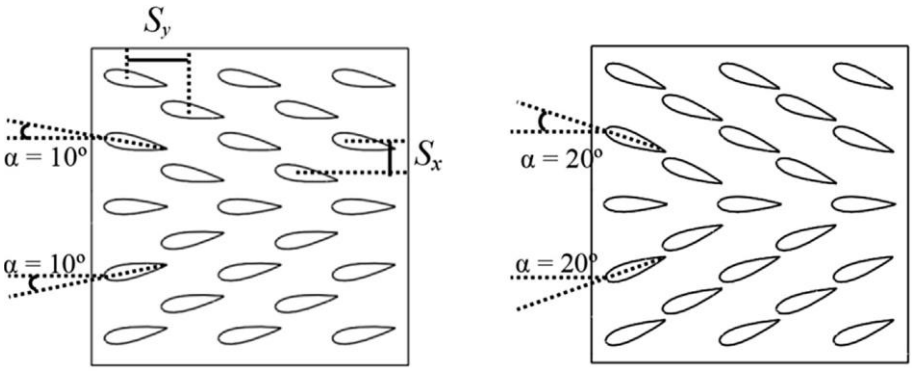

Figure 2.42: Variable angle of attack of NACA airfoils.

Several other shapes of heat sink fins are studied in order to reach an optimum high thermal performance and low pressure drop such as in [89] and [90]. The objective here is to show that the shape of the heat sink fins can affect the cooling performance.

2.2.4.2 Double-side cooling

Double-side cooling of a PCB can highly improve heat transfer and reduce thermal resistance since heat will be dissipated through two paths, i.e. on the top and bottom sides of the flat board.

In [91], 45 % to 60 % reduction in thermal resistance is obtained (depending on the volumetric flow rate) when mounting water cold plate cooling on both sides of a silicon chip with a power loss density of 150 W/cm² (Figure 2.43). Another study [92] shows that with water double-side cooling, thermal resistance is reduced by 20 % compared to single-side cooling for 550 W/cm² SiC chips.

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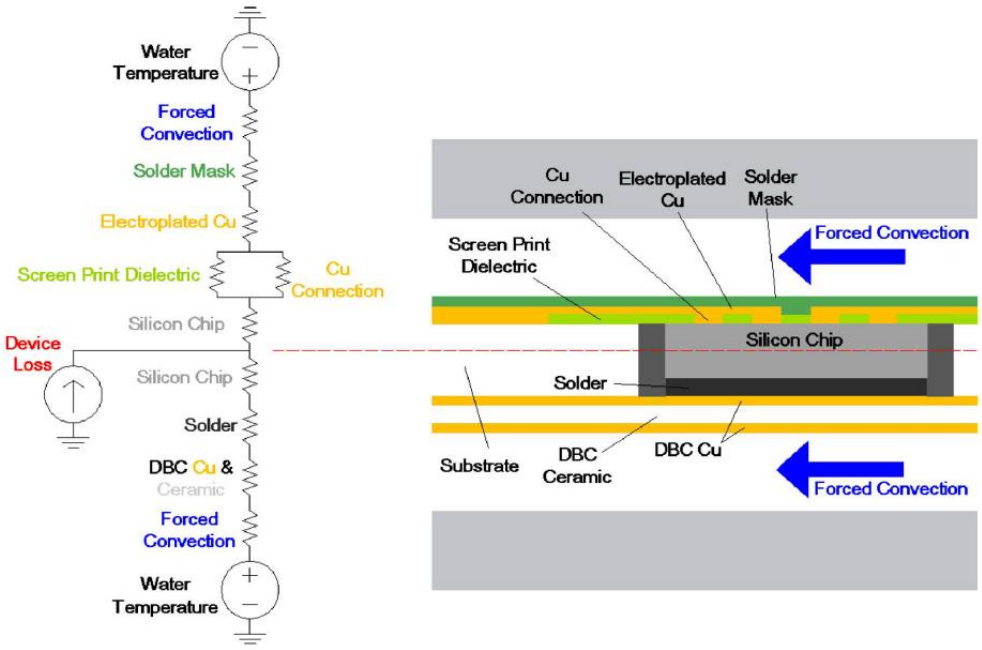

Figure 2.43 : Double-sided cooling of a DBC of a power module [91].

Although double-side cooling provides better cooling, connections on top of the chip are more complex, because several electrical potentials must be connected on top of the chip. Also, at least one side of the PCB is used to mount components and connectors, making the attachment of a heatsink there more difficult.

2.3 Conclusion

2.3.1 Heat spreading

In order to facilitate heat extraction, heat needs to be spread efficiently to a large heat exchange surface area where heat is exchanged with the cooling system. Spreading the heat from an electronic component which dissipates a considerable power loss density, through the PCB layers requires high thermal conductivity as well as suitable CTE values (compatible with PCB materials and semiconductors). The objective is to identify a heat spreader with high thermal conductivity, suitable CTE, compatible with PCB embedding process, compact size, and having low cost.

Diamond is an excellent heat spreader in terms of its high thermal conductivity (2000 W/(m.K)) and low CTE that is matched with semiconductor materials. However, the high cost of diamond makes it unsuitable to power electronics applications attached to commercial products.

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On the other hand, Graphite has a high thermal conductivity that can reach 2000 W/(m.K). However, it is an anisotropic material. The high thermal conductivity is in (X-Y) plane while thermal conductivity in Z-direction is poor (few Watts/(m.K)). The same anisotropic behavior can be seen with the CTE values.

Many reviewed studies considered embedding graphite layers to enhance heat spreading and temperature uniformity, while others worked on stacking graphite layers in an arrangement so that the high thermal conductivity is in the Z-direction where heat is transferring to the cooling side of the substrate. Stacking graphite layers that way would require manufacturing the stack and encapsulating it in a separate process, then embedding the stack as a layer during PCB lamination process. In addition, such an arrangement offers poor thermal conductivity in one of the horizontal directions which limits heat spreading capability and uniformity.

Vapor chamber works as two-phase heat spreader using a working fluid which is an interesting heat spreading cooling technique. Implementations have been proposed using PCB-like technology (TGP). However, the limitations on the applied heat flux (to avoid dry-out) and conduction mode put constraints on using vapor chambers. Also wick structure is a critical element that affect thermal resistance as well as flow resistance, which require more research. Vapor chambers heat spreaders are not investigated in this thesis work.

More work is needed to take advantage of graphite high horizontal thermal conductivity to spread the heat while reducing its thermal resistance in the vertical direction. Furthermore, embedding graphite layers seems to be compatible with PCB manufacturing process since graphite are available in the form of sheets. Therefore, graphite is selected for heat spreading and its integration in a PCB will be studied further.

2.3.2 Heat extraction

A good heat spreader transfers large amounts of heat efficiently from the electronic components to the cooling side in order to keep their temperatures at acceptable levels. After that, the objective is to extract as much heat as possible from the larger surface at the smallest temperature difference with the environment (ambient). The heat is transferred by convection via a coolant fluid to be evacuated to the ambient. To improve heat extraction, the cooling surface area should be larger to exchange more heat with the coolant flow. In addition, we can enhance the heat transfer coefficient by choosing a cooling fluid with high heat capacity, increasing coolant flow velocity, and considering two-phase cooling to take advantage of latent heat transfer. Furthermore, by getting closer to the heat source (direct cooling or near-junction

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cooling), the temperature difference between junction and coolant inlet or ambient will be higher, giving a chance for more heat extraction.

However, increasing the heat extraction capacity of a cooling system can require more power consumption and cost. By providing larger heat exchange area, size and weight will be increased, which can be limiting factors for some applications. Increasing heat transfer coefficients by increasing velocity and flow rate of the coolant will require larger pumps and additional cost. Choosing a coolant with high heat transfer capacity can increase the overall thermal performance but it can be dynamically viscous which causes more pressure drop. Considering two-phase cooling can increase heat flux removal rates but will add to the complexity of the cooling system.

Many studies have been reviewed to identify an efficient cooling solution suitable with PCB embedding technology. Natural and forced air cooling are conventional techniques for power electronics cooling, but their heat transfer capacity is low which make them not suitable for high power loss density applications. Liquid and two-phase cooling techniques showed higher heat transfer rates. The tables and Figure 2.44 below show the thermal performance of reviewed studies of microchannel, liquid jet impingement, and spray cooling. The values in tables are calculated based on the given articles' data. In order to evaluate cooling performance and to quantify heat transfer capacity, a figure of merit that contains much information about cooling system should be used.

- Chip area $A_{chip}\ cm^2$
- Chip power loss Q (W)
- Chip Power loss density:

$$q = \left(\frac{Q}{A_{chip}}\right)\ W/cm^2$$

- Temperature difference between chip junction temperature and reference temperature (ambient, fluid coolant inlet,..etc):

$$\Delta T = \left(T_j - T_r\right)$$

- thermal resistance is defined as follows:

$$R_{th} = \left(\frac{\Delta T}{Q}\right)\ K/W$$

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- Normalized thermal resistance is defined as follows in order to give information about the heat source size:

$$R_{th}^{*} = \left(\frac{\Delta T}{q} \times 100\right) K.mm^2/W$$

- The effective heat transfer coefficient (HTC) from the junction to the reference temperature is defined as follows:

$$HTC_{eff} = \left(\frac{Q}{\Delta T \times A_{chip}}\right) W/(m^2.K)$$

- Fluid volumetric flow rate V (L/min)
- Pressure drop required to circulate certain flow rate $\Delta P\ (kPa)$.
- Pumping Power is defined as:

$$W_p = \frac{\left(V\ (L/min) \times \Delta P(kPa)\right)}{60}\ W$$

- Normalized pumping Power is defined as follows in order to consider the size of the heat source:

$$W_p^{*} = \frac{\left(V\ (L/min) \times \Delta P(kPa)\right)}{60 \times A_{chip}}\ W/mm^2$$

Table 2.1: Reviewed studies of microchannel cooling technique.

Ref.	Coolant	Heat source	q (W/cm²)	Q (W)	T_j (°C)	T_i (°C)	ΔP (kPa)	V (L/min)	W_p^* (W)	HTC_{eff} (kW/m²K)	R_{th}^* (K.cm²/W)
[58]	Water	SiC Chip	250	1000	200	72	10.0	0.21	8.75E-05	78.1	12.8
[42]	Water	SiC MOSFET	127	127	70	50	40.2	0.1	7.00E-04	63.7	15.7
[41]	Water	Surface	700	2800	85	20	22.0	1.3	1.20E-03	107.5	9.3
[40]	Water	IGBTs & diodes	604	1320	120	20	133.0	3	3.07E-02	60.2	16.6
[39]	Water	Chips	417	1250	92	24.5	40.0	1.25	2.94E-03	61.7	16.2
[98]	Nano-fluid	LED	8	50	48	25	7.2	35	6.72E-03	3.48	287
[57]	Two-phase R236fa	Surface	255	2450	52	10	90	0.49	7.70E-04	60.6	16.5
[59]	Two-phase R1234yf	SiC MOSFET	526	33	120	25	350			55.6	18
[58]	Two-phase R245fa	SiC Chip	1000	250	163	90	6.9	0.21	9.60E-04	137	7.3

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Table 2.2: Reviewed studies of liquid jet impingement cooling technique.

Ref.	Coolant	Heat source	q (W/cm²)	Q (W)	T_j (°C)	T_i (°C)	ΔP (kPa)	V (L/min)	W_p^* (W)	HTC_{eff} (kW/m²K)	R_{th}^* (K.cm²/W)
[42]	Water	SiC MOSFET	1020	255	134	50	81.2	0.45	2.44E-02	122	0.082
[49]	Water	Chip	700	2800	88	22.5	4.9	1	2.05E-04	106.4	0.094
[47]	50/50 WEG	4 Diodes	275	132	92	70	17.5	10	6.08E-02	125	0.08
[54]	Water	Chip	175	953	75	10	15	3	1.38E-03	27	0.371
[51]	De-water	Chip	160	800	78.7	40	19.8	2	1.32E-03	41.3	0.242
[53]	Water	Chip	156	100	35	10	40	0.6	6.24E-03	62.5	0.16
[50]	Water	MOSFET direct	127.5	51	140	22.5	6	0.03	7.50E-05	10.8	0.922
[50]	Water	MOSFET TIM	127.5	51	210	22.5	6	0.03	7.50E-05	6.8	1.47
[52]	Water	IGBT & Diode	250	250	117	27	26.3	0.57	2.50E-03	27.8	0.36

Table 2.3: Reviewed studies of spray cooling technique

Ref.	Coolant	Heat source	q (W/cm²)	Q (W)	T_j (°C)	T_i (°C)	ΔP (kPa)	V (L/min)	W_p^* (W)	HTC_{eff} (kW/m²K)	R_{th}^* (K.cm²/W)
[65]	HFE-7100	Surface	255	255	109.6	43	177	0.631	1.86E-02	38.3	0.26
[66]	50/50 WPG	12 IGBT	165	1600	127	100	275.8	3.4	1.61E-02	61.3	0.163
[67]	Water	12 IGBT	160	1545	117	95	172.4	2.83	3.37E-02	72.7	0.138
[68]	Coolant B90°	IGBTs	400	800	133	90	145	0.3	3.63E-03	92.6	0.108
[69]	R134a	Surface	138	230	37.3	20.3	105.0	0.3	3.18E-03	81.3	0.123

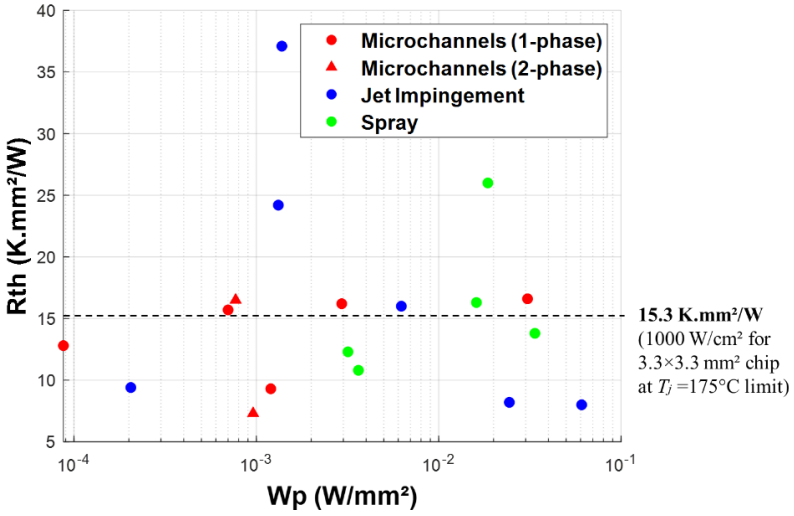

Figure 2.44: The thermal performance of the reviewed studies of liquid cooling.

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From Figure 2.44, microchannel, jet impingement, and spray cooling techniques can reach a thermal resistance that is corresponding to 1000 W/cm² power loss density for 3.3×3.3 mm² chip at 175°C junction temperature limit. However, the studies of microchannel and jet impingement cooling techniques are showing the least thermal resistance with comparable performance. Regarding the pumping power, the studies of jet impingement within the targeted heat dissipation capability are showing higher values of pumping power compared to those of microchannel cooling technique.

In conclusion, Liquid jet impingement combined with efficient enlargement of the heat exchange surface, such as pin-fins, is chosen for heat extraction increases, since it provides more uniform surface temperature (the coolant flow hits the surface perpendicularly the distributes radially in a uniform manner) compared to microchannel technique (with the coolant flowing parallel to the surface).

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3 Methods and tools

This chapter gives a brief idea about the physics encountered in this thesis as well as the tools used to quantify the heat transfer and predict the thermal performance of the proposed thermal management solutions. It starts by describing the governing equations of the heat transfer and fluid dynamics. After that the different approaches to model heat transfer are described and compared in order to choose a preliminary design tool. Then, the tool for numerical simulations is presented and finally, the thermal measurements methods are described as well as the experimental setup.

3.1 Physics governing equations

The heat transfer and fluid dynamics equations are detailed in this section. These equations are the foundation of the analytical models and the numerical simulations tools which are used throughout this thesis.

3.1.1 Heat transfer governing equations

Having a temperature difference between two mediums results naturally in a heat transfer occurring between them, in order to reach an equilibrium state of the thermal energy. The rate of heat transfer per unit area (heat flux) is a vector quantity that has directions and magnitude. It is generally three-dimensional and time-dependent, since the temperature of the mediums varies depending on time and position [99]. The heat transfer can take place according to three mechanisms: conduction, convection, and thermal radiation. This section presents an overview of each heat transfer mode and their governing equations.

3.1.1.1 Conduction

In conduction heat transfer mechanism, thermal energy is transported between the particles of the substance through the interaction between more energetic particles (higher temperature) and less energetic particles (lower temperature). In solids, this interaction takes the form of a combination of molecules vibrations in a lattice and the energy transfer by free electrons. In liquids and gases, the interaction occurs by the collisions and diffusion resulting from the random motion of the molecules [99].

Fourier’s law describes the relation between the conductive heat flux and the temperature gradient field. In the three Cartesian directions and for an isotropic materials, the equation is written as in (3.1)

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$$q = -k\,\nabla T = -k\,(\,\mathrm{i}\frac{\partial T}{\partial x} + \,\mathrm{j}\frac{\partial T}{\partial y} + \,\mathrm{k}\frac{\partial T}{\partial z}\,) \tag{3.1}$$

where the heat flux vector q is the heat transfer rate per unit area (W/m²); the vector q points in the direction opposite to temperature gradient ∇T in each direction [100]; k is the thermal conductivity of the medium material [99].

Thermal conductivity is a material property that can be either isotropic, when it is identical in all directions ($k_x = k_y = k_z$) or orthotropic when the thermal conductivity value differs with respect to the three perpendicular directions. In the isotropic case, k is a scalar quantity, whereas it becomes a tensor in the orthotropic case. Equations (3.2) show the heat Q of the conductive heat transfer in the three main cartesian directions after simplifying equation (3.1)

$$Q_x = k_x\,A_x\,\frac{\Delta T}{\Delta x} \qquad Q_y = k_y\,A_y\,\frac{\Delta T}{\Delta y} \qquad Q_z = k_z\,A_z\,\frac{\Delta T}{\Delta z} \tag{3.2}$$

where A_x, A_y, and A_z are the cross-sectional areas to which heat fluxes are normal and ΔT is the temperature difference through a thickness of the medium in a specific direction (Δx, Δy, and Δz).

Another important material property is the specific heat capacity of the medium (C_p), which is the ability of the material to store thermal energy per unit mass (J/(kg.K)). Multiplying C_p by the material density (ρ), yields the volumetric heat capacity ($\rho\,C_p$) which measures the stored thermal energy per unit volume (J/(m^3.K)) [99].

The ratio between the thermal conductivity and the heat capacity measures the speed at which heat diffuses through a medium. This ratio is called the thermal diffusivity (α) and it is another material property. Equation (3.3) defines the relation between thermal diffusivity (m²/s), thermal conductivity, and heat capacity [99].

$$\alpha = \frac{k}{\rho\,C_p} \tag{3.3}$$

3.1.1.2 Convection

Convection heat transfer mechanism occurs between a hot solid surface and a moving fluid. The fluid motion can be caused by buoyancy force, which results from the density difference due to the variation in the fluid temperature (natural convection) or be forced by external means (forced convection). Fluid motion enhances the convection heat transfer, hence the faster the fluid is moving, the higher the heat exchange rate between the hot surface and the moving fluid.

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Convection also involves effects of the conduction mechanism due to the diffusion of the heat in the fluid. If the fluid does not move (e.g. due to insufficient buoyancy force), then the heat transfer only relies on pure conduction between the hot solid surface and the adjacent fluid [99].

The rate of convection heat transfer is can be expressed by Newton's law of cooling as in equation (3.4) where T_s is the hot solid surface temperature, A_s is the area of the solid surface, and T_∞ is the temperature of the fluid far enough from the solid surface (the "ambient" temperature) [99].

$$Q = h\, A_s\, (T_s - T_\infty) \tag{3.4}$$

Where h is the convection heat transfer coefficient in W/(m².K) which is not an intrinsic property of the fluid. It is a parameter that is affected by several variables such as surface geometry, fluid velocity, properties of the fluid (density, viscosity, thermal conductivity, specific heat,…etc). The larger the value of h, the greater the amount of heat dissipated by convection.

. When Newton's law is used it is not necessary to solve the governing equations in the fluid, only the energy conservation in the solid needs to be solved and equation (3.4) is used as a boundary condition on solid-fluid interfaces. The main difficulty resides in the accurate determination of *h*, also since in many cases the heat transfer coefficient is non-uniform and/or a function of time. A different more time-consuming approach consists in solving the governing equations in both the solid and the fluid.

3.1.1.3 Thermal radiation

Thermal radiation is the transfer of thermal energy by means of electromagnetic waves. Unlike the other mechanisms of heat transfer, thermal radiation does not require a medium; it can transfer heat though vacuum [97].

In the simple case of radiative heat transfer between a material surface A_s at temperature T_s exposed to an environment at temperature T_∞, the net rate of heat transfer by thermal radiation can be estimated by following equation:

$$Q = \sigma\, \varepsilon_s\, A_s\, (T_s^4 - T_\infty^4) \tag{3.5}$$

where σ is the Stefan-Boltzmann constant (σ =5.669×10^{-8} W/(m² ·K^4)), and ε_s is the emissivity of the surface (which depends on the material, surface roughness,…etc). The value of ε_s is in the range of $0 \leq \varepsilon_s \leq 1$. Reaching the maximum emissivity ($\varepsilon_s = 1$) is a characteristic of a

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blackbody [100]. For example, polished copper has an emissivity of about 0.03 [99], whereas for oxidized or rough copper surfaces the value is easily 0.5 or higher.

In forced convection applications such as power electronics cooling, thermal radiation can be considered negligible compared to the other forms of heat transfer [99] (for example: 0.000566 W/cm² for a blackbody with a surface temperature of 100°C at an ambient temperature of 22°C). In this work, radiation will not be considered.

3.1.2 Fluid dynamics

Fluid motion affects the rate of convective heat transfer depending on the fluid properties and motion characteristics. The heat and mass transfer in fluids are governed by three conservation laws: conservation of mass, conservation of momentum, and conservation of energy [100]. In this section, the governing equations of each law are presented assuming that the fluid is Newtonian, with constant viscosity and constant density (i.e. the flow is incompressible).

3.1.2.1 Conservation of mass

The fluid mass is conserved while transferring through a control volume. The net rate of fluid mass entering the control volume equals the net rate of the fluid mass exiting the control volume [100]. This conservation principle is described (in Cartesian coordinates) by equation (3.6), which is called the continuity equation.

$$\frac{\partial(\rho)}{\partial t}+\frac{\partial(\rho u)}{\partial x}+\frac{\partial(\rho v)}{\partial y}+\frac{\partial(\rho w)}{\partial z}=0 \tag{3.6}$$

where u, v, and w are the velocity vector components in Cartesian coordinates. For incompressible flow (constant density), this equation is simplified to (3.7):

$$\frac{\partial u}{\partial x}+\frac{\partial v}{\partial y}+\frac{\partial w}{\partial z}=0 \tag{3.7}$$

3.1.2.2 Conservation of momentum

Conservation of momentum is also called Newton's second law of motion and states that all forces acting on the control volume must be equal to the net rate of the momentum entering and leaving the control volume [100]. Equations (3.8), (3.9), and (3.10) describe the conservation of momentum in the three Cartesian directions for a flow of a viscous incompressible fluid.

$$\rho\left(\frac{\partial u}{\partial t}+u\frac{\partial u}{\partial x}+v\frac{\partial u}{\partial y}+w\frac{\partial u}{\partial z}\right)=-\frac{\partial P}{\partial x}+\mu\left(\frac{\partial^2 u}{\partial x^2}+\frac{\partial^2 u}{\partial y^2}+\frac{\partial^2 u}{\partial z^2}\right)+\rho g_x \tag{3.8}$$

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$$\rho\left(\frac{\partial v}{\partial t}+u\frac{\partial v}{\partial x}+v\frac{\partial v}{\partial y}+w\frac{\partial v}{\partial z}\right)=-\frac{\partial P}{\partial y}+\mu\left(\frac{\partial^2 v}{\partial x^2}+\frac{\partial^2 v}{\partial y^2}+\frac{\partial^2 v}{\partial z^2}\right)+\rho g_y \tag{3.9}$$

$$\rho\left(\frac{\partial w}{\partial t}+u\frac{\partial w}{\partial x}+v\frac{\partial w}{\partial y}+w\frac{\partial w}{\partial z}\right)=-\frac{\partial P}{\partial z}+\mu\left(\frac{\partial^2 w}{\partial x^2}+\frac{\partial^2 w}{\partial y^2}+\frac{\partial^2 w}{\partial z^2}\right)+\rho g_z \tag{3.10}$$

Where P is the pressure while μ is the fluid dynamic viscosity. The last term on the right-hand side represents the gravitational force where g is the constant of gravity. These equations together with the continuity equation (conservation of mass) are also called the Navier-Stokes equations.

3.1.2.3 Conservation of energy

The rate of change of the energy stored in a control volume equals the difference between the rate of energy entering and exiting the control volume [100]. When expressed in terms of thermal energy, this balance of energy is described in differential form by equation (3.11)

$$\rho C_p\left(\frac{\partial T}{\partial t}+u\frac{\partial T}{\partial x}+v\frac{\partial T}{\partial y}+w\frac{\partial T}{\partial z}\right) = \frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(k\frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(k\frac{\partial T}{\partial z}\right)+\mu\emptyset+q \tag{3.11}$$

where μ is the fluid viscosity and $\mu\emptyset$ is the viscous dissipation term which is expressed by equation (3.12), and q represents a volumetric heat source term (Joule effect, chemical reactions, etc.). Viscous dissipation is negligible in most heat transfer problems, except for extremely viscous fluids which are however of no interest for electronic cooling.

$$\mu\emptyset=\mu\left(\left(\frac{\partial u}{\partial y}+\frac{\partial v}{\partial x}\right)^2+\left(\frac{\partial u}{\partial z}+\frac{\partial w}{\partial x}\right)^2+\left(\frac{\partial v}{\partial z}+\frac{\partial w}{\partial y}\right)^2+2\left(\left(\frac{\partial u}{\partial x}\right)^2+\left(\frac{\partial v}{\partial y}\right)^2+\left(\frac{\partial w}{\partial z}\right)^2\right)\right) \tag{3.12}$$

3.1.3 Conjugate heat transfer (CHT)

Conjugate heat transfer involves both solid and fluid domains, which exchange heat at their connecting interfaces. In the solid domain, since the velocity is zero, the conservation of energy equation (3.11) is reduced to:

$$\rho C_p\frac{\partial T}{\partial t}=\frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(k\frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(k\frac{\partial T}{\partial z}\right)+q \tag{3.13}$$

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At the solid-fluid interface, the heat flux is conserved $q_s = q_f$ and for perfect thermal contact interfaces the temperatures of the solid and fluid interface are equal ($T_s = T_f$). In practice, a small temperature difference exists which is roughly proportional to the heat flux. This can be expressed using a contact thermal resistance. In this thesis, we consider only perfect thermal contact.

In the fluid domain the conservation of energy equation (3.11) and Navier-Stokes equations (equations (3.8), (3.8), (3.9), and (3.10)) are solved in order to obtain velocity, pressure and temperature fields in the fluid.

3.2 Heat transfer modeling approaches

The following sections present several heat transfer modelling approaches, from simple analytical models to computationally-intensive numerical models. Their respective advantages and limitations are discussed. An application case (a "heat spreader") is chosen to compare the modelling approaches. This application case is discussed in greater details in chapter 4. It aims at spreading the heat dissipated by a small power source (a semiconductor chip) over a larger surface thanks to heat conduction, so that the larger surface can be cooled more easily by a fluid (convection).

According to [101], there are five approaches to quantify heat spreading and calculate the corresponding thermal resistance: 1-D series-resistance networks, the "L" approximate equation [102], the "SLA" approximate equations, analytical solutions, and FEM numerical solutions.

3.2.1 1-D series-resistance network

The 1-D series-resistance network is the simplest method to estimate conduction heat transfer. The underlying assumption is a uniform heat transfer in one direction between two surfaces with uniform surface temperature.

Equation (3.14) defines in this case the total thermal resistance R_{thJA} (conduction + convection) of a layer as a function of its thickness *t*, area *A*, and its thermal conductivity *k* as well as the heat transfer coefficient *h* at the layer boundary with the surrounding fluid:

$$R_{thJA} = \frac{t}{k\,A} + \frac{1}{h\,A} \tag{3.14}$$

This approach clearly does not take into account heat spreading and therefore cannot be used in this work, but it can serve as a reference value to compare the actual performance of a heat spreader thermal resistance.

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3.2.2 "L" approximate equation

The "L" approximate equation [102] is suited to the case of a uniform single heat source on a square plate with uniform heat transfer coefficients at the bottom side as shown in Figure 3.1.

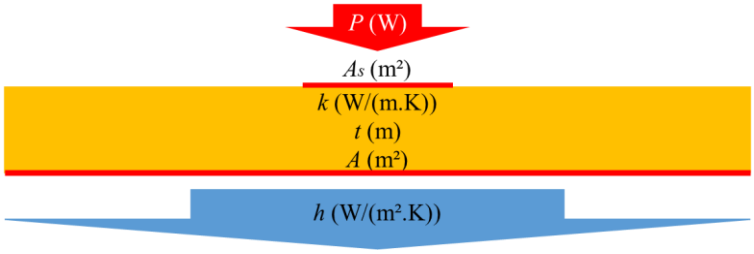

Figure 3.1: Uniform heat transfer model through a square plate.

It is assumed that the square plate of this model is approximated into a flat cylinder. Therefore, equation (3.15) describes a one-sided heat transfer by approximating the Bessel function solution for a cylinder by algebraic equations.

$$R_{thJA} = \frac{\ln\frac{A}{A_s}}{4\,\pi\,k\,t} - \frac{\gamma}{2\,\pi\,k\,t} + \frac{1}{h\,A} \tag{3.15}$$

Where γ is Euler's constant and equals 0.577. The middle term of the right-hand side can be interpreted as a correction term.

Certain geometrical and heat transfer conditions have to be met for this equation to work with high accuracy (better than 90 %). According to [101], the following conditions should be met to guarantee high accuracy:

$$\frac{A}{A_s} > 4 \qquad m \times a < 0.5 \qquad m \times b < 3 \qquad m \times t < 0.15 \tag{3.16}$$

Where,

$$m = \sqrt{\frac{h}{k\,t}} \qquad a = \sqrt{\frac{A_s}{\pi}} \qquad b = \sqrt{\frac{A}{\pi}} \tag{3.17}$$

3.2.3 "SLA" approximate equations

"SLA" approximate equations are developed by Song et al [103] and Lee et al [104]. Based on a model with a single heat source on a square plate (Figure 3.1), this set of equations can achieve good accuracy with an error of less than 5 % if certain geometrical and heat transfer

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conditions are met. It is found in [101] that errors can reach 20 % when $t < 1\,mm$ and $h/k < 10$.

To reduce the number of variables, the following non-dimensional parameters are presented as defined in (3.17).

$$\varepsilon = \frac{a}{b} \qquad \tau = \frac{t}{b} \qquad Bi = \frac{h\,b}{k} \tag{3.18}$$

$$\Psi_{max} = \sqrt{\pi}\; k\; a\; R_{cond,max} \tag{3.19}$$

$$\Psi_{av} = \sqrt{\pi}\; k\; a\; R_{cond,av} \tag{3.20}$$

Where ε, τ, Bi, Ψ_{max}, and Ψ_{av} are the dimensionless heat source radius and plate thickness, the effective Biot number, the maximum dimensionless conductive thermal resistance (based on the maximum junction temperature) and the average dimensionless conductive thermal resistance (based on the average junction temperature) respectively. R_{cond} is the conduction thermal resistance.

$$R_{conv} = \frac{1}{h\,A} \tag{3.21}$$

The maximum and average dimensionless conductive thermal resistances are then approximated by:

$$\Psi_{max} = \frac{\varepsilon\,\tau}{\sqrt{\pi}} + \frac{1}{\sqrt{\pi}}\,(1-\varepsilon)\,\Theta \tag{3.22}$$

$$\Psi_{av} = \frac{\varepsilon\,\tau}{\sqrt{\pi}} + \frac{1}{2}\,(1-\varepsilon)^{\frac{3}{2}}\,\Theta \tag{3.23}$$

where

$$\Theta = \frac{\tanh(\lambda\,\tau) + \frac{\lambda}{Bi}}{1 + \frac{\lambda}{Bi}\tanh(\lambda\,\tau)} \tag{3.24}$$

and

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$$\lambda = \pi + \frac{1}{\sqrt{\pi}\,\varepsilon} \tag{3.25}$$

The temperature difference from the junction to the ambient can be determined by equations (3.26) and (3.27) in terms of the applied heat Q, $R_{cond,max}$ and $R_{cond,av}$ can be calculated from equations (3.19) and (3.20), while R_{conv} is calculated from equation (3.21).

$$\Delta T_{max,JA} = Q\ (R_{cond,max} + R_{conv}) \tag{3.26}$$

$$\Delta T_{av,JA} = Q\ (R_{cond,av} + R_{conv}) \tag{3.27}$$

3.2.4 Orthotropic multi-layer multi-source heat spreading analytical model

Muzychka et al. ([105], [106]) introduced an analytical solution of the temperature rise in a 3D multi-layer stack with multi-heat sources and orthotropic thermal conductivities. This solution is based on applying the method of separation of variables to Laplace's heat transfer equation and Fourier series expansion. Stretched coordinate transformations are used to extend the solution to a multilayer stack. The solution can predict the temperature in any location for all layers. Examples shown in [105] and [106], demonstrate that there is a very slight error between the developed analytical solutions and FEM results. Figure 3.2 shows the geometrical properties of the model of multi-layer stack.

The solution is obtained for $\theta(x, y, z)$ which is the temperature difference between the temperature at a location in the 3D domain of the multi-layer stack $T(x, y, z)$ and a reference temperature T_r which can be chosen to be the ambient temperature (equation (3.28)).

$$\theta(x, y, z) = T(x, y, z) - T_r \tag{3.28}$$

The temperature in a 3-D solid is governed by the steady-state heat conduction equation. In the absence of internal heat generation, the steady-state conduction equation is reduced to Laplace's equation (3.29):

$$\nabla^2\theta = \frac{\partial^2\theta}{\partial x^2} + \frac{\partial^2\theta}{\partial y^2} + \frac{\partial^2\theta}{\partial z^2} = 0 \tag{3.29}$$

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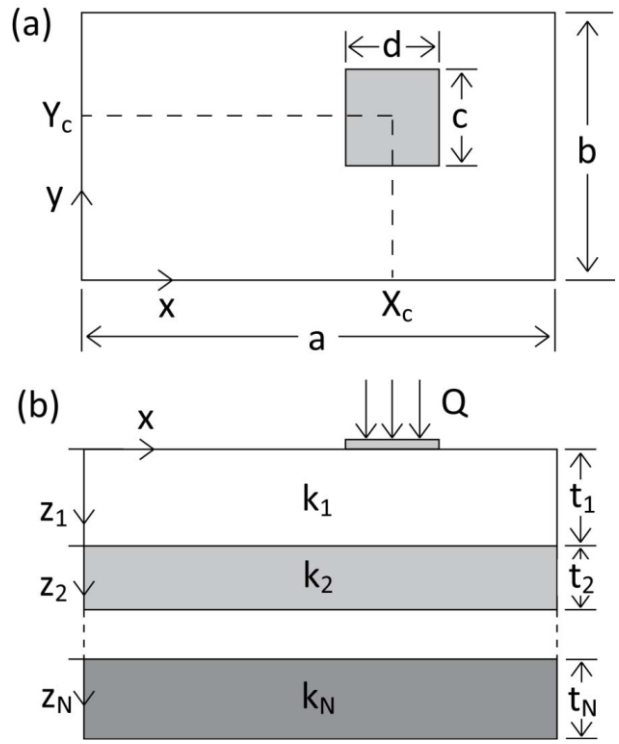

Figure 3.2: the geometrical properties of the model of multi-layer stack [106].

In the first layer (j=1) of the multi-layer stack, the boundary conditions are applied such that the heat (*Q*) is dissipated uniformly over the heat source area (*c d*) on the top plane (equation ((3.30)) while adiabatic boundary condition is considered elsewhere (equation ((3.31)).

$$-k_1 \left.\frac{\partial \theta_1}{\partial z_1}\right|_{z_1=0} = \frac{Q}{c\ d} \tag{3.30}$$

$$\left.\frac{\partial \theta_1}{\partial z_1}\right|_{z_1=0} = 0 \tag{3.31}$$

The adiabatic boundary condition is also applied at the sides of the multi-layer stack as described in equation (3.32).

$$\left.\frac{\partial \theta_j}{\partial x}\right|_{x=0,a} = 0 \qquad \left.\frac{\partial \theta_j}{\partial y}\right|_{y=0,b} = 0 \tag{3.32}$$

At the bottom side of the bottom layer (*j=N*), a heat transfer coefficient (h_s) is applied as described in equation (3.33).

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$$-k_N \left.\frac{\partial \theta_N}{\partial z_N}\right|_{z_N=t_N} = h_s\, \theta_N(x, y, t_N) \tag{3.33}$$

Considering a perfect contact interface between each two layers, the continuity condition is applied, meaning that the temperatures of both layers at the interface are identical (equation (3.34)). Also, the heat flux is conserved while transferring between the two layers (equation (3.35)).

$$\theta_j(x, y, t_j) = \theta_{j+1}(x, y, 0) \tag{3.34}$$

$$k_j \left.\frac{\partial \theta_j}{\partial z_j}\right|_{z_j=t_j} = k_{j+1} \left.\frac{\partial \theta_{j+1}}{\partial z_{j+1}}\right|_{z_{j+1}=0} \tag{3.35}$$

The solution for the increase in temperature $\theta_j(x, y, z_j)$ for the j^{th} layer can be written in terms of a double Fourier cosine series. In this solution, the ratio of Fourier coefficients A_{ij} and B_{ij} defines the spreading function $\emptyset_j(\gamma_n)$ as described in equation ((3.36) [106].

$$\emptyset_j(\gamma_n) = -\frac{B_{ij}}{A_{ij}} \tag{3.36}$$

Where $i = 0, 1, 2, 3$, and γ_n refers to the eigenvalues λ_m, δ_n, and β_{mn} ($\lambda_m = \frac{m\,\pi}{a}$, $\delta_n = \frac{n\,\pi}{b}$, $\beta_{mn} = \sqrt{\lambda_m^2 + \delta_n^2}$).

At the bottom layer ($j=N$), the spreading function is described in terms of the heat transfer coefficient h_s at the bottom boundary as in equation (3.37). For the precedent layers ($j=1:N-1$), the spreading function is described in equation (3.38).

$$\emptyset_N(\gamma_n) = -\frac{B_{iN}}{A_{iN}} = \frac{\frac{k_N\,\gamma_n}{h_s}\,\tanh(\gamma_n\, t_N) + 1}{\frac{k_N\,\gamma_n}{h_s} + \tanh\,(\gamma_n\, t_N)} \tag{3.37}$$

$$\emptyset_j(\gamma_n) = -\frac{B_{ij}}{A_{ij}} = \frac{\frac{k_j}{k_{j+1}}\,\tanh(\gamma_n\, t_j) + \emptyset_{j+1}(\gamma_n)}{\frac{k_j}{k_{j+1}} + \emptyset_{j+1}(\gamma_n)\,\tanh\,(\gamma_n\, t_j)} \tag{3.38}$$

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For the first layer (j=1), Fourier coefficients are defined as follows:

$$A_{11} = \frac{4\,Q\ \cos(\lambda_m\,X_c)\ \sin(0.5\,\lambda_m\,c)}{a\,b\,c\,k_1\,\lambda_m^2\,\emptyset_1(\lambda_m)} \tag{3.39}$$

$$A_{21} = \frac{4\,Q\ \cos(\delta_n\,Y_c)\ \sin(0.5\,\delta_n\,d)}{a\,b\,d\,k_1\,\delta_n^2\,\emptyset_1(\delta_n)} \tag{3.40}$$

$$A_{31} = \frac{16\,Q\ \cos(\lambda_m\,X_c)\ \sin(0.5\,\lambda_m\,c)\ \cos(\delta_n\,Y_c)\ \sin(0.5\,\delta_n\,d)}{a\,b\,c\,d\,k_1\,\lambda_m\,\delta_n\,\beta_{mn}\,\emptyset_1(\beta_{mn})} \tag{3.41}$$

$$A_{01} = \frac{Q}{a\,b}\left(\frac{1}{h_s} + \sum_{l=1}^{N}\frac{t_l}{k_l}\right) \qquad B_{01} = -\frac{Q}{a\,b\,k_1} \tag{3.42}$$

For the next layers (*j=2:N*), equation (3.43) is used to obtain A_{ij} for ($i = 1,2,3$). For $i = 0$, equation (3.44) is used.

$$A_{ij} = A_{i,j-1}\left[\cosh(\gamma_n\,t_{j-1}) - \emptyset_{j-1}\sinh(\gamma_n\,t_{j-1})\right] \tag{3.43}$$

$$A_{0j} = \frac{Q}{a\,b}\left(\frac{1}{h_s} + \sum_{l=j}^{N}\frac{t_l}{k_l}\right) \qquad B_{0j} = -\frac{Q}{a\,b\,k_j} \tag{3.44}$$

The general solution for the increase in temperature in all layers of a multi-layer stack can be obtained from equation (3.45). This analytical model is used below, and its MATLAB implementation is presented in (Appendix C). It can simulate heat transfer in a 3D, orthotropic and multi-layer stack with multiple heat sources (which corresponds to the features of the heat-spreader studied in chapter 4) in short time, which is useful for pre-design study stage.

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$$\theta_j(x,y,z_j) = A_{0j} + B_{0j}z + \sum_{m=1}^{\infty} A_{1j}\ \cos(\lambda_m\, x)\left[\cosh(\lambda_m\, z_j) - \emptyset_j(\lambda_m)\sinh(\lambda_m\, z_j)\right] + \sum_{n=1}^{\infty} A_{2j}\ \cos(\delta_n\, y)\left[\cosh(\delta_n\, z_j) - \emptyset_j(\delta_n)\sinh(\delta_n\, z_j)\right] + \sum_{m=1}^{\infty}\sum_{n=1}^{\infty} A_{3j}\ \cos(\lambda_m\, x)\ \cos(\delta_n\, y)\left[\cosh(\beta_{mn}\, z_j) - \emptyset_j(\beta_{mn})\sinh(\beta_{mn}\, z_j)\right] \quad (3.45)$$

3.2.5 Numerical solutions

Numerical approaches for solving the heat transfer equations are based on the discretization of the heat transfer domain into a large number of smaller and simpler domains. In situations where exact analytical solutions do not exist, numerical solutions are considered more accurate than analytical approaches, which require simplifications and approximations. However, they require more computational power and time. More details are given in section 3.3.

3.2.6 Test case for comparison

Optimizing a heat spreader requires to iterate over many designs. To choose a sufficiently accurate and fast modelling approach, a comparison between different heat transfer modelling approach is necessary.

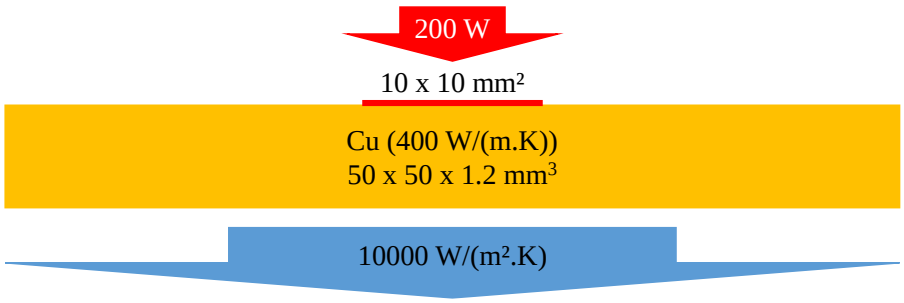

Figure 3.3: Comparison model for heat transfer approaches

For the sake of comparison, a simple model, with a single heat source on a single copper layer (400 W/(m.K)) is considered. As illustrated in Figure 3.3, a heat source of 200 W/cm² is applied on 10×10 mm² area on a copper layer of 50×50 cm² area and 1.2 mm thickness. A heat transfer coefficient (HTC) of 10000 W/(m²K) is applied at the bottom side. This simple model is solved using the modeling approaches described above, and compared to FEM numerical simulations.

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Table 3.1 shows R_{thJA} values calculated using each modeling approach and the error percentage with respect to FEM simulations.

Table 3.1: Comparison of the R_{thJA} between several heat transfer approaches.

Heat transfer modelling approach	R_{thJA} (K/W))	Error %
1-D series-resistance network	0.0412	− 84.3 %
"L" approximate equation [102]	0.3823	+ 50.2 %
"SLA" approximate equations ([103], [104])	0.2923	+ 14.9 %
Muzychka analytical solution model ([105],[106])	0.2649	+ 4.1 %
FEM simulations (ANSYS)	0.2545	REF

The 1-D series-resistance network has the highest error (84 %), because of the large area ratio between the heat source and the copper layer which contradicts the assumption of 1-D heat transfer. "L" and "SLA" approximate equations have errors of 50.2 % and 15 % respectively. These models deal with single heat source and a square plate as in the assumption. Only the area and the thickness of the layer can be defined. In addition, they only give the temperature difference between the power source and the ambient, and not a temperature distribution.

The analytical model of Muzychka ([105], [106]) achieves the smallest error, at 4 %, and it can also deal with multi-layer, multi-source, and layers with orthotropic thermal conductivity. It also provides an estimation of the increase in temperature at every location in the 3-D mutli-layer stack and can deal with rectangular geometries. Therefore, the analytical model of Muzychka ([105], [106]) is chosen for the parametric study to estimate the heat spreading requirements in chapter 4 section 4.1.

3.3 Numerical simulations

The numerical approach starts with a mathematical model which is the set of partial differential equations (or integro-differential equations) and boundary conditions to be solved. The mathematical model is chosen based on the application and corresponding assumptions that simplify the conservation law equations. After selecting the suitable mathematical model, a numerical discretization method is then chosen in order to approximate the mathematical model into a set of algebraic equations to be solved over a discretized computational domain. This computational domain is discretized into a grid of a finite number of subdomains [107]. These steps are described in the subsections below.

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This section presents a general overview of the most known numerical discretization methods. After that, we address the best-known mathematical models for turbulent flows to solve Navier-Stokes equations. Finally, the simulation tool used during this thesis is presented with some details on each type of simulations.

3.3.1 Numerical discretization methods

The numerical discretization method is a method of approximating the partial differential or integral equations into algebraic equations. These algebraic equations are function of the physical variables at discrete locations in space and time. The most recurrent numerical discretization methods are: the Finite Difference Method (FDM), the Finite Volume Method (FVM), and the Finite Element Method (FEM). All these numerical methods should yield the same results if the grid (mesh) is very fine. However, some of them are more suited to some types of problems, so it is important to select them wisely [107].

3.3.1.1 Finite Difference Method (FDM)

It is considered the easiest method to implement simple geometries. The computational domain is discretized into a grid. At each node of the grid, the partial derivatives of the conservation equation are approximated by algebraic terms as a function of the nodal values (values of the physical variables at each node of the grid). Therefore, the algebraic equation is solved at each node. Another advantage of this method is that it can easily be extended to discretization schemes with higher order of accuracy. FDM has some drawbacks such as: the need for some special care in order to enforce the conservation laws. Also, it is much more difficult to implement in general complex geometries, and for this reason this method is rarely used in commercial software.

3.3.1.2 Finite Volume Method (FVM)

The integral form of the conservation equation is used by the FVM. The computational domain is subdivided into multiple control volumes at which the conservation equation is applied. At each center of a control volume, there is a computational node at which the calculation is made. The values of the variables are expressed then on the surface of the corresponding control volumes using interpolation. Volume and surface integrals are approximated, and algebraic equation is then obtained to each control volume as a function of the nodal values [107].

The FVM is suitable for complex geometries, and it is simple to program which makes it popular for engineers. However, the disadvantage of FVM compared to FDM is that is more

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difficult to develop in 3D (for simple geometries) because the FVM requires three levels of approximation: interpolation, differentiation, and integration [107].

3.3.1.3 Finite Element Method (FEM)

Like FVM, the FEM requires breaking the computational domain into discrete subdomain, called finite elements. The difference is that in FEM, the equations are integrated over the computational domain after being multiplied by a weight function. In each element, the solution is approximated by a linear shape function while keeping the continuity of the solution across the boundaries of the element. The shape function is obtained from the corner values of each element. This approximation is then substituted into the weighted integral of the conservation equations and a set of non-linear algebraic equations is obtained [107].

FEM can deal with arbitrary geometries. This is an important advantage of this method, making it easy to refine the grid. In addition, FEM is relatively easy to analyze mathematically. However, the main disadvantage that could be shared by other method is that the matrices of the linearized equations are not very well structured, which increases the difficulty of finding efficient solving methods [107].

3.3.2 Numerical solutions to the Navier-Stokes equations

In order to deal with a turbulent flow (which is the case in this work), several approaches can be followed. Here are some of the most widely used.

3.3.2.1 Direct Numerical Simulation (DNS)

DNS is the most accurate and simplest solution that does not require averaging or approximation (other than the numerical discretization) [107]. In DNS, the flow motion of any scale is considered in the solution. In order to achieve a valid solution for turbulent flows, the mesh has to be very fine so as to capture all turbulence structures and kinetic energy dissipation. However, it is very computationally intensive [107].

3.3.2.2 Large Eddy Simulation (LES)

LES is a mathematical model to solve Navier-Stokes equations for turbulent flows. In order to reduce the computational cost, LES does not solve explicitly the small eddies in the turbulent , which are filtered out using a low-pass (spatial or temporal) filter. The large-scale eddies are more energetic than the small-scale eddies which make them more effective transporters for the conserved properties of the flow. The effect of the small-scale eddies on the large resolved scales is taken into account using so-called subgrid-scale models.

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LES is more accurate than the RANS approach but remains computationally expensive but much less so than DNS. In general, DNS is preferred because of its high accuracy whenever it is feasible. LES is preferred when the Reynold's number of the flow is too high, or the geometry is too complex. More details on LES can be found in [107].

3.3.2.3 Reynolds Averaged Navier-Stokes (RANS)

To model the turbulence in a flow, all variables in Navier-Stokes equations are averaged in time. Every variable is then written as the sum of a time-averaged value and a fluctuation about that value. This approach results in additional terms such as Reynold's stresses and turbulent scalar flux. The presence of these terms adds additional variables to the conservation equations, which requires turbulence models in order to model these terms as a function of the mean flow to remove any of the fluctuation part of the variables [107]. There are several turbulence models which can be chosen to implement in a CFD model such as: k-ε, k-ω, SST k-ω (often simply called SST), etc.

3.3.3 Modelling and simulation tools

In this thesis work, ANSYS workbench is used for modelling and simulations. It is a software platform that has several modules to design and simulate engineering models in order to validate design ideas and solve physical problems.

SpaceClaim is the Computer Aided Design (CAD) modeler tool provided by ANSYS. It is used to design and prepare all the CAD models for numerical simulations and prototype manufacturing. In addition, the meshing module is used for the discretization of the computational domain. The ANSYS mechanical module is used to perform thermal simulations on solid-only models while ANSYS CFX is used to perform CHT simulations where both solid and fluid domains are involved.

3.3.3.1 Modelling

During CAD modeling, geometric symmetries are taken into consideration whenever possible in order to reduce computational power needed for the numerical simulations. Also, some simplifications are made for the same reason without affecting the physical configuration. More details on the modelling can be found in chapter 4 and chapter 6. The CAD model is then transferred into the meshing module for the discretization of the computational domain.

The properties of the materials used for the simulations are specified in Table 3.2 ([122], [123], [114]). Since the thermal conductivity of SiC value changes significantly with the

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temperature [114] as shown in Figure 3.4, the value is taken at 70°C, the temperature at which the tests are performed.

Table 3.2: Material properties.

Material	Thermal conductivity W/(m.K)	Specific heat J/(Kg.K)	Density Kg/m^3
Copper	385	385	8933
FR4	0.3	1150	1850
Graphite (PGS)	1300 XY – 15 Z	850	1500
Adhesive (Pyralux LF0100)	0.22	1926	1100
SiC	300	690	3210
Prepreg (Rogers92 ML)	2.5	1150	2260
PA12	0.3	1800	1020

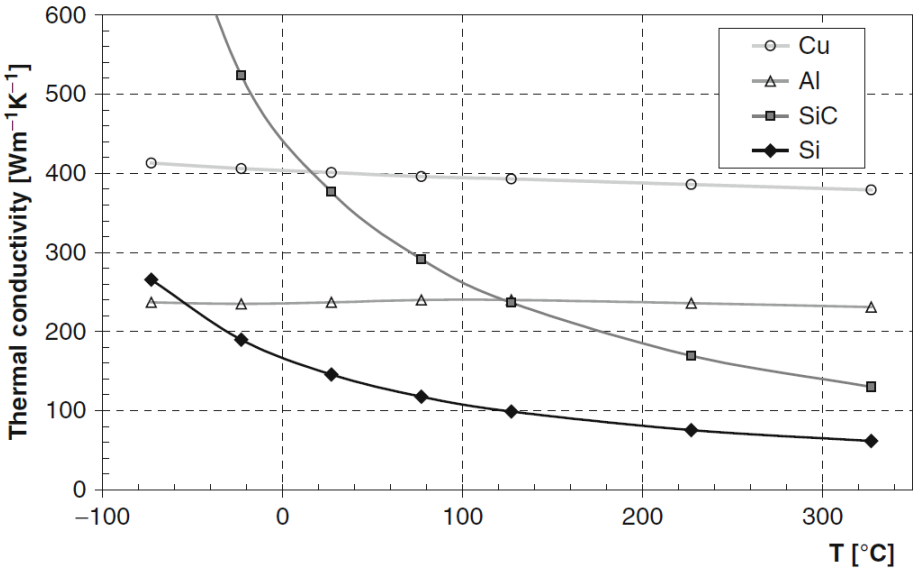

Figure 3.4: Thermal conductivity as a function of the temperature for Si, SiC, Al and Cu [114].

3.3.3.2 Meshing

In this work, unstructured tetrahedral elements are used to discretize the computational solid and fluid domains. The size of the elements varies depending on the geometry of each body. The minimum element size is set equal to 10^{-4} mm (or 8×10^{-5} mm in some cases) with "double refinement" option set at the side boundaries of the solid bodies (layers of the PCB). This mesh refinement ensures that the thickness of each solid layer is divided into at least 3 elements

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regardless of the element size (Figure 3.5). The meshing behavior is set as soft, and the growth rate is kept at 1.2 as the default.

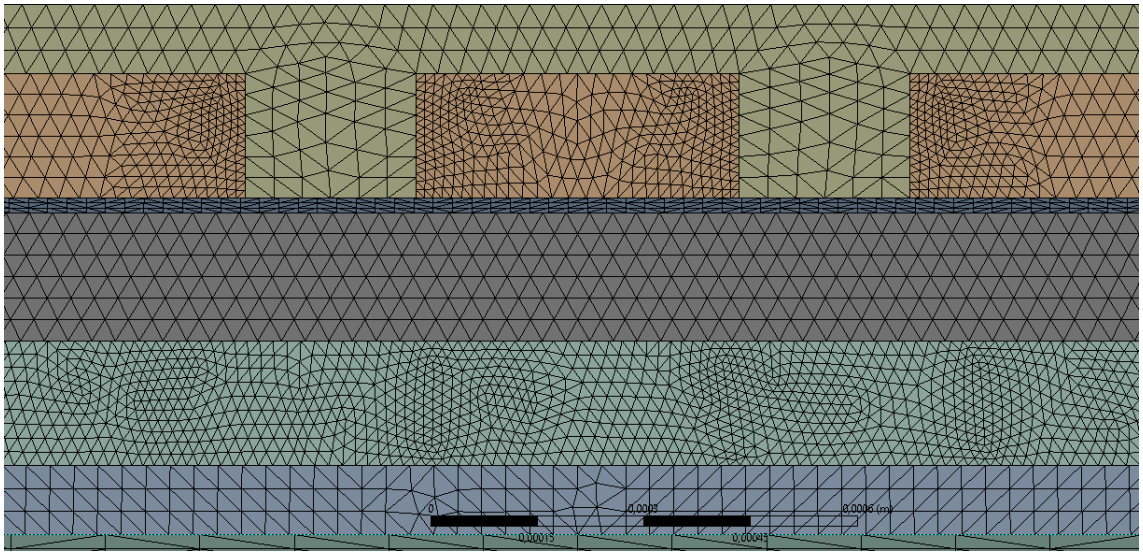

Figure 3.5: Meshing of several layers of a PCB.

For the fluid domain, inflation layers (prism layers) are set at the boundaries of the fluid (the interfaces between the fluid domain and the solid domain). These inflation layers provide higher mesh resolution at the fluid domain boundaries in order to capture the velocity and thermal boundary layers. 15 inflation layers are used with a growth rate of 1.2 and smooth transition for inflation option (Figure 3.6).

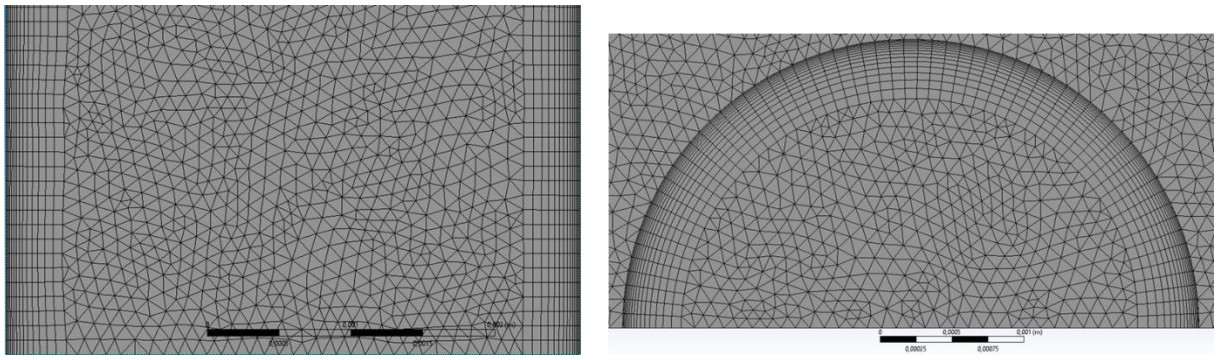

Figure 3.6: Meshing of the fluid domain with inflation layers at the boundaries.

3.3.3.3 Simulation setup

3.3.3.3.1 Mechanical – Thermal Analysis

The ANSYS workbench provides thermal analysis in the Mechanical module for solid bodies. The energy equation (3.11) is solved using FEM for numerical discretization method. Steady-state and transient thermal analysis are performed.

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For steady-state thermal analysis, only the thermal conductivity of each solid body is required to be assigned for the heat transfer application. Orthotropic thermal conductivities can be used.

Transient thermal analysis provides the variation of the temperature over time (needed to produce thermal impedance curves) using the energy equation for solids (3.13). The density and the specific heat appear in the transient term (the left-hand side of the equation (3.13)), so they have to be defined each body material.

The total time considered for the transient thermal analysis in this thesis is 10 seconds in order to ensure reaching the steady state. Assigning a realistic initial temperature is important in transient thermal analysis. The reference temperature in all simulations is set equal to 22°C (ambient). In all transient thermal analysis in this thesis, the initial temperature is set equal to the ambient temperature (22°C).

The boundary conditions for these simulations are detailed in chapter 4 (section 4.2.6).

3.3.3.3.2 CFX

Steady-state CHT simulations are performed using ANSYS's CFX solver. As explained in section 3.1.3, both thermal energy and Navier-Stokes equations are solved. CFX uses the RANS model for turbulent flows. The fluid used in this thesis is water with a reference temperature of 22°C.

Regarding the turbulence model, In [108], 13 turbulence models are investigated in order to find the most suitable one for a highly turbulent, single-jet flow. It is recommended to use the SST turbulence model for jet impingement since it predicts the laminar-turbulent transition with higher accuracy compared to other turbulence models. Also, it is found in [109] that the SST turbulent model can predict the heat transfer coefficient better (however it can overestimate the pressure drop). In this thesis work, SST turbulent model is therefore chosen.

Regarding solver control settings, the "advection" scheme is set to high resolution (default). The" turbulence numerics" option is set to first order (default). For the convergence criteria, the residual type is set to RMS (root mean square) and the target is to reach 10^{-4}.

At solid-fluid interfaces, the non-slip condition is applied (flow velocity at the wall is zero). At all solid-solid and solid-fluid interfaces, the heat transfer option is set to "conservative interface flux" in order to conserve the heat across the interfaces.

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For the boundary conditions of the fluid domain, velocity is set at the inlet with an inlet temperature of 22°C. At the outlet, the pressure and temperature are set to the atmospheric values (101325 Pa and 22°C). The boundary conditions of the CHT simulations are detailed in chapter 6.

3.3.3.4 Simulations post-processing

During simulations, certain parameters are monitored in order to evaluate the thermal resistance and the thermohydraulic performance. The temperature is calculated all over the computational domain and 3D contours are obtained. The junction temperature T_j is taken as the maximum temperature on top of the chip (where the heat is generated). The thermal resistance R_{thJA} is then calculated as a function of T_j (Equation (3.46)) where T_r is the reference temperature of 22°C and Q is the total heat dissipated from the chip.

$$R_{thJA} = \frac{T_j - T_r}{Q} \tag{3.46}$$

In case of a transient simulation, T_j is monitored for each time step in order to obtain the thermal impedance Z_{th} curve, following equation (3.47).

For the junction-to-case thermal resistance R_{thJC}, the experimental method explained in section 3.4.2 (perform the acquisition twice, with two different thermal interface materials) is mimicked in simulations. The details of applying that method to simulations are explained in section 4.2.6 of chapter 4.

Regarding the CHT simulations, the pressure drop ΔP is obtained as the difference between the total pressure at the inlet and the outlet of the cooling water. To obtain the impact of the flow rate on R_{thJA} and ΔP, the inlet velocity is varied in order to cover the range of flow rates considered for comparison with the measurements.

3.4 Thermal experimental measurements

In order to validate the results of the numerical simulations, experimental measurements are performed and compared to simulations. In this section, thermal impedance measurements are described for R_{thJA}. Also, the method of predicting R_{thJC} is illustrated. Finally, the thermo-hydraulic experimental setup for the water jet impingement cooler (JIC) is presented.

3.4.1 Thermal impedance Z_{th} and R_{thJA} measurements

The objective of these measurements is to quantify the thermal resistance of the PCB package from the junction temperature of the chip to the reference temperature (ambient temperature, coolant inlet temperature,...etc).

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The thermal impedance (Z_{th}) is the difference between chip junction temperature (T_j) at certain time during heating and a reference temperature (T_r) divided by the dissipated power Q as the following equation (3.47):

$$Z_{th(j-r)}(t) = \frac{T_j(t) - T_r}{Q} \tag{3.47}$$

When the thermal impedance reaches a steady state, its value becomes equal to the thermal resistance R_{th}.

The thermal impedance measurement is performed using a thermal analyzer (AnalysisTech Phase 12 [110]). This system automatically injects a given power level in the sample under test to force it to heat-up, and then monitors a Temperature-Sensitive Electrical Parameter (TSEP) of the sample during the cooling down phase.

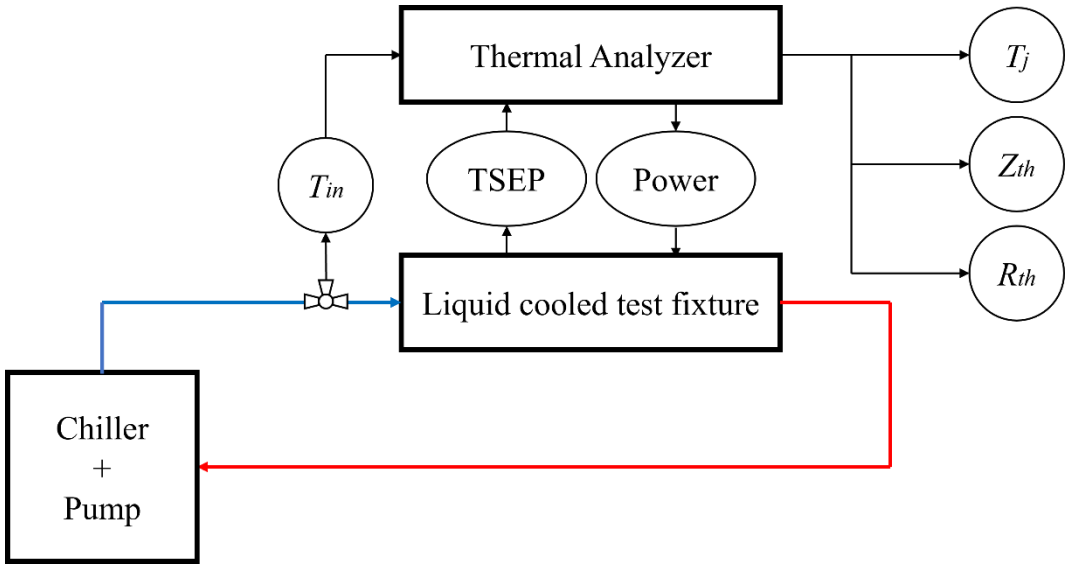

Figure 3.7: Schematic of the thermal experimental setup

The system is composed of the Phase 12 thermal analyzer, a liquid-cooled test fixture, and a recirculating chiller (National Lab GUPCPR020.03-NED [111]). In addition, an oven is used for the calibration of the semiconductor devices to be tested with the thermal analyzer. Figure 3.7 shows a schematic of the thermal experimental setup.

3.4.1.1 Calibration of the devices under test

The junction temperature T_j is obtained by measuring a (TSEP) of the semiconductor chip. In order to obtain the relationship between the TSEP and the junction temperature, the chip is

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calibrated by placing it in the calibration oven with no power dissipated (assuming $T_j = T_r$). The temperature in the oven is then slowly varied and the corresponding TSEP values are recorded.

Two types of semiconductor chips are used in this work: SiC diodes and SiC MOSFETs. The TSEP of the diodes is their forward voltage drop. For the MOSFETs, the TSEP is the forward voltage across the body diode with a V_{GS} = -5 V bias. Both TSEPs are measured under a biasing current of 5 mA, a current value which is low enough to cause negligible heat dissipation. Figure 3.8 and Figure 3.9 show the calibration electrical circuit for the diodes and MOSFETs respectively. Sense high/low are where the TSEP voltage is measured.

The device is placed in the calibration oven where the temperature increases until reaching 80°C. Then the oven tuns off and the cooling down takes place (a temperature overshoot is observed, up to 105-110°C). As cooling down is slower than heating up, it results in a more homogeneous temperature distribution in the oven. Figure 3.10 shows an example of a diode calibration curve showing the relation between the junction temperature and the TSEP (junction voltage).

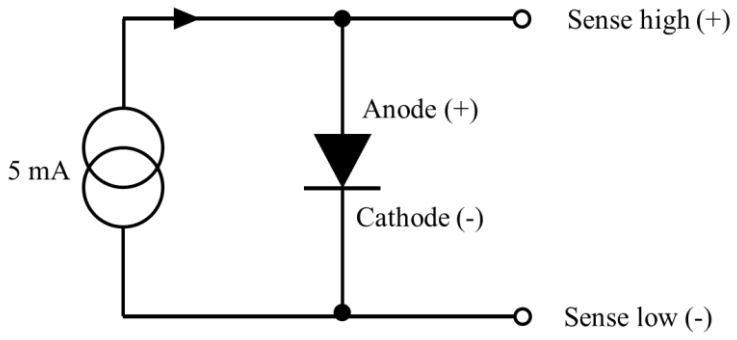

Figure 3.8: Electrical circuit for diode calibration.

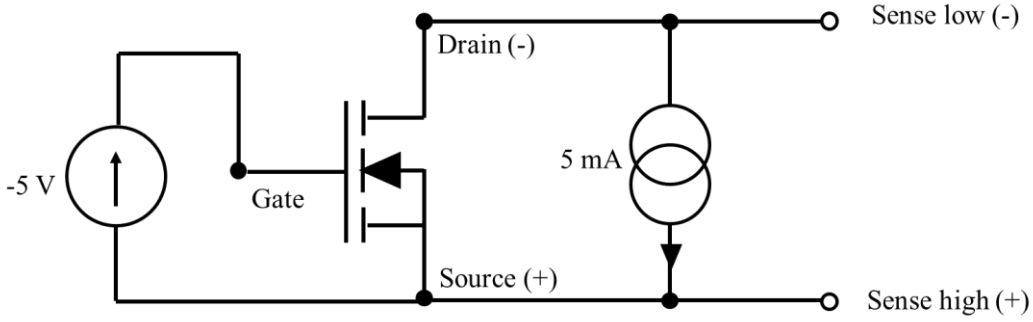

Figure 3.9: Electrical circuit for MOSFET calibration.

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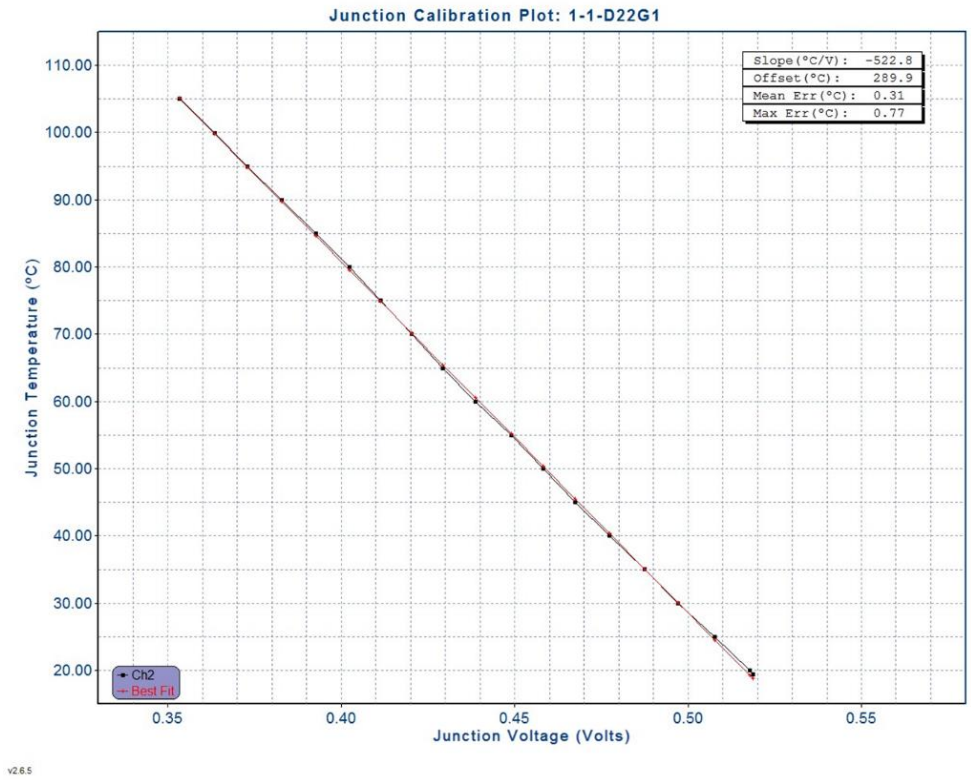

Figure 3.10: Calibration curve showing the relation between the junction temperature and voltage of the embedded diode.

3.4.1.2 Accuracy estimation of Z_{th} measurements

The manual of the thermal analyzer indicates an accuracy of ± 0.5°C for the TSEP measurements [112], and that shows that ± 0.5°C can be expected for the "T-type" thermocouple that measures the water inlet temperature of the cold plate [112]. In addition, the calibration curve of the die introduces some more uncertainties: calibrating the same SiC chip several times results in an estimated variation of ±1.7°C in T_j (as shown in Figure 3.11). Other sources of error (estimation of the dissipated power, etc.) are considered negligible here. As a result, an accuracy estimation for the thermal resistance R_{thJA} of around ± 6 % (or a total ±2.7°C accuracy) for a ($T_j - T_r$) temperature difference of 47°C is considered (assuming T_j = 70°C, the value typically used in our experiments). A lower T_j, i.e. a lower ($T_j - T_r$) temperature difference would lead to an even lower accuracy of R_{thJA} measurement.

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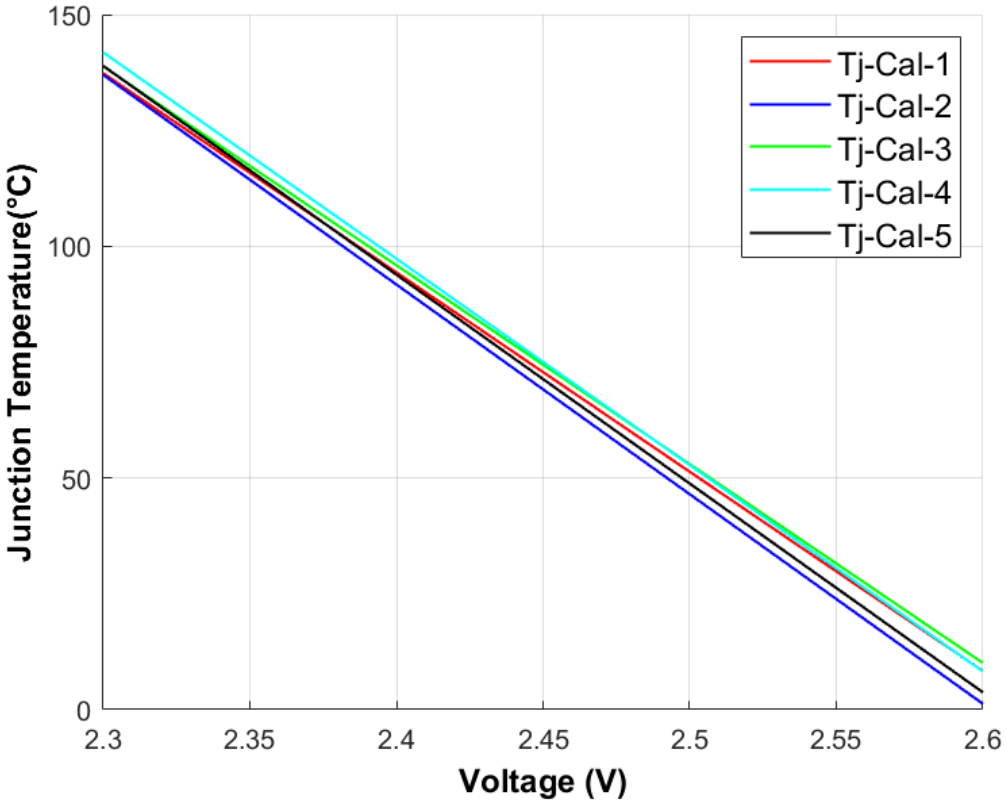

Figure 3.11: Several calibration curves for the same SiC MOSFET showing some uncertainty in the slope of the $V_f(T_j)$ characteristic (offset differences are not relevant, as they are canceled at the beginning of the measurement procedure, before any power is dissipated and $T_j=T_r$).

3.4.1.3 Test setup and Measurements.

For the characterization of PCBs with or without heat spreaders, the PCB sample is clamped on a cold plate with a Thermal Interface Material (TIM: Sil-Pad®1500ST [113], which has a thermal conductivity of 1.8 W/(m.K) and a thickness of 0.2 mm). A clamping pressure of 1.8 bar is applied at the level of contact with the cold plate. An elastomeric mat (Viton) and a rigid PEEK block are used for homogeneous distribution of the pressure on the 0.8 mm thick PCB sample. An alignment jig is fixed on the cold plate to maintain PCB sample position in order to ensure the repeatability of the tests.

Connectors are soldered on the PCB sample terminals to facilitate the electrical connection to the thermal analyzer. The cold plate is cooled by water circulation with an inlet temperature of 23°C (±0.5°C), which is taken as T_r for thermal impedance and thermal resistance calculation. The applied power is adjusted for different PCB variants to keep T_j around 70°C, to ensure the same level of accuracy regardless of the PCB variant and the TIM used.

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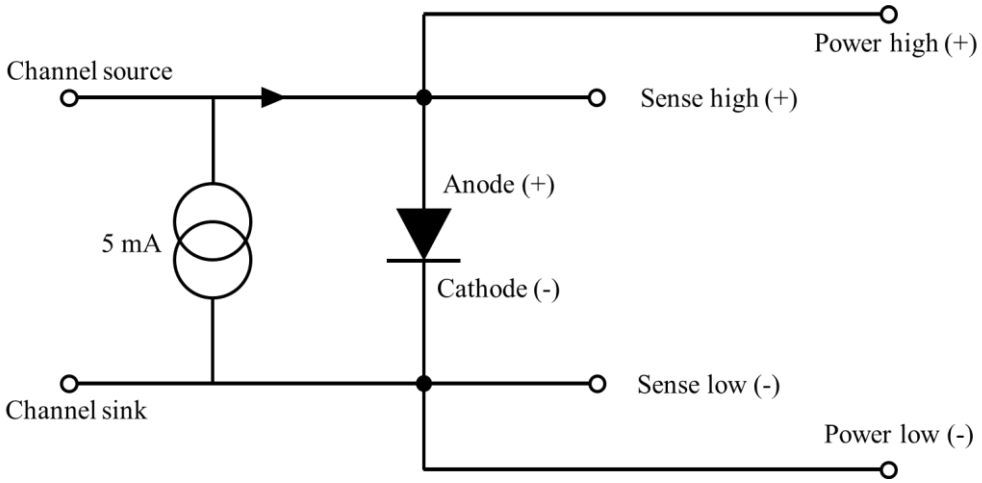

Figure 3.12: Electrical circuit for diode Z_{th} measurement.

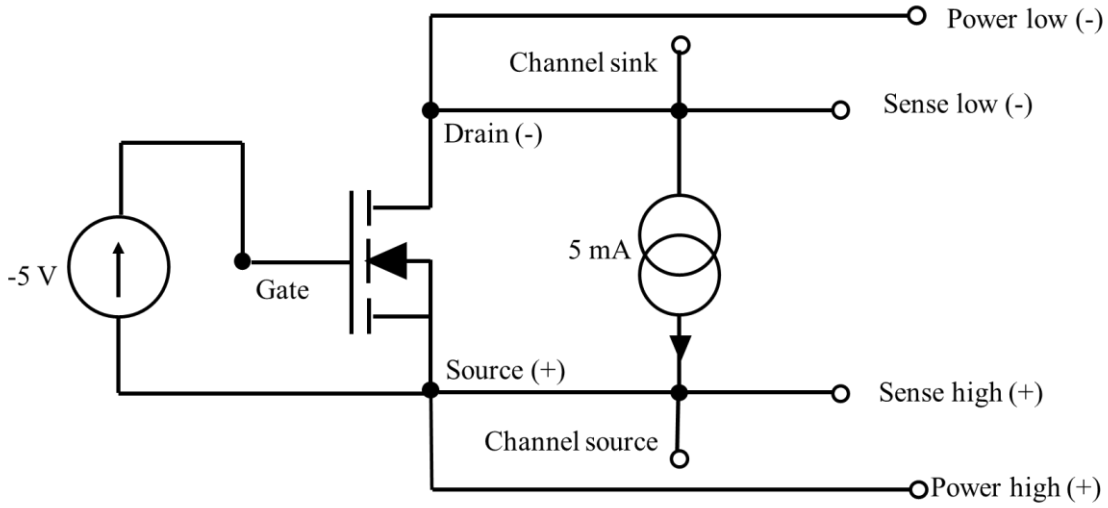

Figure 3.13: Electrical circuit for MOSFET Z_{th} measurement.

Figure 3.12 and Figure 3.13 show the electrical circuit for the Z_{th} measurements of the diode and MOSFET respectively, while Figure 3.14 shows the test fixture for the thermal impedance and thermal resistance tests.

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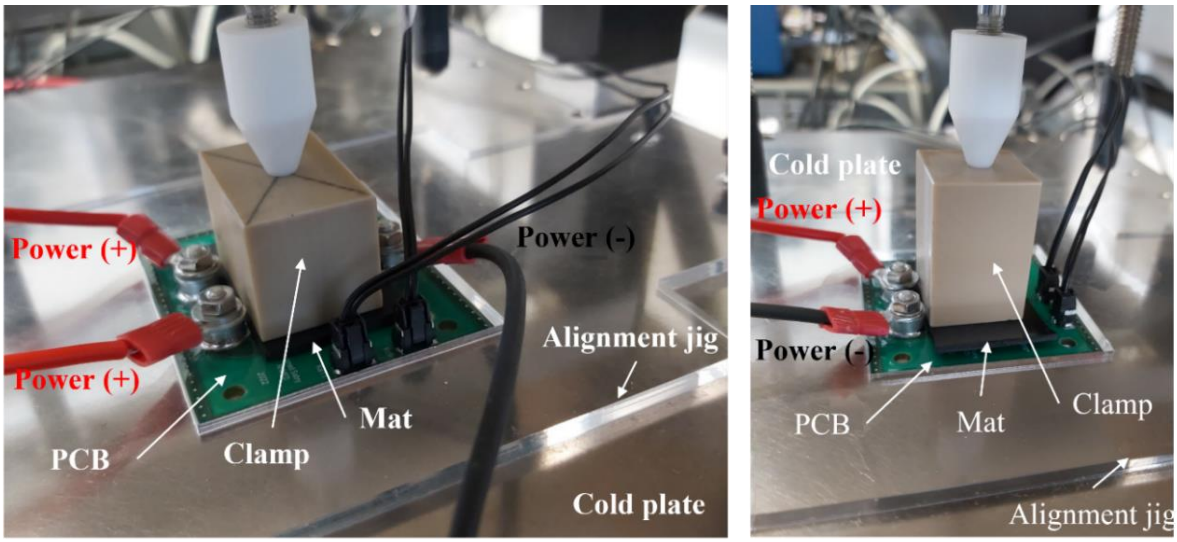

Figure 3.14: Experimental test fixture for thermal measurements. Dual-chips PCB sample (left) and single-chip PCB sample (right).

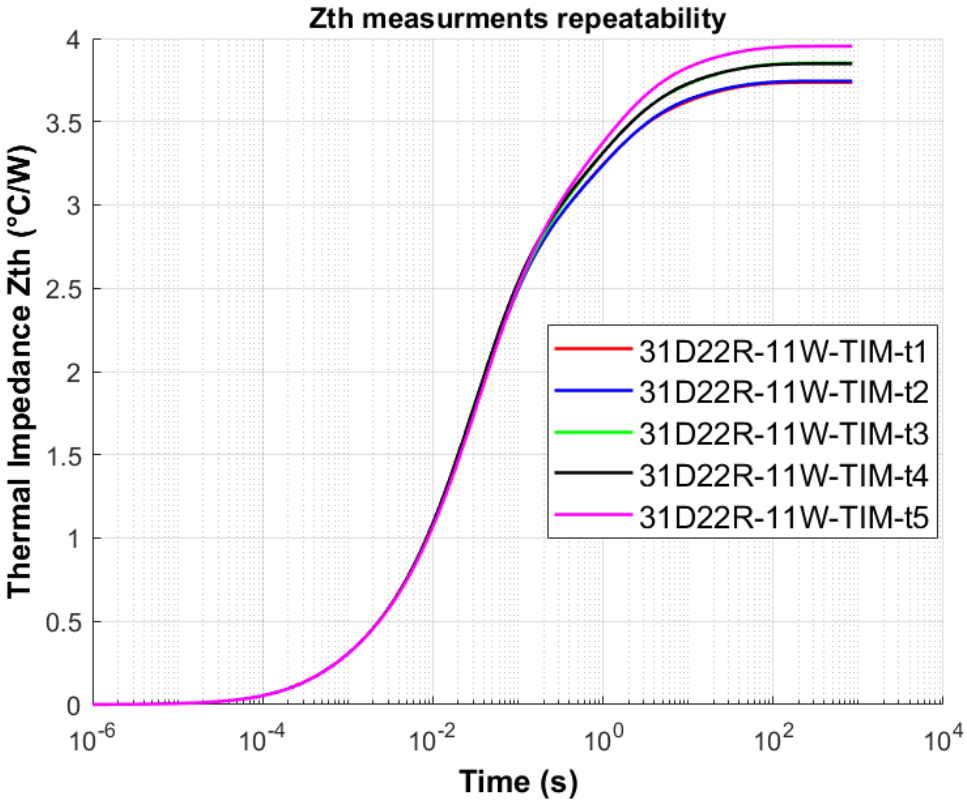

Figure 3.15: Typical results of Z_{th} measurements on the same diode.

Figure 3.15 shows an example of the Z_{th} measurements for a PCB sample at 11 W. Five measurements are taken, then the average is calculated at the steady-state values of the Z_{th} curves which corresponds to the R_{thJA} value (3.83 K/W in this example). The repeatability of the measurements of this example shows a standard deviation of about 0.09 K/W. Note that

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most of the measurements show better repeatability with less standard deviation (around 0.04) as will be seen in section 5.4 in chapter 5.

3.4.2 Thermal Dual Interface Method (TDIM) for R_{thJC} estimation

The junction to case thermal resistance (R_{thJC}) can be calculated using a local measurement of the temperature of the case (on a given location on the bottom surface of the PCB sample) as the reference temperature T_r. However, the case is not isothermal, especially considering the flat form factors of a PCB (very thin and large, resulting in large temperature differences across the surface). In this thesis, we use TDIM to estimate the R_{thJC} of the PCB samples, as it does not rely on a case temperature measurement. TDIM is described in the JEDEC51-14 standard [115].

3.4.2.1 Measurement principle

TDIM is a differential technique that is based on measuring the thermal impedance Z_{th} of a sample twice, with two different TIMs having significant difference in thermal resistance. The difference in TIMs creates a change in the heat path resistance, which results in a separation between the two thermal impedance curves. According to JEDEC51-14 standard, the separation point is assumed to take place at the interface between the PCB package and the TIM. Therefore, the thermal impedance value at which the separation takes place corresponds to R_{thJC}.

3.4.2.2 R_{thJC} value estimation procedure

The estimation procedure of R_{thJC} starts by performing the thermal impedance Z_{th} measurements on the device with two different TIMs (or with and without TIM) in order to create the separation between the two Z_{th} curves.

As illustrated in [116], Figure 3.16 shows two Z_{th} curves obtained: (a) using a thermal grease (as a TIM) in the first measurement, and (b) without thermal grease in the second measurement (to create higher contact thermal resistance with the cold plate). As shown in the Figure 3.16, a difference in steady state thermal resistance is obtained (ΔR_{th}).

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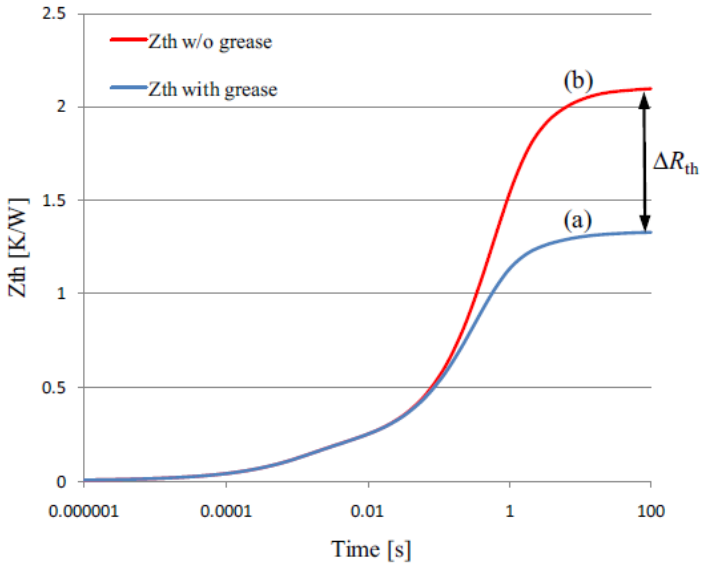

Figure 3.16: The separation between the two Z_{th} curves (a) using a thermal grease, and (b) without thermal grease [116].

The second step is to determine the point of separation. Because the actual separation point is not obvious from the figure, JEDEC51-14 describes an analysis method: the derivatives of the Z_{th} curves as a function of logarithmic time, da/dz, are obtained as illustrated in the equations below. z is the logarithmic time as indicated in equation (3.48) and $a(z)$ is the Z_{th} value as a function of the logarithmic time (i.e. equation (3.49)).Therefore da/dz equals to the slope of the Z_{th} curve in the log-linear representation. After that, the difference between the slope of the two Z_{th} curves are obtained, $(\Delta(da/dz))$ is obtained, as shown in Figure 3.17.

$$z = \ln(t) \tag{3.48}$$

$$a(z) = Z_{th}(t) \tag{3.49}$$

Therefore, the third step is to obtain the normalized difference of the derivatives (δ) as shown in the equation, where ΔR_{th}, is the maximum difference between Z_{th} curves when reaching steady-state.

$$\delta(z) = \frac{\Delta(da(z)/dz)}{\Delta R_{th}} \tag{3.50}$$

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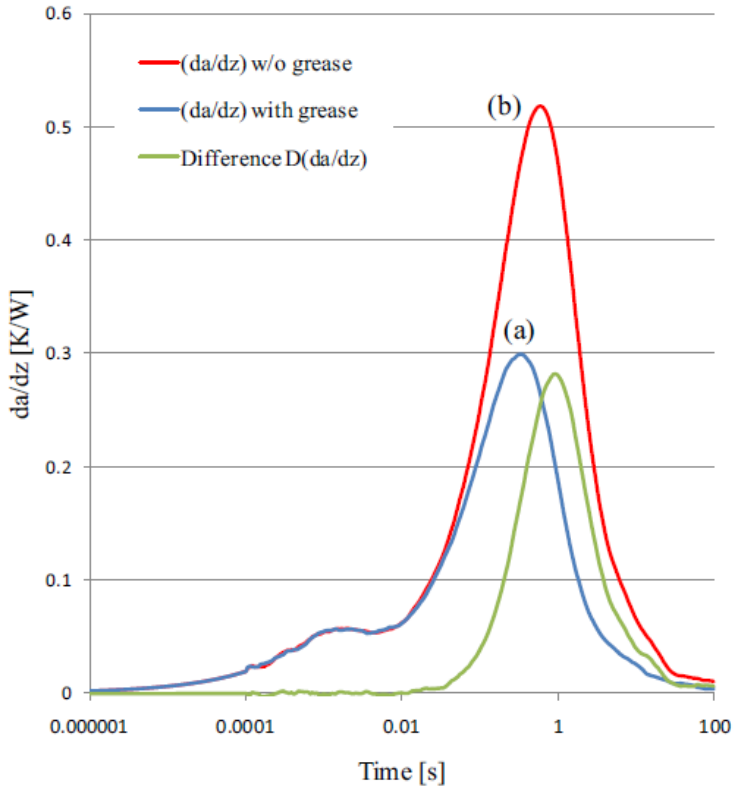

Figure 3.17: The difference between the slope of the two *Zth* curves are obtained $\Delta(da/dz)$ [116].

As explained in the JEDEC51-14, the separation point is defined as the point where the normalized difference of the derivatives δ exceeds a certain separation distance ϵ [116]. Based on FEM simulations, JEDEC51-14 proposes the following definition of ϵ:

$$\epsilon = 0.0045\, R_{th} + 0.003 \tag{3.51}$$

The actual value of the separation distance ϵ depends on several parameters such as the interfaces between the device and the cold plate (TIM), the geometry and material characteristics of the device under test, and the thermal resistance of the cold plate [116]. This can affect the accuracy and the reproducibility of the test. However, the definition of ϵ in (3.51) is adopted in JEDEC51-14 as a suitable approximation for most cases.

The last step is to determine the intersection between δ and ϵ which indicates the separation point between the two Z_{th} curves, hence the R_{thJC}. Figure 3.18 shows the intersection between δ and ϵ indicating the value of R_{thJC} as illustrated in [116].

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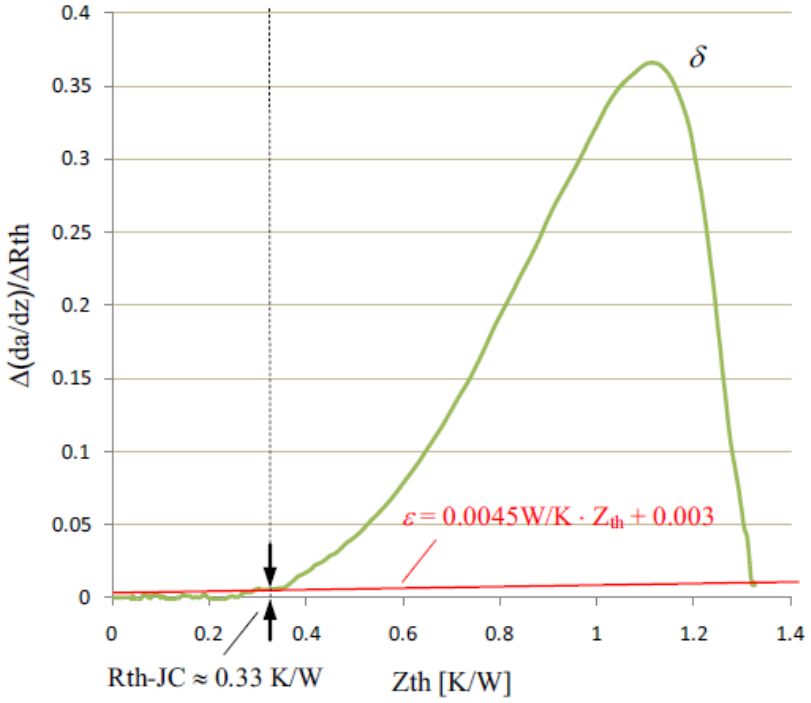

Figure 3.18: The intersection between δ and ϵ indication the value of R_{thJC} [116].

In this thesis work, a custom MATLAB code (Appendix D) is used to calculate R_{thJC} following the TDIM procedure described above. The same code is used for both measurement and simulation data.

3.4.2.3 TIMs used for measurements

To choose the best suitable combination of two TIMs to be used in R_{thJC} measurements, four TIMs (in addition to a dry case without TIM) are initially investigated. These must achieve enough difference in thermal resistance to create a clear separation in Z_{th} curves and high repeatability, but not too much so that the heat path is not changed completely. Table 3.3 lists the investigated TIMs.

Considering a two-TIMs configuration, the thermal impedance measurement is taken 3 times for each TIM. R_{thJC} values are then calculated using each combination of two Z_{th} measurements (i.e. 9 values for 3 measurements with each TIM) Then, the average and the standard deviation is calculated.

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Table 3.3: TIMs candidates for R_{thJC} measurements.

TIM	*k (W/m K)*	Thickness
TIM1: Thermal Pad (Sil-Pad®1500ST)	1.8	0.2 mm
TIM2: Thermal Pad (GCS-104-PCM-150150-0.12)	4	0.12 mm
TIM3: Metal Oxide Thermal Paste (RS 554-311)	0.65	-
Deionized Water (3 droplets)	0.58	<< 0.2 mm
No TIM (dry)	-	-

The tables below show some examples of these measurements in order to choose the best two-TIMs combination.

Table 3.4: R_{thJC} measurements using TIM1 with no TIM combination.

PCB sample		No TIM		
		1	2	3
TIM1 1.8 W/(m.K)	1	2.15	2.082	NAN
	2	2.029	1.958	2.117
	3	2.043	1.949	2.087
R_{thJC}_Av (K/W)	2.052			
STD (K/W)	0.072			

Table 3.5: R_{thJC} measurements using TIM2 with no TIM combination.

PCB sample		No TIM		
		1	2	3
TIM2 4 W/(m.K)	1	0.636	0.582	0.608
	2	0.581	0.532	0.556
	3	0.907	0.832	0.832
R_{thJC}_Av (K/W)	0.674			
STD (K/W)	0.142			

Table 3.6: R_{thJC} measurements using de-water with no TIM combination.

PCB sample		no TIM		
		1	2	3
De-water	1	0.646	0.646	0.646
	2	0.596	0.596	0.596
	3	0.621	0.621	0.621
R_{thJC}_Av (K/W)	0.621			
STD (K/W)	0.0216			

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Table 3.7: R_{thJC} measurements using de-water with TIM1 combination.

PCB sample		TIM1		
		1	2	3
De-water	1	0.695	0.671	0.695
	2	0.642	0.619	0.642
	3	0.668	0.644	0.668
R_{thJC}_Av (K/W)	0.66			
STD (K/W)	0.0257			

Table 3.8: R_{thJC} measurements using TIM1 with the thermal paste combination.

PCB sample		TIM1 (1.8 W/(m.K))		
		1	2	3
Thermal Paste 0.65 W/(m.K)	1	0.869	0.929	0.929
	2	0.999	0.999	0.999
	3	0.749	0.804	0.804
R_{thJC}_Av (K/W)	0.898			
STD (K/W)	0.0957			

Table 3.9: R_{thJC} measurements using de-water with the thermal paste combination.

PCB sample		Thermal Paste 0.65 W/(m.K)		
		1	2	3
De-water	1	0.447	0.571	0.571
	2	0.447	0.526	0.526
	3	0.467	0.548	0.548
R_{thJC}_Av (K/W)	0.517			
STD (K/W)	0.0503			

Figure 3.19: Application of the thermal paste on the PCB using a stencil.

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The combination TIM1/NOTIM shows a late separation between the two thermal impedance curves which results in high R_{thJA} values compared to other combinations of TIMs. This indicates that there is no enough difference in the thermal resistance between the two TIMs. The TIM2/NOTIM combination (TIM2 is a phase change material) shows a high standard deviation between the R_{thJA} (0.142 K/W) which indicates low repeatability. The reason can be that the TIM2 material is difficult to manipulate which makes a difference between each Z_{th} measurement. De-water/NOTIM and de-water/TIM1 combinations work fine with a small standard deviation of (0.022 K/W and 0.026 K/W, respectively). The combination of TIM3/TIM1 has a fairly high standard deviation (~0.1 K/W). Generally, TIM3 (thermal paste) requires special application (using stencil) to ensure tests repeatability which complicates the process of the measurements. Figure 3.19 shows the application of TIM3 (the thermal paste) on the PCB to ensure a constant thickness of the thermal paste for each measurement.

As a conclusion on these trials of TIMs combinations, the de-water/TIM1 couple is found satisfactory in both value and standard deviation, as the de-water/NOTIM. The use of TIM1 is preferred over NOTIM since TIM1 was already used during the measurements of the thermal impedance Z_{th} in order to obtain R_{thJA}, so their Z_{th} curves are used.

For the rest of the work in this thesis, de-water/TIM1 couple is used for all R_{thJC} measurements. Figure 3.20 presents two Z_{th} curves using the chosen TIMs showing a clear separation between them.

Table 3.10 shows the thermal conductivity (k) and the thickness of the two TIMs chosen for the measurements to estimate R_{thJC}: a commercial thermal pad, and 3 droplets of deionized water.

Table 3.10: TIMs used in R_{thJC} determination using TDIM.

TIM	***k (W/m K)***	**Thickness**
Thermal pad (Sil-Pad®1500ST)	1.8	0.2 mm
Deionized water (3 droplets)	0.58	<< 0.2 mm

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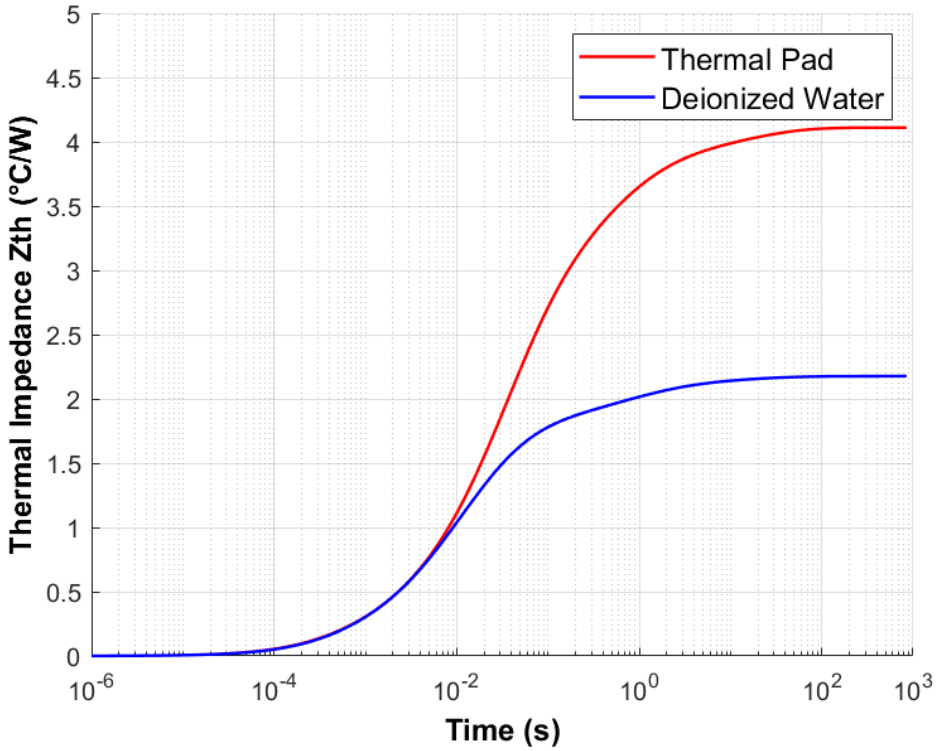

Figure 3.20: Example of Z_{th} curves using the chosen TIMs.

3.4.2.4 Concerns about TDIM accuracy and reproducibility

TDIM is sensitive to many parameters which can affect the accurate estimation of R_{thJC}, especially for PCB packages. The JEDEC51-14 standard evokes a ± 20 % accuracy [116].

Some studies tried to improve the accuracy and the reproducibility of the TDIM. A guide for improvement is presented in [117]. As mentioned above, one key element is that the selected TIMs should be different enough to create a separation between the Z_{th} curves, while maintaining the same heat flow path. Also, test conditions such as position of the sample, clamping pressure position and homogeneity should be consistent throughout the tests. In [118], it is suggested to extend the scope of TDIM since it is more suitable for large modules with a single, dominant heat flow path. This makes TDIM less suitable for small packages with heat spreading patterns and makes it difficult to obtain accurate and repeatable results using TDIM. Overall, in this thesis, a ±20 % accuracy will be considered, which means that variations below this threshold will not be considered significant.

3.4.3 Thermo-hydraulic experimental setup

The objective of this setup is to quantify the thermal performance of the water jet impingement cooler (JIC) in terms of achieved R_{thJA} and pressure drop/volumetric flow-rate

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characteristics. The JIC is addressed in chapter 6, and replaces the cold plate described above in the full thermal management system (which include the heat spreader and the JIC).

In this setup, the thermal impedance measurement is performed using the same thermal analyzer (AnalysisTech Phase 12 [110]) as explained previously. The cooling water is circulated as shown in Figure 3.21 and Figure 3.22. The water circuit includes a pump (Totton Pumps: NDP25/4 [119]), and a heat exchanger connected to the recirculating chiller (National Lab GUPCPR020.03-NED [111]) in order to maintain the inlet temperature at a constant value (23°C). The water flow rate is measured using a flowmeter (RS PRO: RS511-3965 [120], covering a range of 0.25-6.5 L/min with an absolute error of ±0.1 L/min), the inlet temperature using a T-type thermocouple (with an absolute error of ±0.5°C), and the pressure drop using a pressure sensor (NXP: MPX5010DP [121], measuring up to 10 kPa with an absolute error of ±0.5 kPa). The water exits in an open tank connected to the pump which sucks the water back into the loop. Mainstream and bypass valves allow to adjust the water flow.

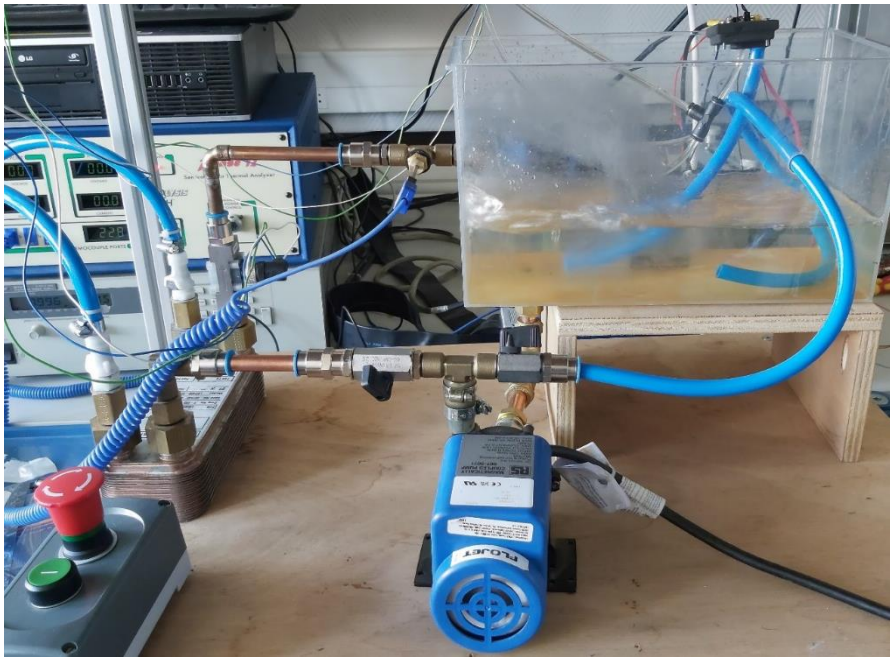

Figure 3.21: Thermo-hydraulic test setup.

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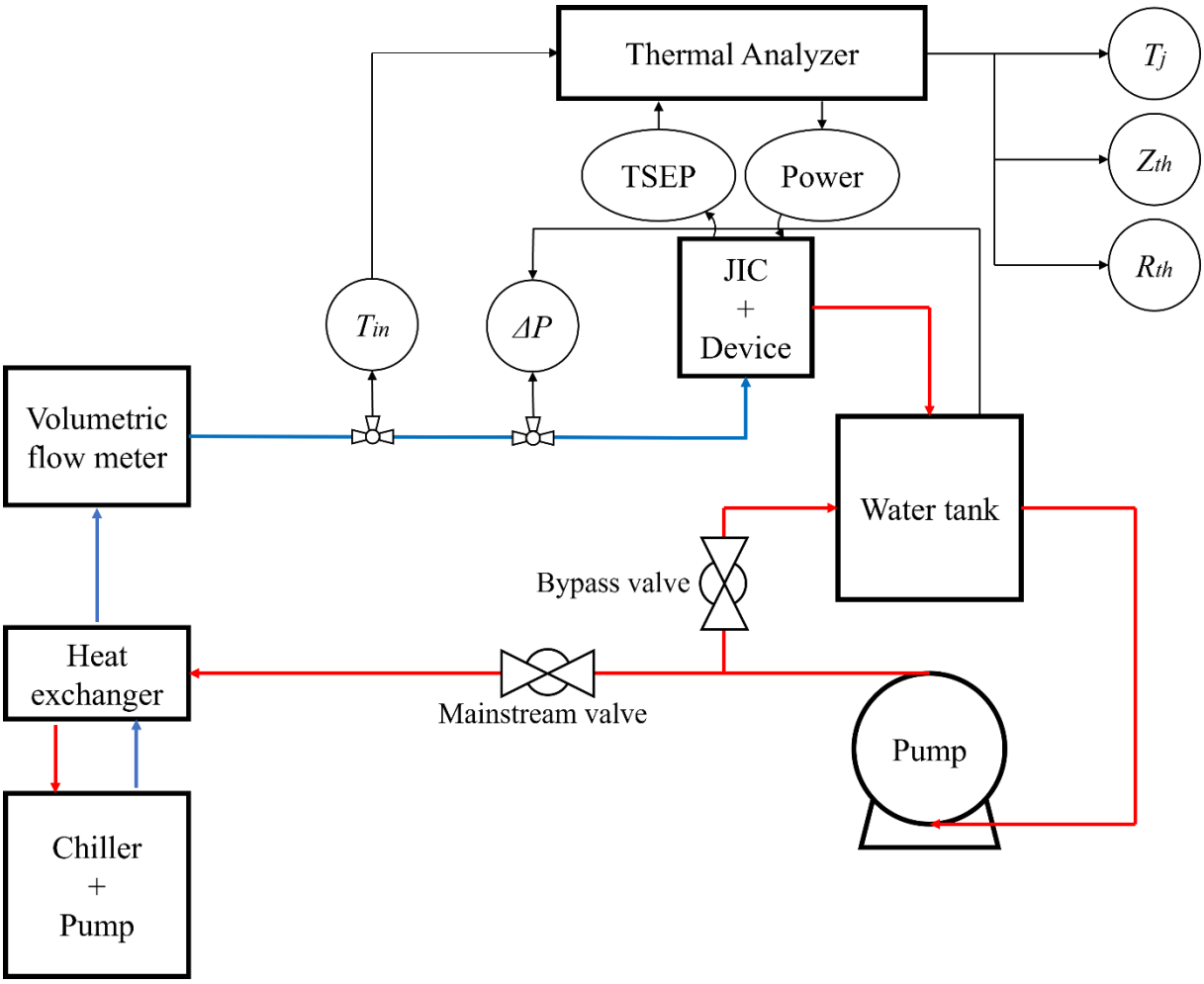

Figure 3.22: Schematic of the thermo-hydraulic experimental setup.

3.5 Conclusion

This chapter describes the involved heat transfer mechanisms and their governing equations. In addition, the analytical models and the numerical methods used in this thesis are briefly explained. The numerical simulation tools and their setup parameters were detailed as well as the experimental test setups for the experimental validation. The next chapters will focus on the results of the simulations and experimental validation tests.

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4 Heat Spreading – design and simulation

This chapter presents the design of the heat spreading solution by embedding graphite in a PCB package. It starts with a parametric study for the preliminary design. After that, the concept of embedding graphite heat spreaders in a PCB is presented. Finally, the detailed design based on manufacturing requirements, modelling, and FEM thermal simulations results for R_{thJA} and R_{thJC}, are presented. The next chapter (Chapter 5) will present the experimental validation of the heat spreading solution.

4.1 Parametric model to study heat spreading requirements

The objective of a heat spreader is to reduce the heat flux by enlarging the heat exchange surface, so that the heat flux can be absorbed by a suitable heat exchanger (here a jet impingement cooler). The thermal performance of the heat spreader depends on many parameters such as material characteristics and geometrical dimensions. In order to choose a heat spreading solution, a preliminary investigation is performed based on the analytical model of ([105], [106]) described in chapter 3 section 3.2.4.

The goal of the heat spreading solution is to enable the chip to operate at 500 W/cm² heat flux using a conventional cold plate for heat extraction. In order to choose a suitable heat spreader, R_{thJA} calculations are performed using a simplified model as illustrated in Figure 4.1.

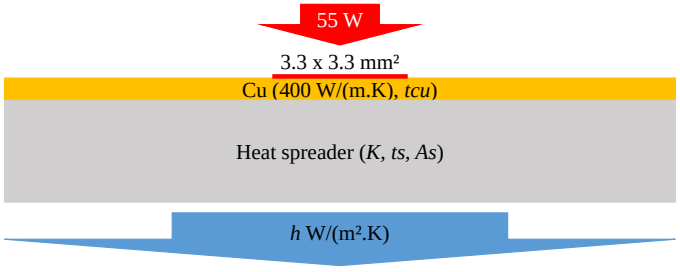

Figure 4.1: A simplified PCB model to choose the heat spreader characterizations.

The model is composed of a copper layer and heat spreader with a 55 W heat source on a 3.3×3.3 mm² chip area (500 W/cm²), which is representative of the chip size actually used in this work. A heat transfer coefficient (*h*) is applied on the bottom surface of the heat spreader to represent a heat sink. The heat transfer coefficient is varied from 100 to 100 000 W/(m².K) to cover air and liquid cooling heat sinks. The copper layer thickness (*tcu*) is varied from 35 µm (standard copper thickness for PCB) to 1 mm. Heat spreader thickness (*ts*), surface area (*As*), and thermal conductivity (*k*) are varied according to Table 4.1. The overall thermal resistance is calculated for 4 375 cases and saved in a 5-dimensional structure.

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Table 4.1 : The range of each parameter considered for the parametric study.

Parameter	**Range**
Heat spreader thermal conductivity *k* (W/(m.K))	100, 200, 400, 700, 1000, 1500, 2000
Copper layer thickness *tcu* (mm)	0.035, 0.1, 0.2, 0.5, 1
Heat preader thickness *ts* (mm)	0.1, 0.2, 0.5, 1, 5
Heat spreader area *As* (mm²)	5^2, 10^2, 20^2, 50^2, 100^2
Heat transfer coefficient *h* (W/(m².K))	100, 1000, 10000, 50000, 100000

4.1.1 Results and discussion

Figure 4.2 shows that R_{thJA} decreases as *h* increases (the other parameters remain constant).

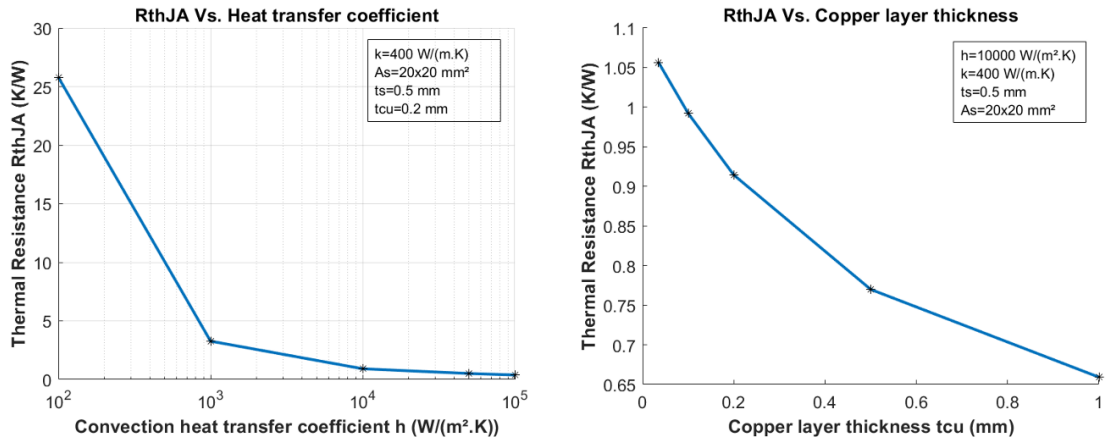

Figure 4.2: R_{thJA} against *h* (left) and top copper layer thickness *tcu* (right).

R_{thJA} drops dramatically (from 25.8 K/W to 3.3 K/W) as *h* increases from 100 to 1000 W/(m².K). The gain achieved after that by increasing *h* to 10000 W/(m².K) is less but still considerable (from 3.3 K/W to 0.9 K/W). Increasing *h* five times (to reach 50000 W/(m²K)) reduces R_{thJA} to 0.5 K/W. Finally, when reaching 100000 W/(m².K), R_{thJA} decreases to only 0.38 K/W. From that, one can conclude that the gain achieved after certain values of *h* (50000 W/(m².K) in this case, which is also a sort of a limit to water jet impingement cooling technique based on the literature survey in chapter 2) could be unnecessary given the added cost and complexity by the heat extraction cooling technique to achieve higher values of *h*.

As presented in Figure 4.2, R_{thJA} also decreases as the copper layer thickness, *tcu*, increases. However, the gain achieved by increasing *tcu* is not as dramatic as that achieved when increasing *h*, since two conflicting effects are at play: increasing tcu reduces thermal resistance thanks to a better heat spreading, but also increase the thickness of material the heat has to go

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through. For very thick copper layers (thicker than investigated here), it is expected that R_{thJA} will increase again. Figure 4.3, Figure 4.4, and Figure 4.5 show the impact on varying heat spreader thickness, area, and thermal conductivity on R_{thJA}. In these graphs, *h* and *tcu* are set at reasonable values (10000 W/(m².K), 0.2 mm, respectively).

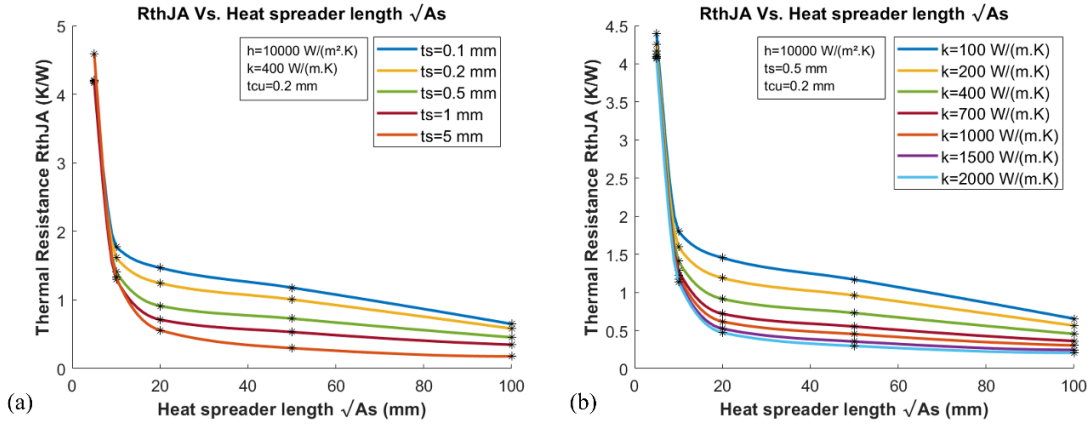

Figure 4.3: R_{thJA} against heat spreader area *As*.

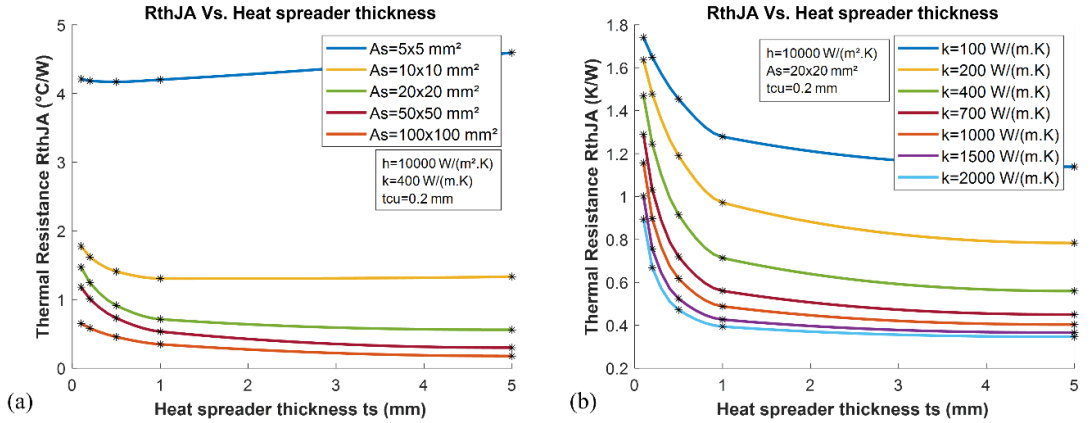

Figure 4.4: R_{thJA} against heat spreader thickness *ts*.

Increasing the heat spreading area *As* reduces R_{thJA}, but this effect starts to be less significant beyond 20×20 mm². For example, extending *As* from 20×20 mm² to 50×50 mm² decreases R_{thJA} by only 0.17 K/W (from 0.62 K/W to 0.45 K/W) compared to 0.6 K/W (from 1.22 K/W to 0.62 K/W) when extending the *As* from 10×10 mm² to 20×20 mm² at *k*=1000 W/(m.K), setting the other parameters constant (*ts*=0.5 mm, *h*=10000 W/(m².K), *tcu*=0.2 mm). This suggests that increasing the heat spreader area beyond 20×20 mm² does not offer much gain in this case.

Increasing heat spreader thickness *ts* up to 5 mm reduces R_{thJA}. At *k*=1000 W/(m.K), the reduction in R_{thJA} achieved by increasing *ts* five folds (from 1 mm to 5 mm) is only 0.09 K/W

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(from, 0.49 K/W down to 0.4 K/W) when setting the other parameters constant (*ts*=0.5 mm, *h*=10000 W/(m².K), *tcu*=0.2 mm). One can conclude that increasing the heat spreader thickness is not beneficial beyond 1 mm in this case.

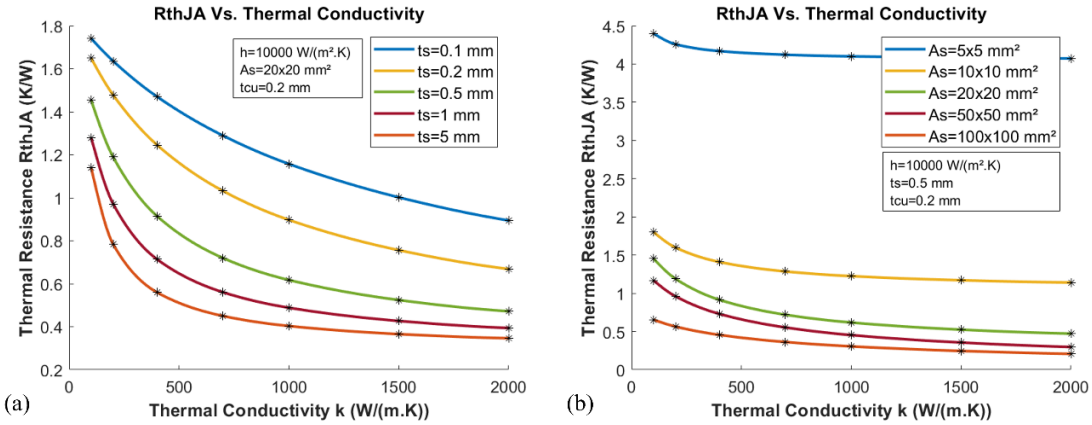

Figure 4.5: R_{thJA} against heat spreader thermal conductivity *k*.

Increasing the heat spreader thermal conductivity obviously decreases R_{thJA}. However, the gain achieved after certain value of the thermal conductivity (depending on the area and thickness) is not considerable. At a heat spreader thickness of 0.5 mm, increasing thermal conductivity from 400 W/(m.K) to 1000 W/(m.K) achieves a significant reduction in R_{thJA} of 0.3 K/W (from 0.92 K/W down to 0.62 K/W). On the other hand, the reduction of thermal resistance between 1000 W/(m.K) and 1500 W/(m.K) is 0.1 K/W (from 0.62 K/W to 0.52 K/W). Moreover, by reaching 2000 W/(m.K), R_{thJA} decreases by only 0.05 K/W (from 0.52 K/W to 0.47 K/W). This suggests a heat spreader with isotropic thermal conductivity in the range of 1000 – 1500 W/(m.K) would bring the most performance improvement.

From this parametric study, a range of values for each parameter is established in order to choose the most suitable heat spreader:

- Heat transfer coefficient (*h*) → 10000 - 50000 W/(m².K) (can be achieved by liquid cooling)
- Heat spreader area (*As*) → up to 20×20 mm²
- Heat spreader thickness (*ts*) → up to 1 mm.
- Heat spreader thermal conductivity (*k*) → 1000 - 1500 W/(m.K).

The required thermal conductivity of the heat spreader is estimated at 1000 – 1500 W/(m.K). As shown in the literature survey (chapter 2), reaching this level of thermal conductivity is

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possible by using either diamond (~2000 W/(m.K), isotropic) or pyrolytic graphite sheets (PGS) can reach a thermal conductivity higher than 1000 W/(m.K), but in the in-plane direction only because of its anisotropy. The vertical thermal conductivity of PGS is only 15 W/(m.K). PGS being much cheaper (~0.08 $/cm²) than diamond, it is the solution considered here.

As presented in the second chapter, several studies show using graphite in various ways to improve thermal performance of power modules, however, these ways are not compatible with PCB manufacturing process and embedding technology which is essential for our work. Therefore, the objective is to find out a way to embed graphite sheets in the PCB to maximize heat spreading.

4.2 Embedding graphite in a PCB

4.2.1 The concept

In PCBs, the dielectric is often an epoxy-based material with a poor thermal conductivity (< 1 W/(m.K)) compared to the copper of the conductive layer, limiting heat spreading around the die and increasing thermal resistance. To overcome this limiting point, we propose to insert graphite to take advantage of its high in-plane thermal conductivity.

Figure 4.6 shows the proposed concept of embedding graphite in a PCB stack. To overcome the low through-plane thermal conductivity of graphite, a copper pillar is connected to the heat source, distributing the heat through the graphite thickness.

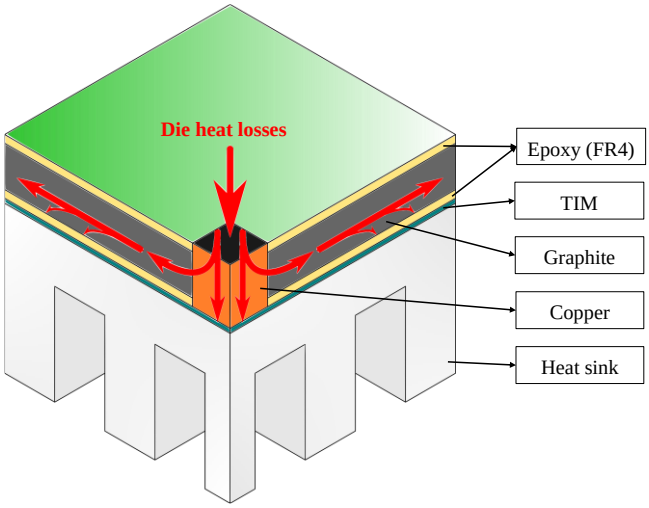

Figure 4.6: The concept of embedding graphite heat spreader in a PCB stack.

The combination of a vertical thermal path, offered by copper inserts, and a lateral one with graphite layers might result in an efficient spreading effect to extract the heat as close to the

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chip as possible and to spread the heat within the PCB before reaching the TIM of the cooling system. To apply that concept on a PCB stack, several configurations of a PCB with embedded graphite are investigated in the following, with a special attention given to manufacturability.

4.2.2 Configurations of a PCB with embedded graphite

The PCB configurations with embedded graphite have to be compatible with the classical manufacturing process of the PCB and the embedding technology. Figure 4.7 shows the manufacturing process of a PCB for die embedding.

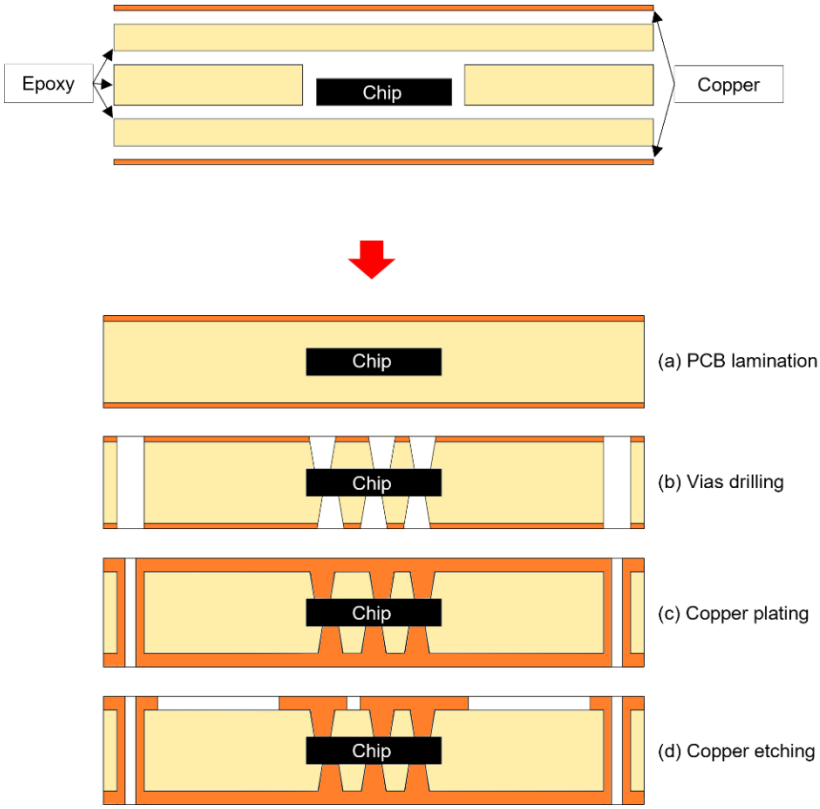

Figure 4.7: PCB manufacturing process for die embedding.

As illustrated in Figure 4.7, the PCB manufacturing process starts by stacking up conductive layers (copper) and un-cured dielectric layers (epoxy). The embedded SiC chip is placed in a cavity of an epoxy layer. After that, the stack-up is laminated resulting in a die embedded in a solid PCB. In order to interconnect the embedded chip to outer copper layers, vias are drilled by laser on both sides of the PCB package (Figure 4.7). In addition, through-hole vias are drilled mechanically to interconnect the top and bottom external copper layers. The vias are then plated with copper using an electrodeposition process. Finally, the copper layers are chemically etched to form the individual tracks needed for electrical connection copper tracks. More layers of copper can be stacked with epoxy layers in the same way to produce a multi-layer PCB.

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To improve thermal performance of power PCBs (especially those with embedded chips), it is possible to add a thick copper layer to act as a heat spreader using large mechanical vias filled with copper (Figure 4.8a). Such vias are drilled mechanically, hence the characteristic conical shape. Starting from this reference configuration, several PCB configurations with embedded graphite were suggested and considered for simulations to compare their thermal performances (examples: Figure 4.8b and Figure 4.8c).

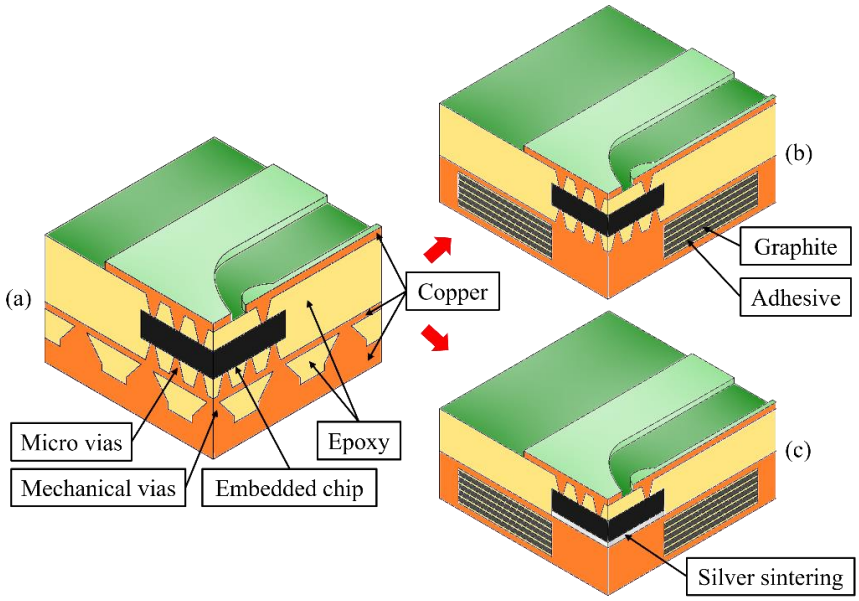

Figure 4.8: Proposed PCB configurations with embedded graphite by replacing thick copper layers and mechanical vias.

The graphite layers aim at replacing the combination of a thick copper layer and mechanical vias. Thin graphite and adhesive layers (25 µm – 100 µm each) are stacked together before PCB lamination to bond with copper and form a multi-layer graphite stack. In these example configurations, the copper pillar in the middle has to go through the graphite/adhesive stack to distribute the heat from the chip into the graphite layers. The chip is either connected by micro vias (Figure 4.8b), or attached (using sintered silver, the die-attach technique with the best thermal conductivity) directly on the copper layer (Figure 4.8c). However, these solutions require a thick copper pillar, a feature which is difficult following the classical steps of the PCB manufacturing process (whether it is the making pillar itself, ensuring good contact with the graphite, or drilling vias through it).

Figure 4.9 shows a more realistic PCB configuration allowing to embed graphite while ensuring compatibility with the PCB manufacturing process. Graphite layers are stacked together with adhesive layers during the stack-up process. Micro vias are laser-drilled through

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the graphite/adhesive stack and filled with copper to provide the chip with electrical connections as well as offering a low thermal resistance vertical path for the dissipated heat. In this configuration, micro vias replace the copper pillar, so the density of micro vias should be sufficient to transfer the dissipated heat from the chip into graphite with low thermal resistance.

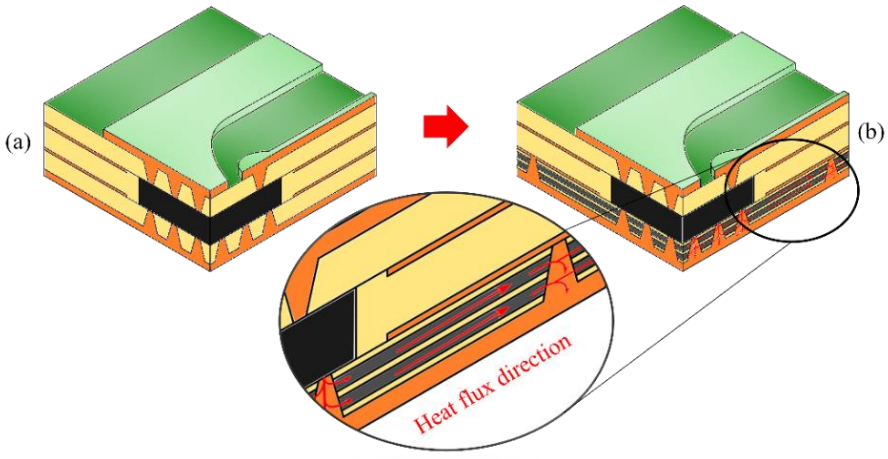

Figure 4.9: The chosen PCB configuration with embedded graphite.

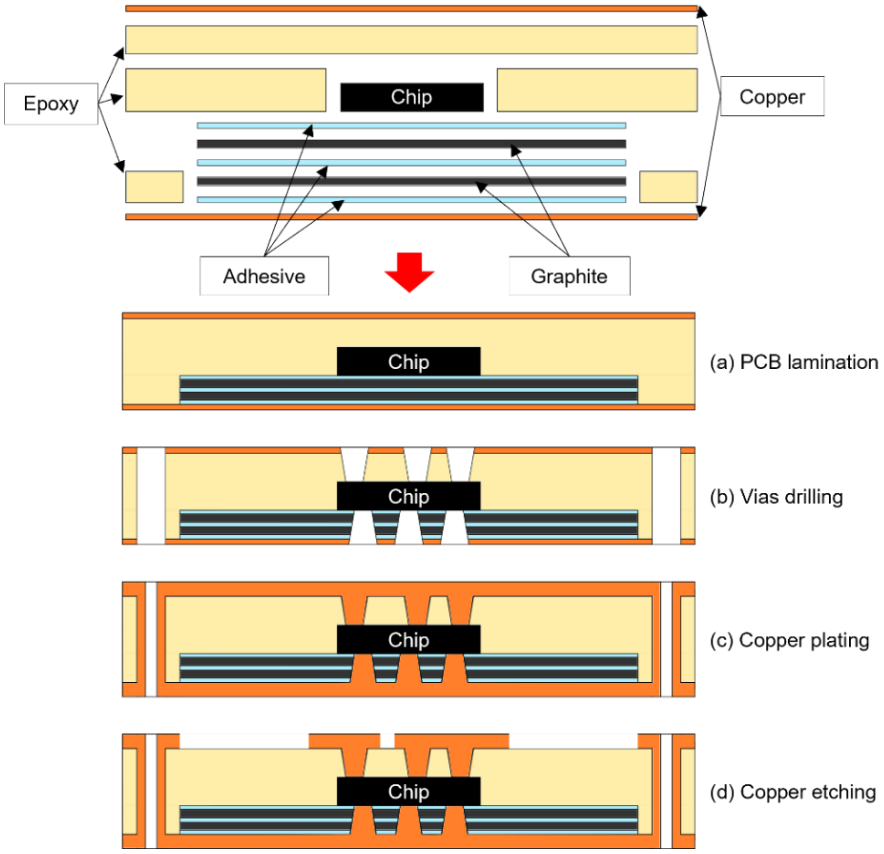

Figure 4.10: The manufacturing process of the PCB package with embedded graphite/adhesive.

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Figure 4.10 shows the manufacturing steps of such a PCB with embedded chip and graphite layers. In order to initially verify the concept of embedding graphite in a PCB and the copper adhesion within the via hole during electrodeposition, a small-scale in-house fabrication of a simple PCB stack is performed (this stack does not include any chip nor any micro-via). The stack is composed of several pyrolytic graphite sheets (PGS: Panasonic EYG-S091210) of 100 µm thickness stacked together with FR4 epoxy sheets (Isola PCL-FR-370HR) with a thickness of 38 µm after lamination. These are laminated with two copper layers (35 µm) on top and bottom. Mechanical vias are drilled through the stack and plated with copper.

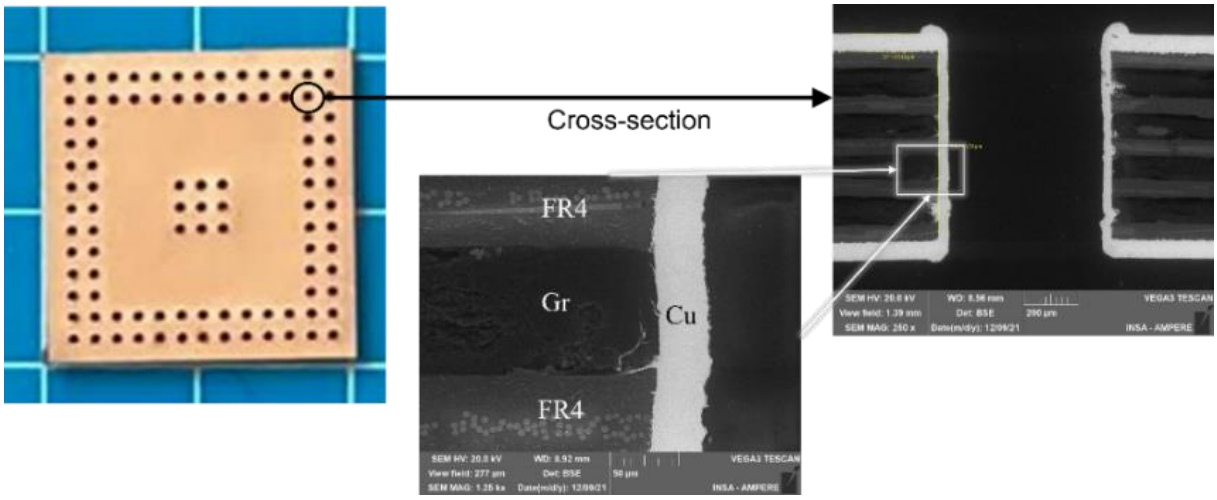

Figure 4.11: Photograph of a simple PCB (20×20 mm²) including a 4-layer graphite stack (left). Microscopic images of a cross-section (center and right), showing the good interface quality between graphite, FR4 and copper.

Figure 4.11: Photograph of a simple PCB (20×20 mm²) including a 4-layer graphite stack (left). Microscopic images of a cross-section (center and right), showing the good interface quality between graphite, FR4 and copper. shows a cross-section of one of the mechanical vias, which demonstrate a good contact between the graphite sheets and the copper (no voids or cracks at the interface), which is a key point for that concept to work properly. Also, the FR4 layers provide the adhesion necessary between graphite sheets, and the FR4/graphite interfaces are also found to be of good quality.

4.2.3 Optimization of the graphite heat spreader

The optimization step consists in calculating the equivalent thermal conductivity of the possible graphite/adhesive/copper vias combinations to choose the most suitable thicknesses and number for each of the layers as well as the density and the diameter of the micro vias

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(taking into account the technical capability of the manufacturer). Because many configurations have to be investigated, the analytical model described previously is used at this stage.

4.2.3.1 The choice graphite and adhesive layers

The equivalent vertical and lateral thermal conductivity of the graphite/adhesive stack is estimated for a range of PGS sheets (commercially available from Panasonic) with different thicknesses and lateral thermal conductivities (the vertical thermal conductivity is constant) [122]. In addition, the influence of the number of PGS sheets is investigated. Table 4.2 presents the thicknesses of PGS sheets and the corresponding thermal conductivities.

Table 4.2: PGS sheet thicknesses and the corresponding thermal conductivities [122].

PGS	Thickness (µm)	k_{xy} (W/(m.K))	k_z (W/(m.K))
Panasonic EYG-S091201	10	1950	15
Panasonic EYG-S091202	17	1850	15
Panasonic EYG-S091203	25	1600	15
Panasonic EYG-S091204	40	1350	15
Panasonic EYG-S091205	50	1300	15
Panasonic EYG-S091207	70	1000	15
Panasonic EYG-S091210	100	700	15

The thickness of the adhesive layer is varied (up to 100 µm) to determine its impact on the equivalent thermal conductivity. Its thermal conductivity is assumed here to be constant at 0.3 W/(m.K) which is a classical value for a dielectric used in PCBs.

Figure 4.12 shows the estimation of the vertical and lateral equivalent thermal conductivity of the graphite/adhesive stack in terms of the number of PGS sheets in the stack for several PGS types (with adhesive layer thickness = 25 µm, the thinnest value commercially available). As shown in the figure, stacking more PGS sheets increases the equivalent lateral thermal conductivity. However, there is no more significant gain beyond 5 PGS sheets. For the vertical equivalent thermal conductivity keq_z of the graphite/adhesive stack, the higher the thickness of the PGS, the higher keq_z since all the PGS have the same vertical thermal conductivity (k_z=15 W/(m.K)). On the other hand, for the lateral thermal conductivity keq_{xy}, the PGS sheets with a thickness of 50 µm (k_{xy} = 1300 W/(m.K)) shows the highest value.

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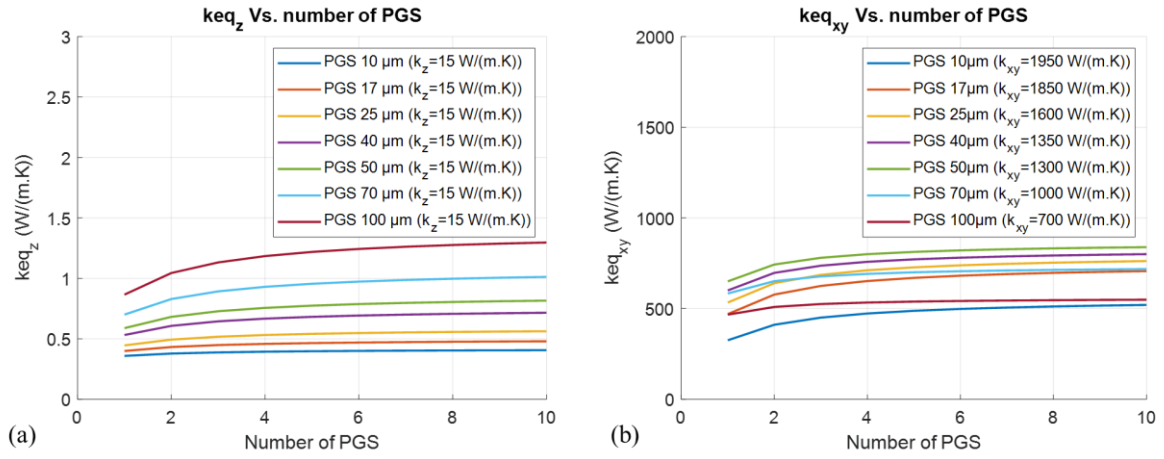

Figure 4.12: The equivalent thermal conductivity of the graphite/adhesive stack against the number of PGS sheets (assuming 25 µm adhesive thickness).

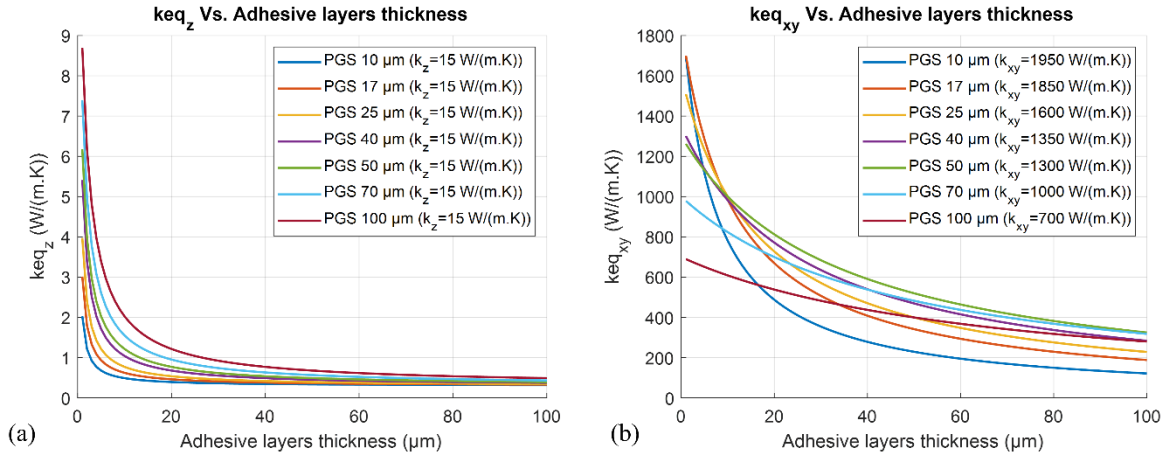

Figure 4.13: The equivalent thermal conductivity of the graphite/adhesive stack against the thickness of the adhesive layers (assuming two PGS sheets)

While 5 layers appear to be a good trade-off between performance and stack complexity, a discussion with the PCB manufacturer exhibits difficulties and risks regarding the drilling of the micro vias in a thick, heterogeneous stack. In consequence, a simpler structure, with only 2 PGS sheets is considered for the prototypes

Figure 4.13 shows the equivalent thermal conductivity of the graphite/adhesive stack (with two PGS and three adhesive layers) against the adhesive layer thickness. Generally, the thinner the adhesive layers, the higher the equivalent thermal conductivity. For keq_z, higher ratios of PGS/adhesive thicknesses results in higher conductivities keq_z. The situation is more complex for the in-plane conductivity: for very small thickness of adhesive layers (less than 10 µm), the PGSs of 10 µm and 17 µm (with k_{xy} = 1950 W/(m.K) and k_{xy} = 1850 W/(m.K) respectively)

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achieve a higher keq_{xy}. However, for adhesive layer thicker than 10 µm, the PGS material of 50 µm (k_{xy} = 1300 W/(m.K)) reaches a higher keq_{xy}. From previous results, the PGS of 50 µm (k_{xy} = 1300 W/(m.K) and k_z = 15 W/(m.K)) is chosen (Panasonic EYGS091205). Two PGS sheets of 50 µm are chosen to be stacked with three adhesive layers of 25 µm (the total thickness of the graphite/adhesive stack is 175 µm). The adhesive layer must be as thin as possible. The thinnest commercial product we could find is an acrylic-based adhesive layer of 25 µm is chosen (DuPont Pyralux LF0100 [123]) with a thermal conductivity of 0.22 W/(m.K) which will slightly degrade the equivalent vertical thermal conductivity compared to the 0.3 W/(m.K) considered in the optimization procedure.

For the chosen graphite/adhesive stack, the equivalent thermal conductivity is estimated to be: $keq_{xy} = 743\ W/(m.K)$ and $keq_z = 0.5\ W/(m.K)$.

4.2.3.2 The choice of micro vias dimensions

The limit set by the manufacturer for the thickness/diameter ratio of a micro via is less than 0.9. (to ensure the micro via is properly filled with copper). The laser drilling is applied through a stack of graphite adhesive of 175 µm plus a copper layer of 17 µm (total thickness of 192 µm). By choosing micro vias with a diameter of 240 µm, the thickness/diameter ratio is 0.8 (< 0.9 limit). Therefore, the diameter of the micro vias is chosen to be 240 µm based on the manufacturer capability for the laser drilling.

In our proposed stack with graphite, a high density of micro vias is needed in the area under the chip (ideally, the vias would touch each other to form a solid copper pillar), to provide a high equivalent vertical thermal conductivity. This is important because the heat dissipated by the chip must be distributed to the two PGS sheet before it is spread laterally through graphite. Figure 4.14 shows the impact of the spacing between the edges of the micro vias on the equivalent thermal conductivity (of the volume of graphite/adhesive/microvias situated just inder the chip). keq_z increases for smaller spacings between the micro vias (coppers becomes dominant), while keq_{xy} increases by increasing the spacing between the micro vias (graphite becomes dominant).

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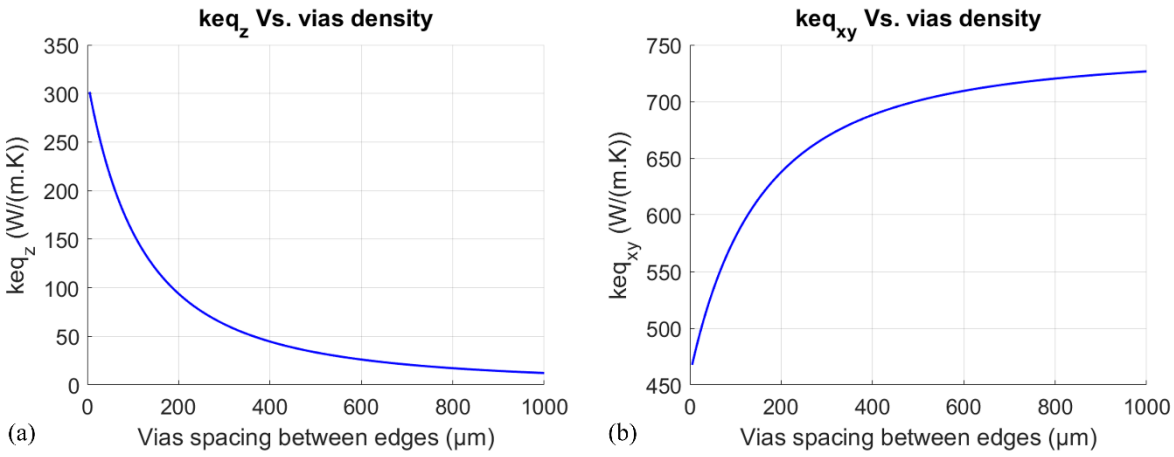

Figure 4.14: The equivalent thermal conductivity of the graphite/adhesive stack with copper vias against the density of vias.

Based on the laser drilling capability of the manufacturer, the smaller spacing between the edges of the micro vias that can be applicable is 150 µm (smaller than that is desirable but not applicable). Therefore, the equivalent thermal conductivity of a region of graphite/adhesive stack with micro vias (on the bottom side of the chip) is estimated to be: $keq_{xy} = 614\ W/(m.K)$ and $keq_z = 119\ W/(m.K)$.

4.2.4 PCB variants

Several PCB samples with different sizes and micro vias patterns are designed. Three sizes are considered for the embedded graphite pads: 20×20 mm², 10×10 mm² (for single-chip samples) and 20×30 mm² (for double-chip samples only). This is to show the impact of the heat spreading area through graphite.

One series of PCB samples embeds SiC diode chips, while the other embeds SiC MOSFET chips. While no major difference is expected between both variants from a thermal point of view (Diode chip size is 3.1×2.86×0.24 mm^3 and MOSFET chip size is 3.36×3.1×0.21 mm^3), the two variants aim at evaluating the manufacturability. In particular, the gate contact of the MOSFETs is very small (0.5×0.8 mm²), and requires very good alignment. On the contrary, the diode has a large anode contact, maximizing the chances of succeeding in manufacturing the samples.

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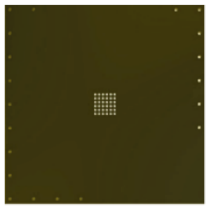
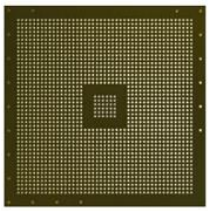
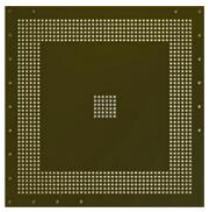
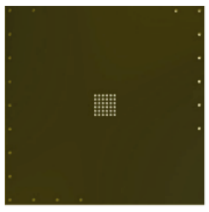
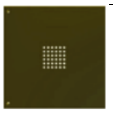
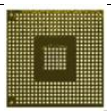
Table 4.3: The characteristics of all PCB variants.

Diode samples	MOSFET samples	Spreading area	Graphite	Vias pattern
D22R	M22R	20x20 mm²	No	
D22Ga	M22Ga	20x20 mm²	Yes	
D22Gb	M22Gb	20x20 mm²	Yes	
D22Gc	M22Gc	20x20 mm²	Yes	
D11R	M11R	10x10 mm²	No	
D11Ga	M11Ga	10x10 mm²	Yes	
2D23R	-	20x30 mm²	No	
2D23Gc	-	20x30 mm²	Yes	

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Since the copper micro vias through graphite/adhesive stack increases the equivalent vertical thermal conductivity, three patterns of micro vias distribution in the spreading area are considered: micro vias distributed over all the spreading area, micro vias distributed on the periphery of the spreading area, and no micro vias in the spreading area. For all variants, micro vias are drilled in the area under the chip, as they are essential to transfer the heat into graphite as well as for electrical connections. Considering the size of the chips, a 6×6 micro vias matrix is with 150 µm spacing between the edges of the micro vias. The hole-diameter of micro-vias is 240 µm.

In addition, another variant embeds two diodes to study the effect of graphite on thermal coupling from chip to chip. Table 4.3 shows the characteristics of the PCB variants as well as micro vias patterns on the bottom side of the PCB variants.

4.2.5 PCB layout design

The PCB variants are designed using Altium Designer, which is an electronics computer-aided design (ECAD) software. The schematic of the electronic circuit is first established. Next, the structure of the PCB is specified including each layer (type, thickness, etc.) and the characteristics of the vias (diameter, spacing, etc.). In addition, electrical isolation constraints are specified to allow for automatic validation of the design rules (1200V-rated chips are used, and their blocking voltage capability must be maintained once embedded). Then the actual layout of the PCB (drawing of the geometrical features of each layer) can be performed. Finally, Altium Designer can export the files (Gerber) required by the manufacturer to produce the samples.

While the samples containing diodes and MOSFETs chips have a similar structure (same spreader size, via patterns on the back, etc.) they differ by their electrical connections on the top of the PCB. A diode has two electrical terminals: anode and cathode. On the other hand, a MOSFET has three terminals: source, drain, and gate. The MOSFET controls how much current can flow between its source and drain terminals depending on how much voltage is applied to its gate terminal. The electrical isolation gap must be of 3.5 mm where the voltage difference can be large (between anode and cathode, source and drain, drain and gate). Where the voltage difference is limited to a few volts (between gate and source, a much shorter minimum distance of 175 µm is allowed.

Some connectors are mounted on the top surface of the PCB: high current (50 A) connectors to inject power through the anode and cathode or Source and Drain (A and C in diode PCB, S

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and D in MOSFET PCB); sensing connectors for voltage monitoring (Ka and Kc in diode PCB, Ks and Kd in MOSFET PCB) or driving the MOSFETs (Kg). Figure 4.15, Figure 4.16, Figure 4.17, Figure 4.18, and Figure 4.19 show the circuit and layout of the different PCB samples.

Because all the electrical connections are located on top of the PCB (the bottom surface being dedicated to cooling), copper vias are needed to bring the cathode or drain potential from the bottom copper layer to the top layer. Mechanical vias with a 300 µm hole diameter and 80 µm copper plating thickness are used. Such vias are estimated to accept a maximum current of 4.95 A each. The number of mechanical vias are chosen to be able to carry a current of 30 A. All single-chip samples have a total dimension of 46×46 mm², the chip being located in the center, aligned with the 20×20 or 10×10 mm² graphite pads. The larger sample size is chosen to host the connectors and allow for mechanical clamping of the samples during testing.

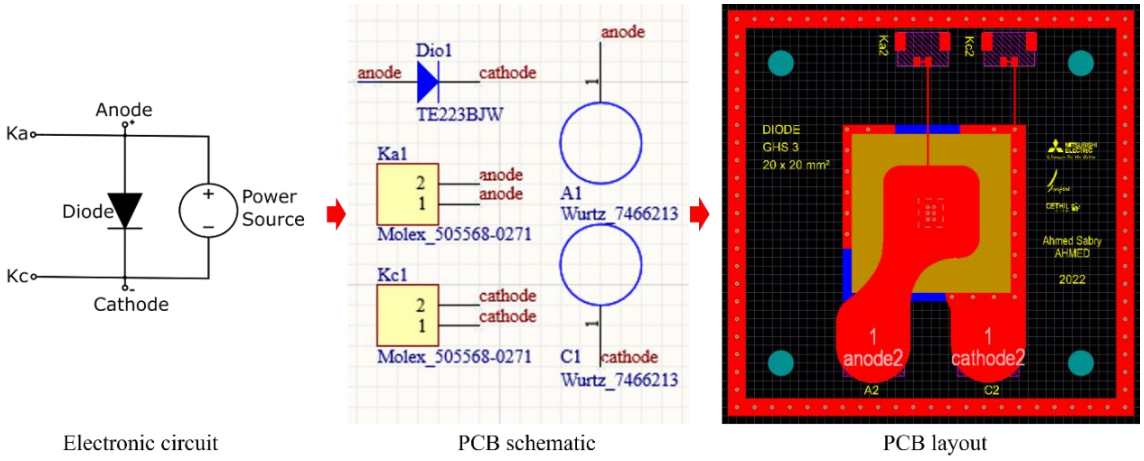

Figure 4.15: The electronic circuit and the layout of a diode PCB of 20×20 graphite size.

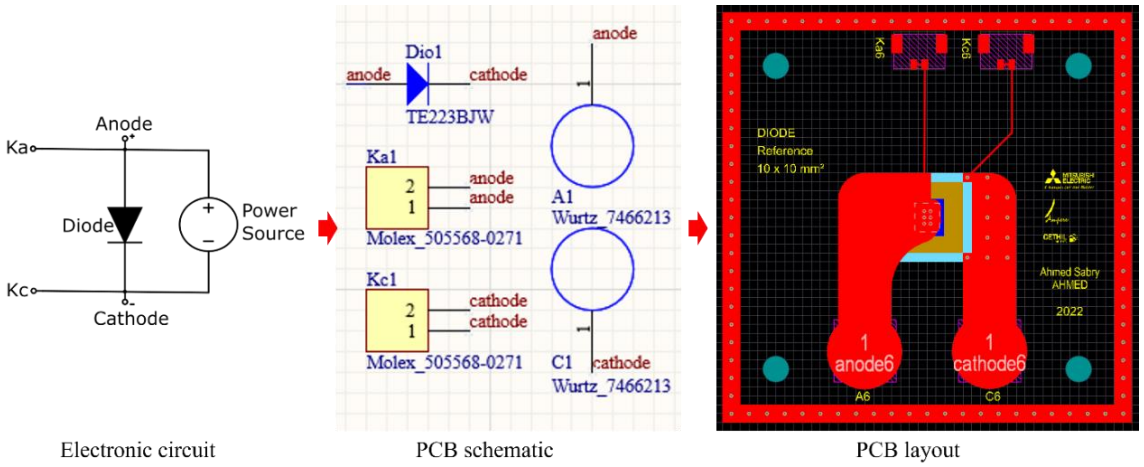

Figure 4.16: The electronic circuit and the layout of a diode PCB of 10×10 graphite size.

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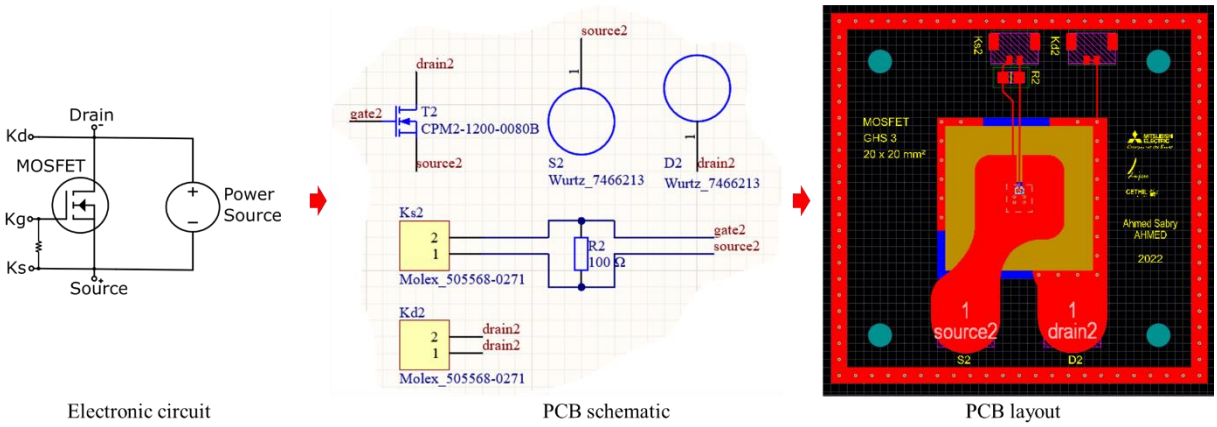

Figure 4.17: The electronic circuit and the layout of a MOSFET PCB of 20×20 graphite size.

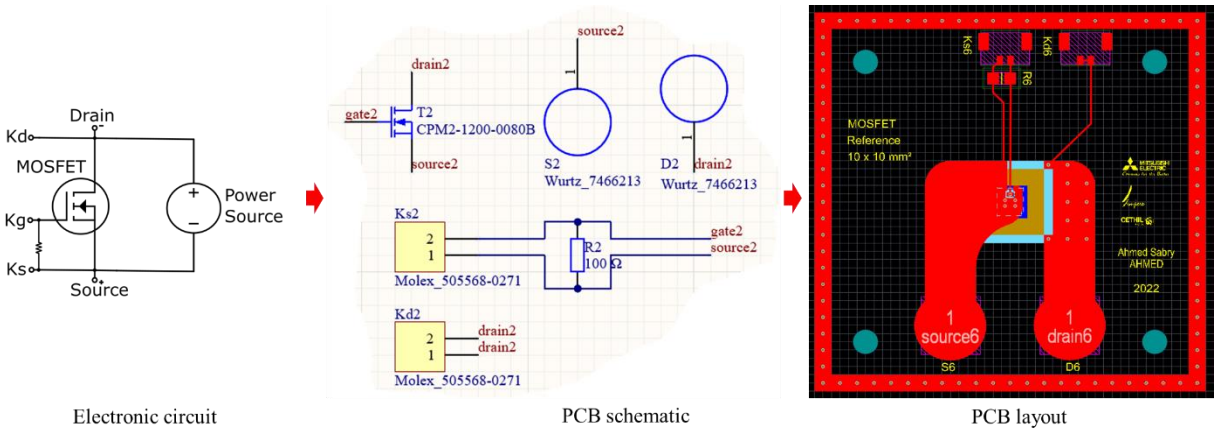

Figure 4.18: The electronic circuit and the layout of a MOSFET PCB of 10×10 graphite size.

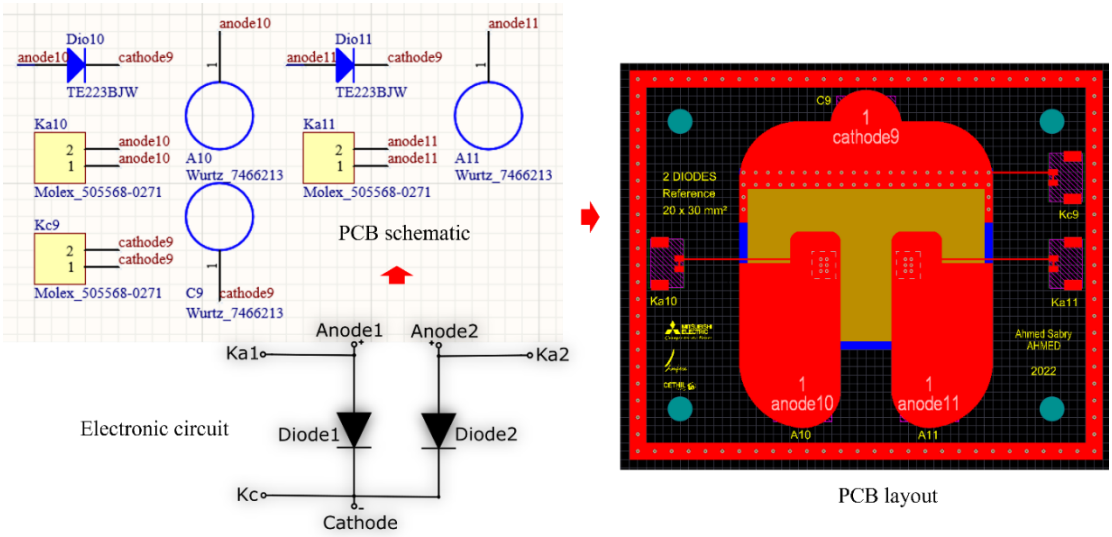

Figure 4.19: The electronic circuit and the layout of a dual-diodes PCB of 20x30 graphite size.

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Figure 4.20 shows the layout of the PCB panel of all the variants (with embedded diodes and MOSFETs) designed using Altium Designer.

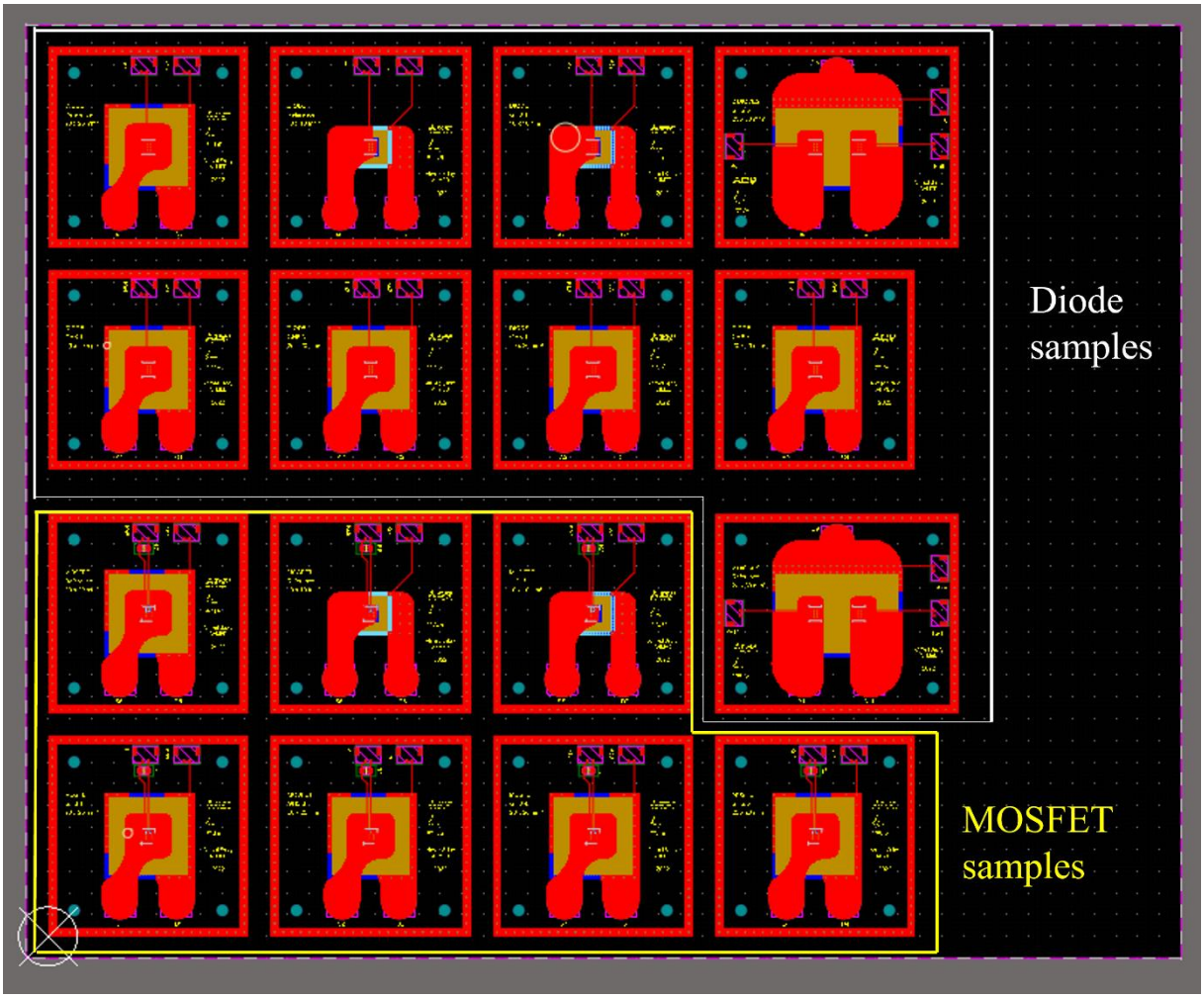

Figure 4.20: The layout of a PCB panel with all the variants.

4.2.6 Modelling

Thermal numerical simulations are performed using the finite element method (FEM) on ANSYS Mechanical. By taking advantage of the symmetry, only one quarter of the active part (the 10×10 mm² or 20×20mm² area containing graphite) of the single-diode PCB samples is considered to limit computational time (Figure 4.21) without affecting simulation results. For the double-diode part, half of the structure is considered instead of a quarter (Figure 4.22). The top and bottom copper layers are not exactly symmetrical because of the differences in the electrical connections.

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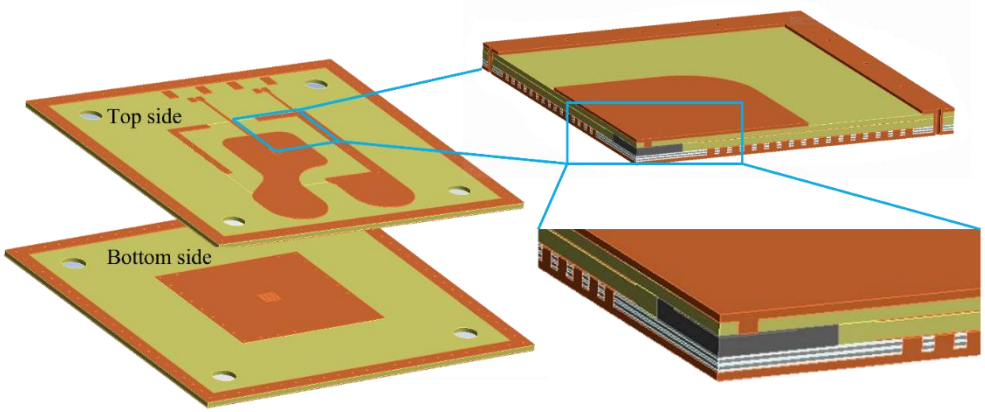

Figure 4.21: CAD model of the single-chip PCB showing the quarter model considered for simulations.

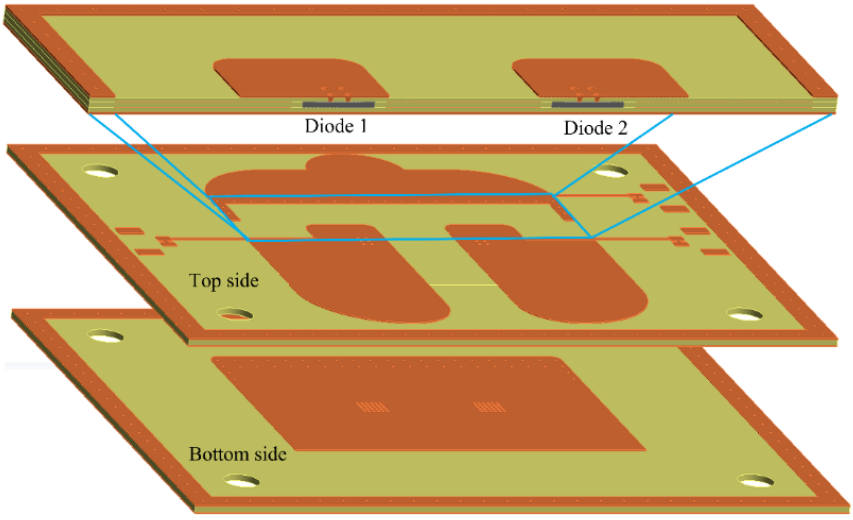

Figure 4.22: CAD model of the dual-chips PCB showing the half model considered for simulations.

The boundary conditions are set according to the experimental measurements. A heat transfer coefficient (h) is used at the backside of the PCB to represent the cooling of the TIM and the cold plate. Since this heat transfer coefficient is unknown, h is adjusted in the simulations so as to achieve the same R_{thJA} value as the experiment of the reference samples without graphite (D22R and D11R). The value of h for which the simulations are found to correspond to the experimental results of the reference sample is 6000 W/(m² K. For 10×10 mm² reference sample, this h value is found to be 9000 W/(m².K) This larger value is probably due to the relatively larger copper pad on the bottom side that is necessary for electrical connections (the bottom copper pad has the size of the graphite pads (in orange in Figure 4.21) plus a margin for the mechanical vias (in blue)).

R_{thJC} is calculated in a way which mimics the TDIM method: two transient thermal simulations are performed for each sample, with two different values for h: 6000 W/(m².K) and

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36000 W/(m².K), representing respectively TIMs which are used in measurements (thermal pad and deionized water TIMs respectively). For the 10×10 mm² PCB samples, the values of *h* are: 9000 W/(m².K) and 40000 W/(m².K). These values of *h* are obtained so that the simulations of the reference samples achieve the same results as the measurements with thermal pad and deionized water TIMs. The processing method described in JEDEC51-14 (calculation of the derivative of the difference between both Z_{th} curves, threshold detection) is then applied. This allows us not to make any assumption on the temperature distribution on the backside of the samples, and yields a R_{thJC} value which is fully consistent with the measurement method. Table 4.4 shows the boundary conditions applied in simulations in order to obtain R_{thJA} and R_{thJC}.

Table 4.4: Boundary conditions of the simulations to obtain *RthJA* and *RthJC*.

Location	Type	Value
SiC chip (3.1×2.86)	Internal heat generation	16 W
PCB top	Heat transfer coefficient	10 W/(m².K)
PCB bottom (20x20 mm² & 20x30 mm²)	Heat transfer coefficient	6000 W/(m².K) Or 36000 W/(m².K)
PCB bottom (10x10 mm²)	Heat transfer coefficient	9000 W/(m².K) Or 40000 W/(m².K)

4.2.7 Simulation results and discussion

4.2.7.1 Single-diode PCB variants

Two parameters are compared here: Junction-to ambient thermal resistance (R_{thJA}, the steady-state value of Z_{th}) and junction-to-case thermal resistance (R_{thJC}, obtained using the TDIM method). Samples with graphite are compared to reference samples (without graphite) of the same size. For the simulations, the maximum T_j (i.e. the highest temperature value at the surface of the chip) is used as the chip temperature in the calculations. Figure 4.23 and Figure 4.24 show the temperature distribution in various PCB configurations (reference, distributed vias, vias on the periphery and no distributed vias) when applying 16 W power loss. For the 20×20 mm² PCB variants, the maximum T_j drops from 90.3°C in D22R down to 55.4°C in D22Ga due to the better heat spreading achieved by graphite. The distribution of micro vias in D22Ga reduces the maximum T_j by 1.8°C only when compared to D22Gc. On the other hand,

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10×10 mm² PCB variants, the maximum temperature is reduced to 61.7°C in D11Ga down from 90.4°C in D11R.

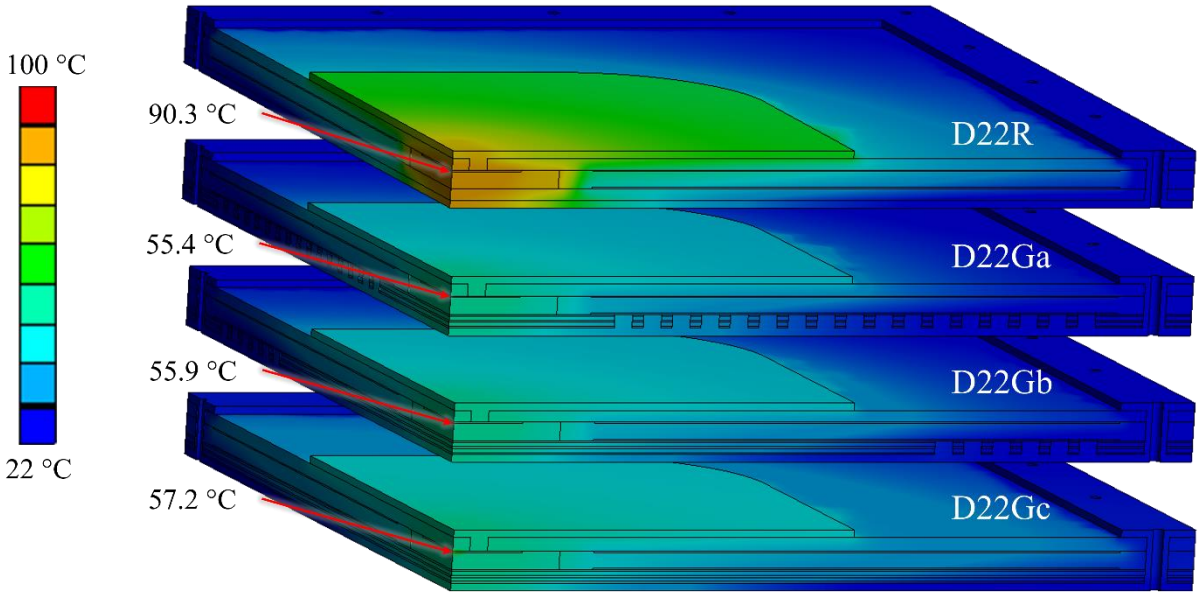

Figure 4.23: Temperature contours of the 20×20 mm² PCB variants model showing the impact of embedding graphite on the maximum junction temperature (micro vias under the chip do not appear here due to cross section location).

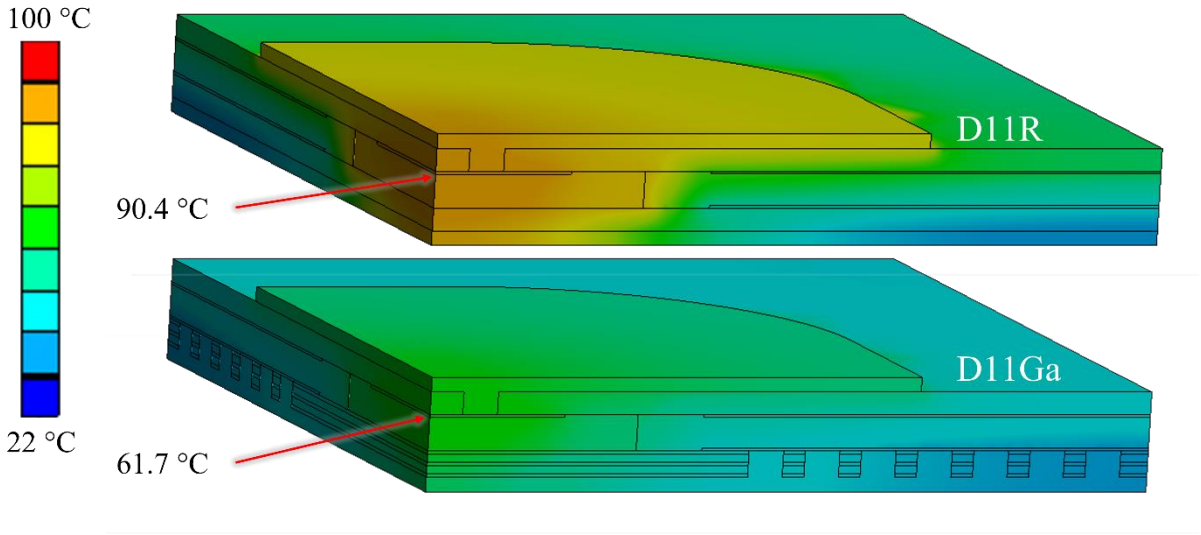

Figure 4.24: Temperature contours of the 10×10 mm² PCB variants model showing the impact of embedding graphite on the maximum junction temperature (micro vias under the chip do not appear here due to cross section location).

Figure 4.25 shows the thermal impedance curves and the R_{thJA} values for all the single-diode PCB variants of obtained by FEM transient thermal simulations. The influence of embedding

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graphite is obvious. Up to 51 % reduction in R_{thJA} is achieved in 20×20 mm² PCB variants (from 4.27 K/W in D22R down to 2.1 K/W in D22Ga or D22Gb). Moreover, increasing the micro-vias density (layout Ga or Gb) reduces R_{thJA} by about 2.5 % compared to Gc layout without distributed micro vias (2.1 K/W compared to 2.2 K/W). Regarding the 10×10 mm² PCB variants (D11R and D11Ga), the R_{thJA} is reduced by 42.1 % (from 4.28 K/W in D11R to 2.48 K/W in D11Ga).

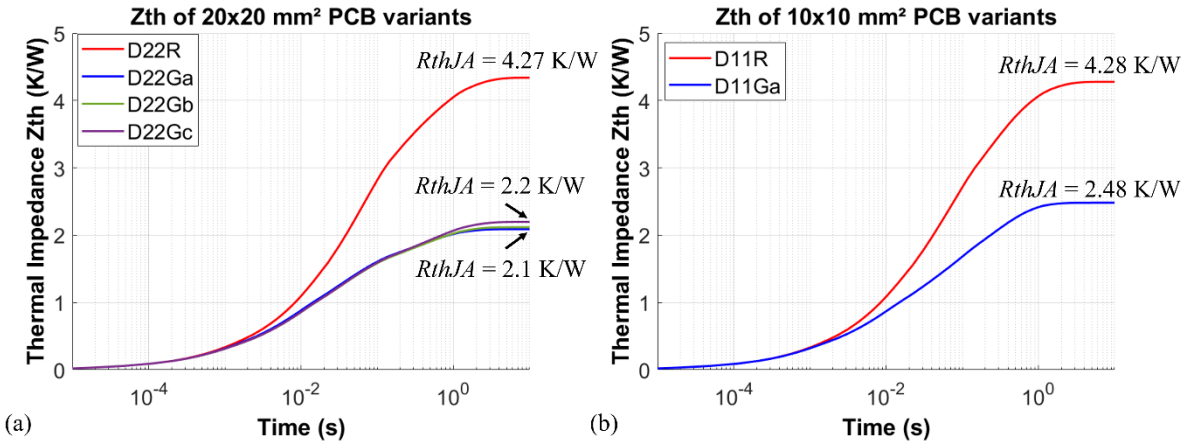

Figure 4.25: Thermal impedance curves for all PCB variants showing the impact of embedding graphite on the R_{thJA} (FEM simulations).

The effect of heat spreading due to graphite can be seen when comparing D22Ga with D11Ga (graphite sheet sizes of 20×20 mm², 10×10 mm², respectively) with an increase in R_{thJA} of about 18.7 % in simulations (2.09 K/W, 2.48 K/W, respectively). However, even the relatively modest area offered by the 10×10 mm² variant (a quarter of the area of the 20×20 mm² samples) already has a dramatic spreading effect compared with the reference PCB variant (42.1% reduction in R_{thJA}). That means that even a 10×10 mm² graphite heat spreader can be sufficient for some applications, and that increasing the graphite area further may only yield moderate gains.

Regarding R_{thJC}, the values are calculated using the TDIM calculation procedure described in JEDEC51-14 standard for the various PCB variants as illustrate in 3.4.2.2. For each sample, two thermal impedance curves are obtained by applying two heat transfer coefficient values at the bottom side of the PCB (as illustrated in 4.2.6). According to the simulations, the PCB variants with graphite achieve around 25 % reduction in R_{thJC} compared to the reference sample (Figure 4.26). For the 10×10 mm² samples, the reduction is more modest, 11 % for D11Ga with respect to the reference sample D11R (Figure 4.27).

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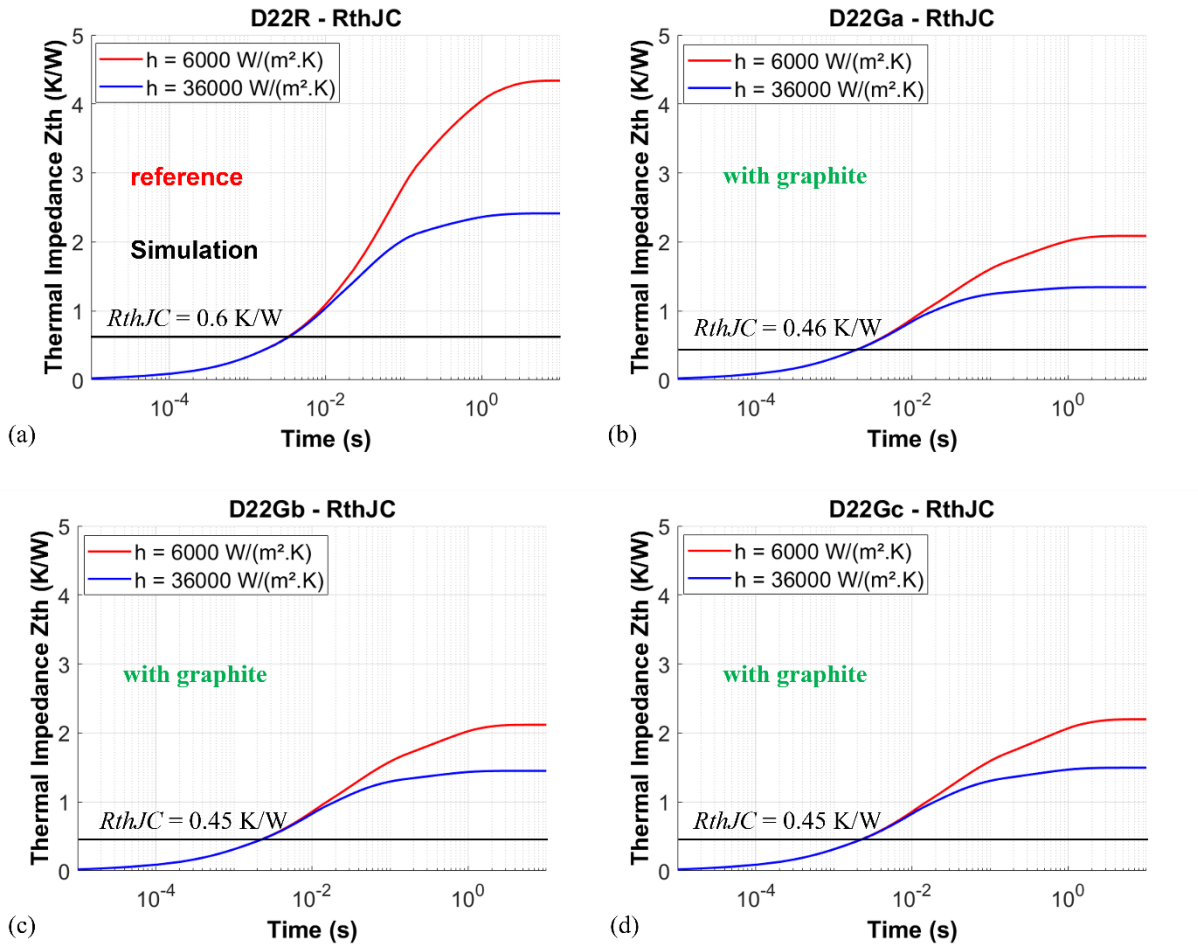

Figure 4.26: Thermal impedance curves for the 20×20 PCB variants with different *h* at the bottom side boundary and the calculated R_{thJC} at the separation point (FEM simulations).

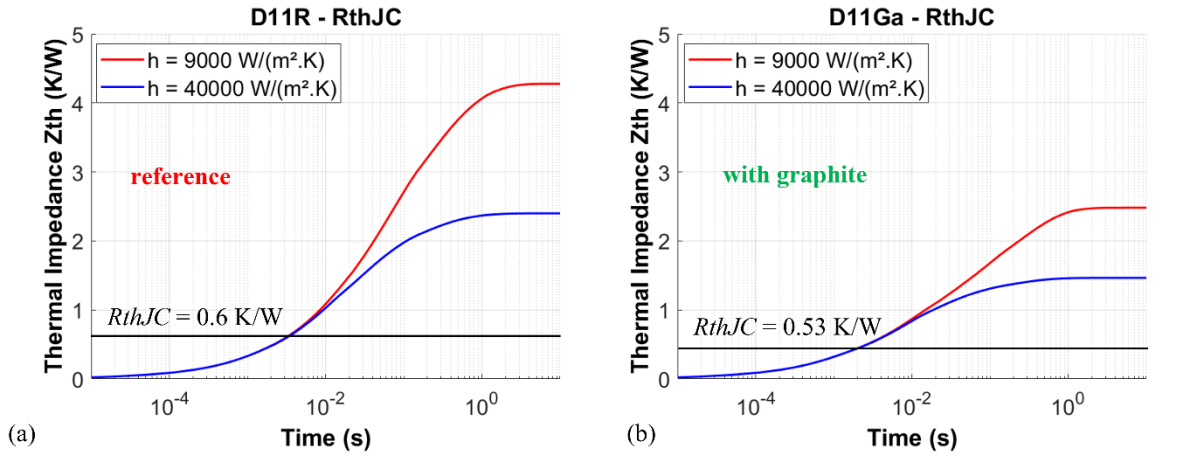

Figure 4.27: Thermal impedance curves for the 10×10 PCB variants with different *h* at the bottom side boundary and the calculated R_{thJC} at the separation point (FEM simulations).

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Table 4.5 shows a comparison between all the PCB variants in terms of R_{thJA} and R_{thJC} values and the reduction achieved compared to the reference PCB variants.

Table 4.5: Comparison between all PCB variants in terms of R_{thJA} and R_{thJC} (FEM simulations).

PCB variant	**R_{thJA} (K/W)**	**Reduction in R_{thJA}**	**R_{thJC} (K/W)**	**Reduction in R_{thJC}**
D22R	4.27	REF	0.6	REF
D22Ga	2.09	– 51 %	0.46	– 23.3 %
D22Gb	2.12	– 50.4 %	0.45	– 25 %
D22Gc	2.2	– 48.5 %	0.45	– 25 %
D11R	4.28	REF	0.6	REF
D11Ga	2.48	– 42.1 %	0.53	– 11.7 %

The limited reduction in R_{thJC} compared to R_{thJA} raise the question of the suitability of TDIM method described in JEDEC51-14 standard. One would expect that all the reduction in R_{thJA} is due to lower R_{thJC} (and therefore expect a 60-80 % reduction in R_{thJC}). However, the opposite is observed. This can be attributed to the definition of R_{thJC}, which assumes one-directional distribution of the heat between two isothermal surfaces. These assumptions tend to be not valid the more the heat is spread in the package in all directions. TDIM for R_{thJC} calculations assumes an undistributed heat flow from the die junction to the back side case of the PCB package. However, different TIMs (i.e. different heat-exchange coefficients on the backside of the sample) probably result in change of heat fluxes within the heat spreader, and therefore a change in the heat distribution and path in spreading within the PCB results in changes in the heat flow inside the package, something which is not expected in the assumptions of the R_{thJC} calculations by TDIM.

4.2.7.2 Double-diode PCB variants

The PCB variants with two embedded diodes are designed to study the influence of the graphite on the thermal coupling between the two diodes. Figure 4.29 show the impact of em bedding graphite on the maximum junction temperature in a dual-diodes PCB stack when applying 16 W power loss on the first diode (D1) only and leaving the second diode (D2) without assigning power loss. The maximum T_j of D1 drops from 94.5°C in 2D23R down to 57.5°C in 2D23Gc due to the better heat spreading achieved by graphite. At the same time, the

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T_j of D2 increases by 2.8°C (from 23.3°C in 2D23R to 26.1°C in 2D23Gc) due to the increase in the thermal coupling between the two diodes caused by graphite.

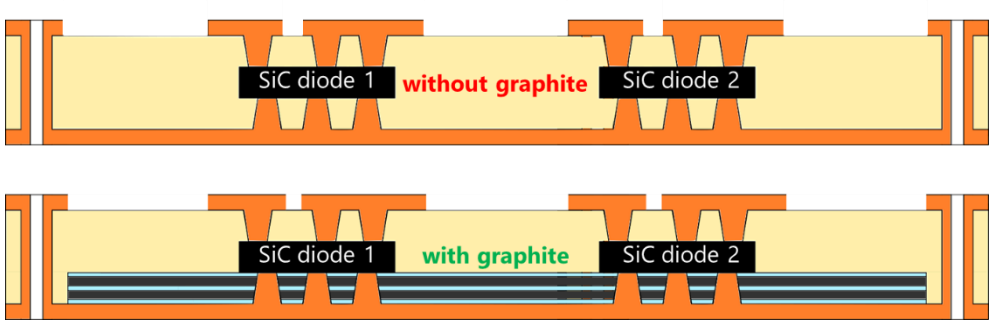

Figure 4.28: PCB variants with two embedded diodes.

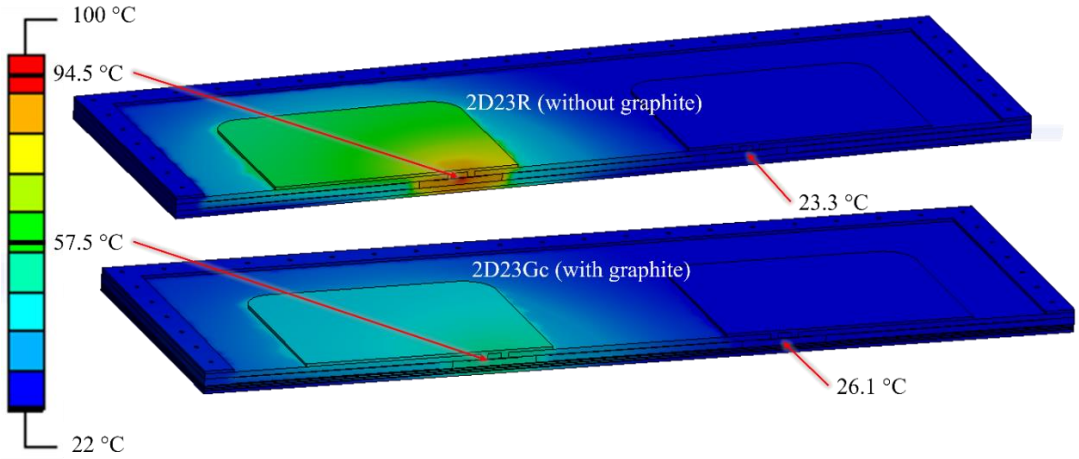

Figure 4.29: Temperature contours of the dual-diodes PCB variant model showing the impact of embedding graphite on the junction temperatures of the diodes.

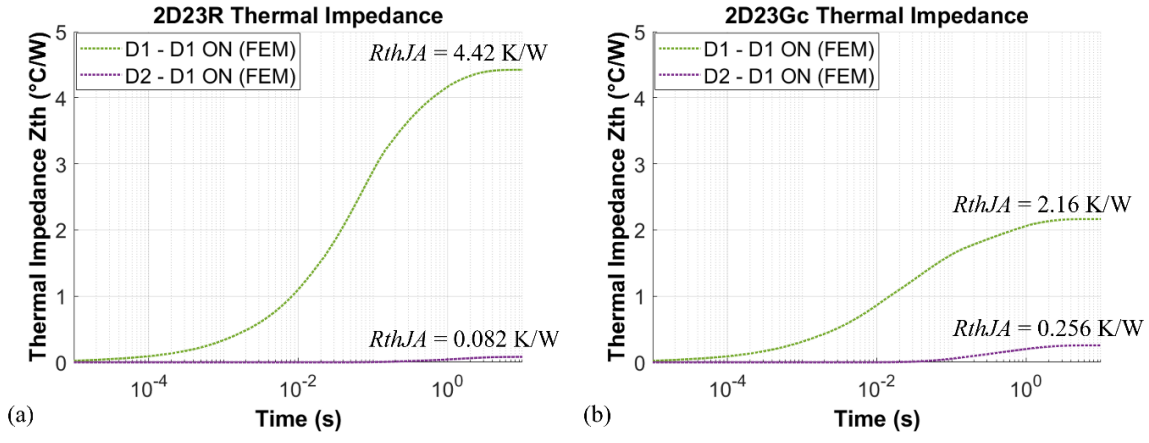

Figure 4.30: Thermal impedance curves for dual-diodes PCB variants showing the impact of embedding graphite on the R_{thJA} and the thermal coupling (FEM simulations).

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Figure 4.30 shows the thermal impedance curves of the two diodes obtained by transient thermal FEM simulations of the PCB with graphite (b) compared to the reference PCB without graphite (a). The 16 W power loss is applied to the first diode only. The R_{thJA} of the first diode is reduced by 51 % (from 4.42 K/W in 2D23R to 2.15 K/W in 2D23Gc). Concerning the second diode, the R_{thJA} is increased from 0.082 K/W in 2D23R to 0.256 K/W in 2D23Gc.

Table 4.6 compares the percentage of the thermal coupling in 2D23R reference PCB variant and 2D23Gc PCB variant with graphite and shows a 6-fold increase in thermal coupling by (from 1.85 % in 2D23R to 11.85 % in 2D23Gc) due to graphite heat spreading effect.

The graphite heat spreader not only results a significant reduction in R_{thJA}, but also in an increase in the thermal coupling between the two diodes. The thermal coupling percentage can be defined by the following equations:

$$Thermal\ coupling\ \% = 100 \times \frac{R_{thJA-D2-OFF}}{R_{thJA-D1-ON}}$$

Where $R_{thJA\text{-}D1\text{-}ON}$ is the R_{thJA} of the first diode while dissipating heat (ON) and $R_{thJA\text{-}D2\text{-}OFF}$ is the R_{thJA} of the second diode with no heat dissipation (OFF).

Table 4.6: Comparison of the *RthJA* and the thermal coupling percentage of 2D23R and 2D23Gc PCB variants (FEM simulations).

PCB variant	$R_{thJA\text{-}D1\text{-}ON}$ **(K/W)**	$R_{thJA\text{-}D2\text{-}OFF}$ **(K/W)**	**Thermal coupling %**
2D23R	4.42	0.082	1.85 %
2D23Gc	2.16	0.256	11.85 %

4.3 Conclusion

In this chapter, a parametric study based on an analytical heat transfer model was performed to determine the heat spreading requirements to dissipate 500 W/cm² power loss density. Consequently, a solution for heat spreading which is compatible with PCB manufacturing processes was presented. It relies on a sandwiched structure of adhesive and graphite embedded in a PCB package.

Diode and MOSFET PCB packages with embedded graphite were designed and modelled. Several PCB variants with embedded graphite were compared to reference samples without graphite. Thermal impedance simulations were performed to obtain R_{thJA} and R_{thJC} values of the PCB variants. For R_{thJC}, the TDIM method was implemented in simulations according to

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JEDEC51-14 standard. Additional PCB variants with dual diodes were designed and simulated and thermal coupling behavior was compared.

The impact of embedding a graphite heat spreader in the PCB is obvious: up to 51 % reduction in R_{thJA} and 25 % reduction in R_{thJC} was observed by FEM thermal simulations. Moreover, the thermal coupling was increased (from 1.85 % to 11.85 %) due to the graphite layers. This may help balance the temperature of chips, for example in the case of parallel connection.

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5 Heat spreading – test and validation

This chapter presents the experimental validation of graphite embedding in PCB for heat spreading improvement. The fabrication of the diode and MOSFET PCB packages is demonstrated as well as the electrical characterization, the thermo-mechanical tests, and the thermal impedance measurements to obtain R_{thJA} and R_{thJC} for comparison with FEM simulations.

5.1 Fabrication of the PCB with embedded graphite

5.1.1 Fabrication process

As explained in the previous chapter, the objective is to embed graphite heat spreaders in the PCB using a process compatible with the classical PCB manufacturing process (Figure 4.10). A 160 µm-thick epoxy layer (FR4 prepreg) is stacked on a 17 µm-thick sheet of copper. As shown in Figure 5.1, this epoxy layer has a cavity where two pyrolytic graphite sheets (PGS: Panasonic EYGS091205) of 50 µm thickness are stacked together with three thin acrylic-based adhesive layers (DuPont Pyralux LF0100) of 25 µm thickness. An epoxy laminate of 254 µm is then stacked up with a cavity where the chip is placed. A 160 µm FR4 layer is then stacked on top and covered by 17 µm sheet of copper.

After that, the standards of PCB manufacturing are followed: the stack-up is laminated under pressure and temperature; micro vias are UV laser drilled through graphite, then plated with copper using electrodeposition; finally, copper is etched to form copper tracks for electrical connection. The total thickness of the PCB after lamination and copper plating is about 0.8 mm. Figure 5.2 presents some of the produced samples.

Figure 5.3 presents a microscopic image of a cross-section through a PCB sample showing the good contact between the copper vias (vertical thermal path) and the graphite sheets (lateral thermal path) which is a key point for this stack to efficiently spread the heat.

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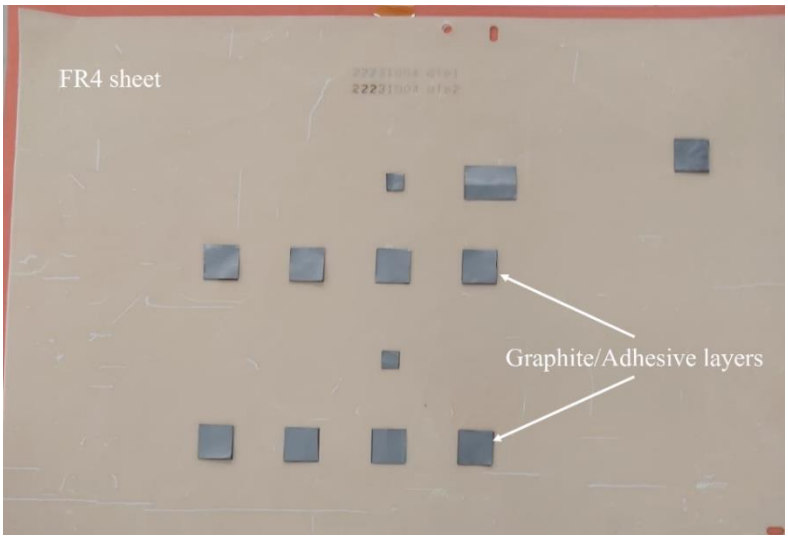

Figure 5.1: Placing graphite/adhesive layers in FR4 cavities during PCB stack-up process.

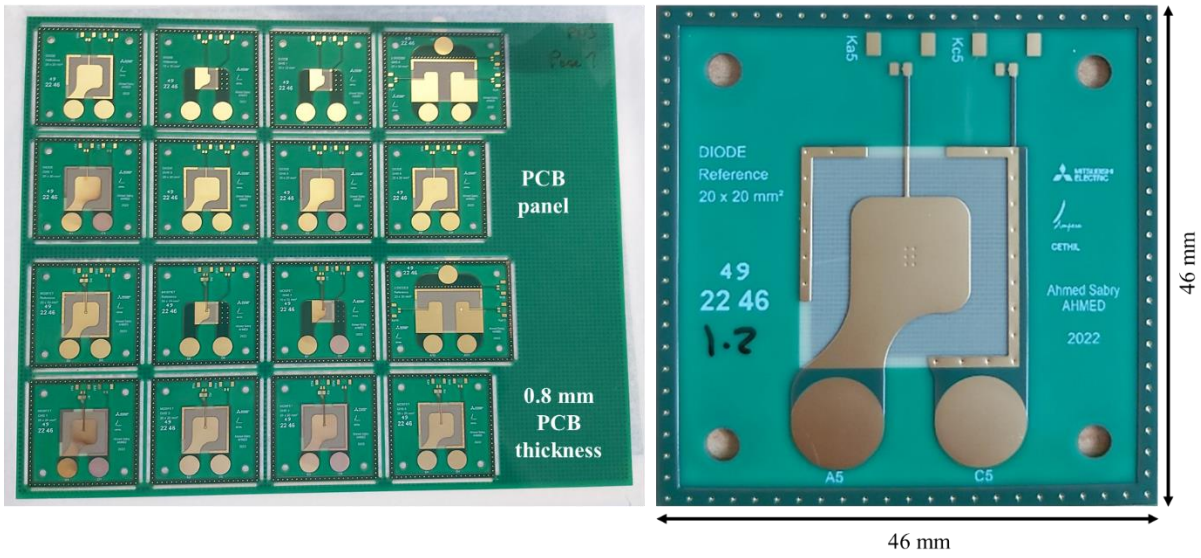

Figure 5.2: Examples of the fabricated PCB samples.

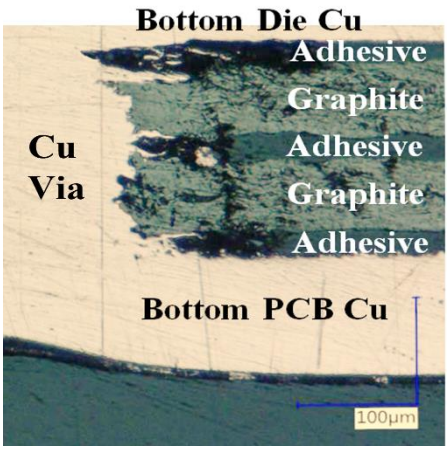

Figure 5.3: Cross-section of a PCB sample with graphite showing copper via through graphite/adhesive stack.

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5.1.2 Difficulties observed during fabrication

During the fabrication process, the placement of graphite/adhesive layers is performed in a way similar to the placement of SiC chips (in an epoxy layer cavity). However, the graphite and adhesive sheets are not perfectly flat, and therefore do not register completely with their cavity which made the alignment of graphite/adhesive layers in the cavity of the epoxy layer less accurate. As a result, a misplacement of graphite layers can be observed through the transparency of the FR4 in few fabricated PCB samples. Figure 5.4 shows an example of a PCB sample with misplaced graphite layers.

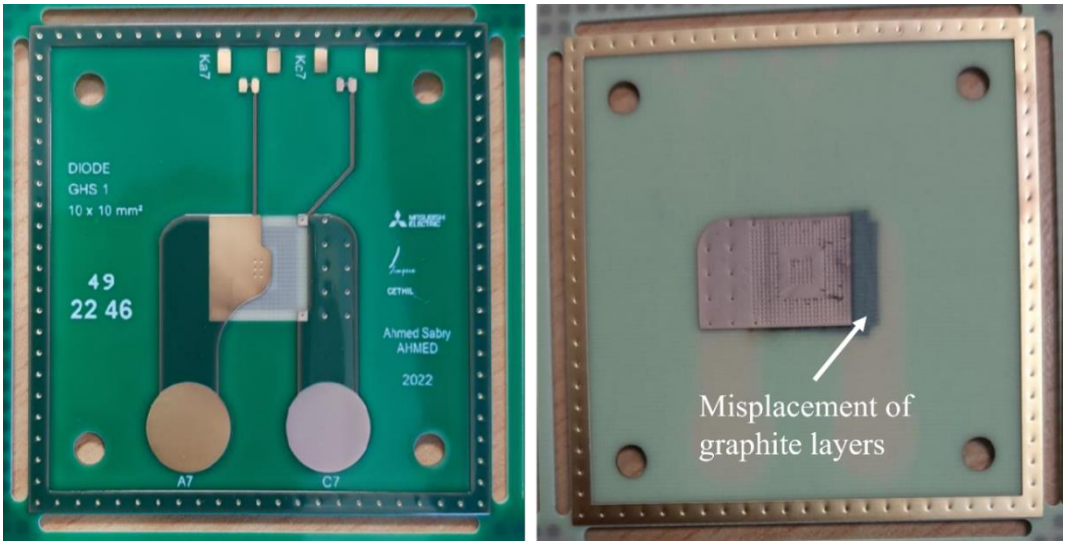

Figure 5.4: Misplacement of graphite layers in a PCB sample.

Another issue is that laser-drilling micro vias through graphite presents some difficulties. An Ultra-Violet (UV) laser has to be used since the CO_2 laser does not work with graphite according to several attempts which have been performed by the manufacturer. As the UV laser can penetrate through the thin (few µm) copper metallization of the embedded chip, a careful tuning of the laser intensity is required so that no damage happens to the chip. Also, the laser power must be adjusted to penetrate through graphite/adhesive layers, which is different than that can penetrate the usual FR4 prepreg.

Even with the UV laser, graphite residues can be found in some micro vias holes after drilling. At the same laser drilling parameters, heterogeneity in drilling can be observed (some holes have residues, some haven't). It can result from a local difference in the thickness or mechanical characteristics. Graphite residues are then cleaned as much as possible by multiple desmearing baths before electrodeposition of copper. Figure 5.5 shows micro vias region

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without graphite residues (left) and micro vias region with graphite residues before cleaning (right).

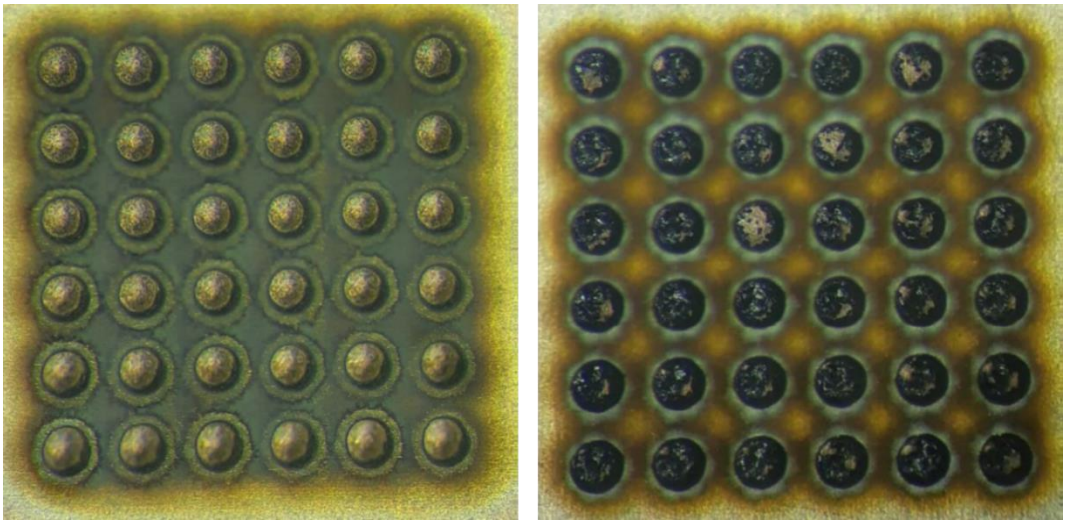

Figure 5.5: Micro vias region without graphite residues (left) and micro vias region with graphite residues before cleaning (right). Micro vias hole diameter is 240 µm.

5.2 Electrical characterization tests

Electrical characterization tests of the 55 diodes and 42 MOSFETs samples are performed using a curve tracer (Keysight B1505A) and a probe station as presented in Figure 5.6. Comparison is made with devices specification to detect any drift which may have been caused by embedding process.

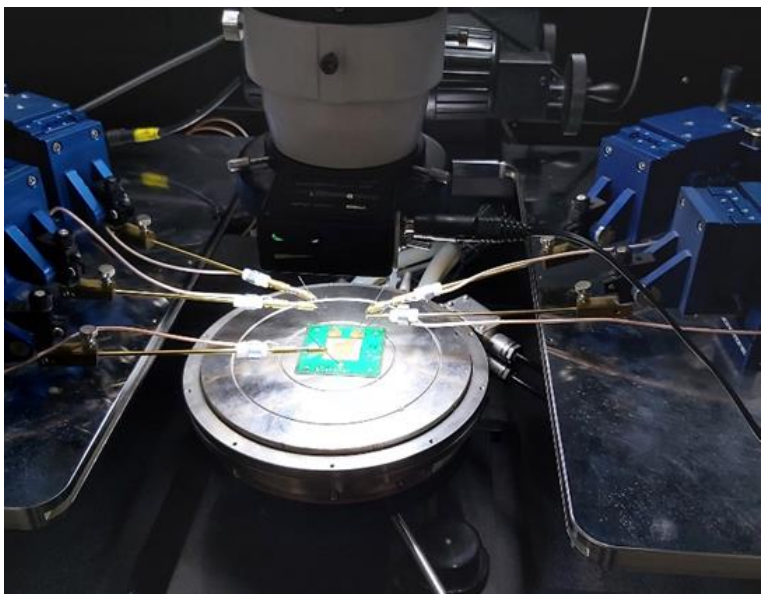

Figure 5.6: Electrical characterization test using probe station.

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Several parameters are tested (such as: leakage currents I_{GS} & I_{DS}, drain-source on resistance R_{DSon}, gate-source threshold voltage $V_{GSTH,}$ drain-source break-down voltage V_{BV}, etc.). In this section, only the parameters for which some chips show deviation with the specifications are presented. Regarding MOSFETs, gate-source threshold voltage (V_{GSTH}) as well as drain-source break-down voltage (V_{BV}) values are shown in Figure 5.7. For diodes, break-down voltage (V_{BV}) values at high voltage are presented in Figure 5.7

The tests conditions are:

- MOSFETs V_{GSTH} measured at V_{DS}=5 V, I_D = 10 mA.
- MOSFETs V_{BV} measured at 10 µA drain current.
- Diodes V_{BV} measured at 100 µA anode current.

MOSFETs dies are CPM2-1200-0080B (1200 V, 36 A) with a minimum V_{BV} of 1200 V and minimum V_{GSTH} of 2 V [124]. In Figure 5.7, results show that 36 out of 48 MOSFETs have a V_{BV} higher than 1500 V while 38 MOSFETs have V_{GSTH} higher than 2 V. The diodes are SiC schottky devices and 47 of them have a V_{BV} higher than 700 V. In consequence, 86 % of the dies are found to be functional which is considered a good yield for the first batch.

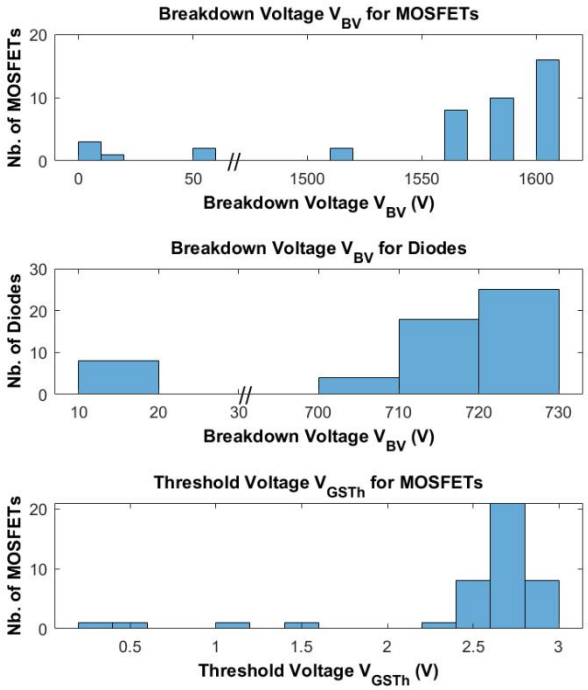

Figure 5.7: Electrical characterization tests results.

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Some of the non-functional samples show after cross-sectioning that the SiC diode was broken during fabrication as shown in Figure 5.8 (probably during the lamination process). This can result from misplacing the die during stack-up process.

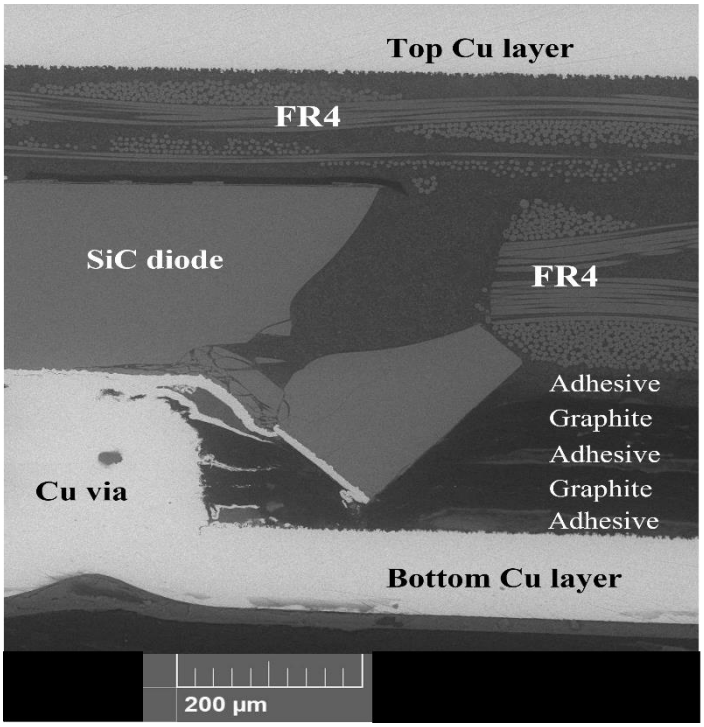

Figure 5.8: Broken SiC chip leading to a non-functional PCB sample.

5.3 Thermal stress reflow test

A thermal stress convection reflow test is performed on some of the PCB samples following the IPC-TM-650 standard [125]. This test simulates thermal cycles experienced by a PCB in soldering ovens when soldering electrical components and connections and is used here as a first assessment of the thermo-mechanical behavior of the graphite heat spreader (graphite and FR4 have very different coefficients of thermal expansion: graphite has 0.93 ppm/K in X-Y plane and 32 ppm/K in Z-axis, compared to FR4 with 14 ppm/K in X-Y plane, and 45 ppm/K in Z-axis). The test is specified by six consecutive thermal cycles with a maximum temperature of 260 °C (corresponding to the reflow cycle for lead-free solder). The temperature profile is described by the IPC-TM-650 standard as two boundaries (upper and lower specification limits, USL & LSL) as indicated in Figure 5.10.

5.3.1 Temperature profile setting of the reflow oven

The reflow oven temperature profile is set initially using a piece of PCB epoxy with a thermocouple attached on it. After that, fresh PCB samples with embedded graphite are used.

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Many trials have been performed to reach a suitable temperature profile consistent with the standard. Because of the small thermal mass and uncontrolled reflection on PCB samples, a graphite box is used to stabilize the temperature profile. The PCB sample is placed in a graphite box as shown in Figure 5.9.

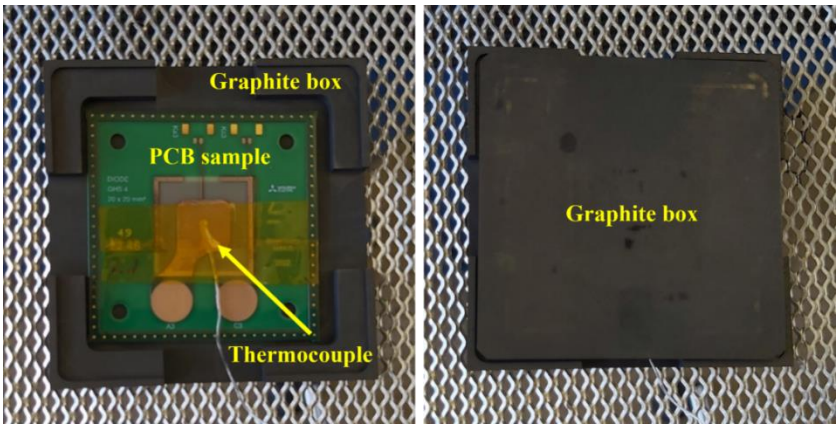

Figure 5.9: PCB sample as placed in the reflow test oven.

The graphite box stabilizes the heating rate by adding more thermal mass and prevents the reflection on the PCB copper. A suitable reflow profile is finally obtained in agreement with IPC-TM-650 standard as shown in Figure 5.10.

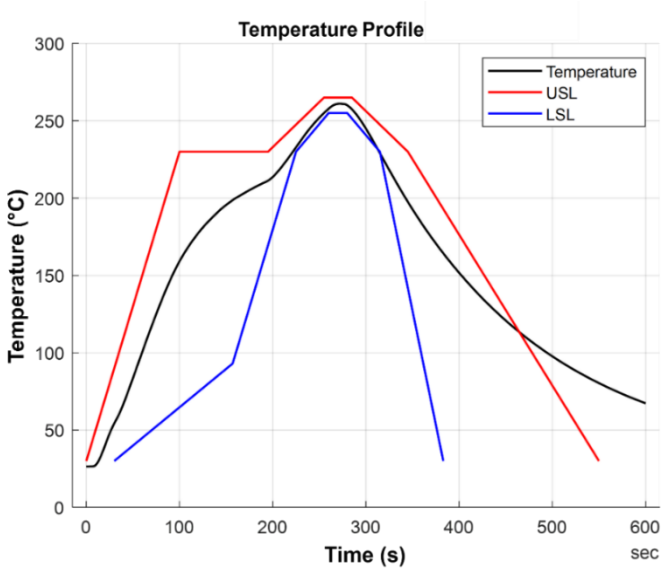

Figure 5.10: Thermal reflow cycle showing temperature profile between USL and LSL profiles.

5.3.2 Samples before and after the reflow test

Profilometer measurements are performed using a Nano-Point-Scanner (NPS-NP3) on different PCB variants before and after reflow test to capture the deformation which may have

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been caused by the thermal stress cycles. Figure 5.11, Figure 5.12, Figure 5.13, and Figure 5.14 show the deformation in micrometers (color scale) observed on the surface of the PCB variants.

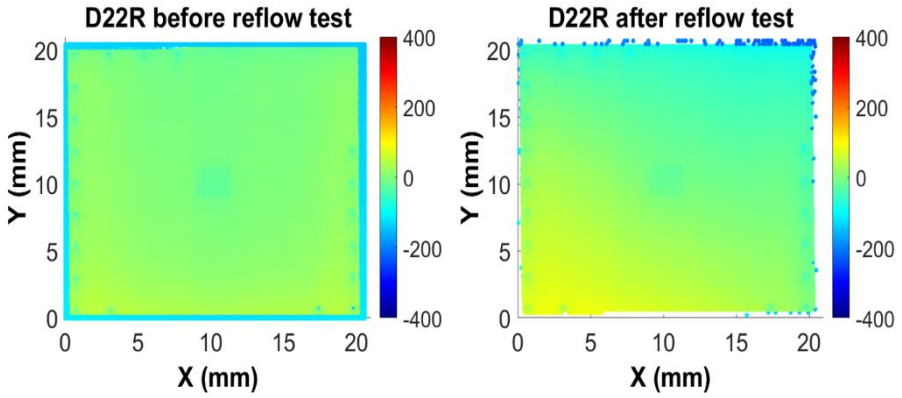

Figure 5.11: Profilometer pictures before and after thermal reflow tests of D22R sample.

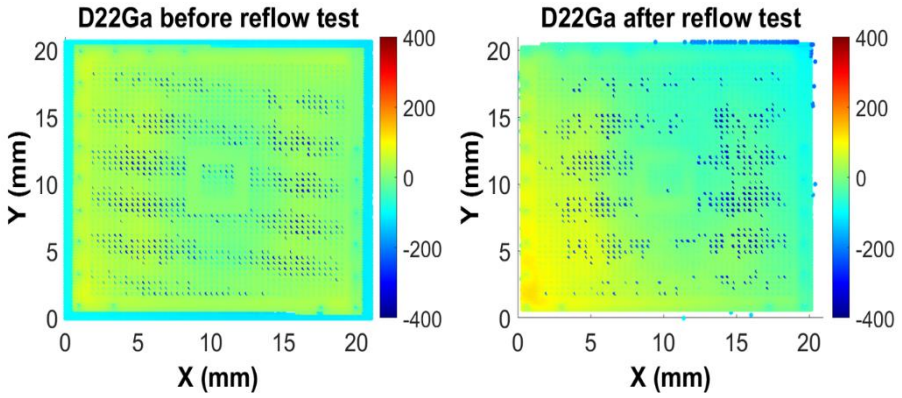

Figure 5.12: Profilometer pictures before and after thermal reflow tests of D22Ga sample.

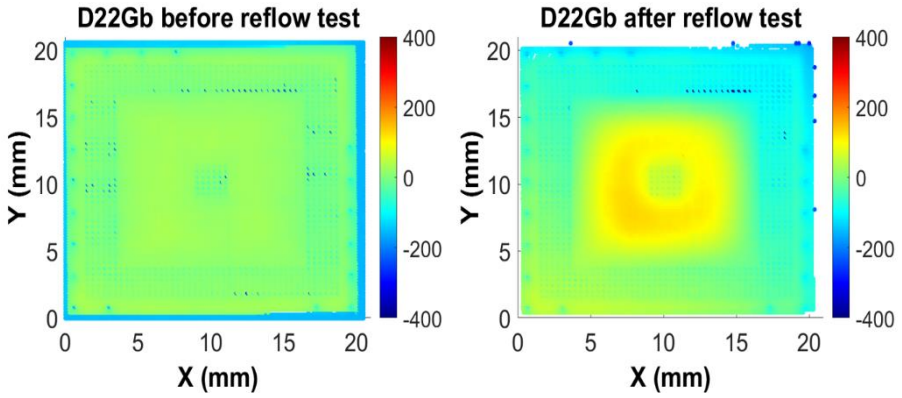

Figure 5.13: Profilometer pictures before and after thermal reflow tests of D22Gb sample.

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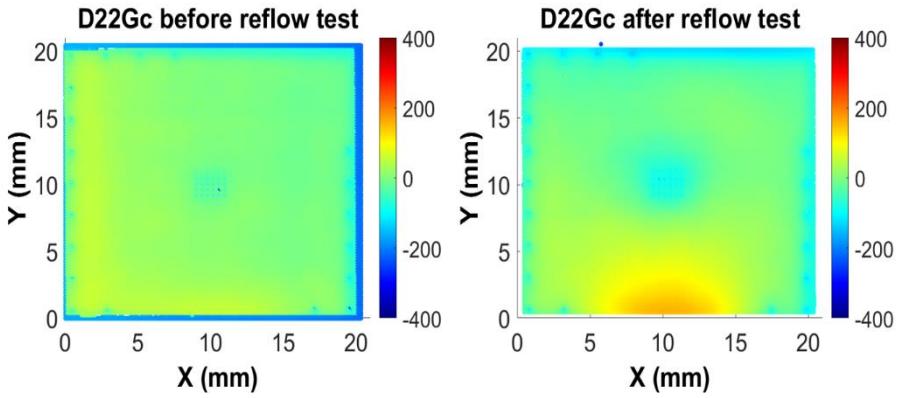

Figure 5.14: Profilometer pictures before and after thermal reflow tests of D22Gc sample.

D22R and D22Ga are not affected by thermal stress cycles except for a little warping that can be observed on the edge. On the other hand, D22Gb show a significant swelling (more than 100 µm) in the middle region where there are no micro vias. D22Gc exhibits swelling at the bottom edge as indicated in Figure 5.14.

In addition to a low CTE (0.93 ppm/K in X-Y plane, and 32 ppm/K in Z-axis) compared to FR4 (14 ppm/K in X-Y plane, and 45 ppm/K in Z-axis), graphite has a low inter-layer shear strength and will exfoliate easily. Therefore, it can be expected that the shear stress that will occur at the graphite-adhesive interface would result in exfoliation of the graphite. This is consistent with the observation that PCB samples with graphite will exhibit swelling if not otherwise contained. Copper vias placed through the copper/adhesive/graphite stack form mechanical clamps which prevent such delamination from propagating through the graphite layers.

Distributed vias were initially designed as a way to increase the thermal conductivity in the z-direction, to overcome the poor thermal conductivity of the adhesive layers (and, to a lower extent, of graphite). However, thermal simulations from chapter 4 show little effect of the vias on the thermal resistance of the samples (in the order of 2 %). But it is in the reflow test that the distributed vias show an unexpected effect: they “nail” together the layers of the PCB stack, preventing graphite defoliation to propagate. While long term reliability tests would be needed to ensure such stack is reliable enough, it seems distributed vias are an interesting solution to stabilize the graphite spreader structure when considering thermo-mechanical stress.

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5.4 Thermal resistance measurements

5.4.1 R_{thJA} results

Thermal impedance tests are performed on all PCB variants using the test protocol as described in 3.4.1. The applied power is adjusted to keep T_j at the level of 70°C to work on the same level of accuracy: 11 W for reference samples (without graphite), 16 W for samples with graphite. Figure 5.15 shows the thermal impedance curves of all tested PCB variants and the corresponding R_{thJA} at the steady state. Five measurements are performed for each variant (the sample was removed and replaced, with a fresh TIM each time). The error bars indicate the standard deviation at each point with respect to the five measurements performed.

Table 5.1 shows experimental R_{thJA} values compared with the values obtained by FEM simulations, as well as the reduction achieved in R_{thJA} by embedding graphite with respect to reference samples. The experimental values are the average of the five measurements, and the error value corresponds to the standard deviation.

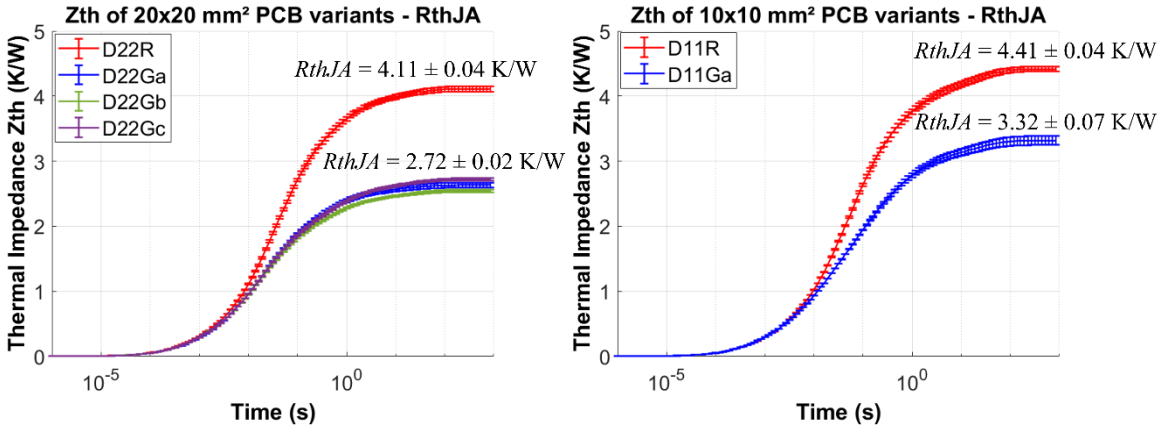

Figure 5.15: Thermal impedance curves of all PCB variants showing R_{thJA} values.

Table 5.1: Experimental R_{thJA} values for all single-diode PCB samples compared to FEM simulations.

PCB Sample	R_{thJA}(K/W)			Reduction in R_{thJA} %	
	Experiment	*FEM*	Difference %	*Experiment*	*FEM*
D22R	4.11 ± 0.04	4.27	3.7 %	REF	REF
D22Ga	2.63 ± 0.04	2.09	26.1 %	– 36 %	– 51 %
D22Gb	2.54 ± 0.02	2.12	20 %	– 38.2 %	– 50.4 %
D22Gc	2.72 ± 0.02	2.2	23.8 %	– 33.8 %	– 48.5 %
D11R	4.41 ± 0.04	4.28	3.1 %	REF	REF
D11Ga	3.32 ± 0.07	2.48	33.8 %	– 24.7 %	– 42.1 %

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The boundary condition (heat exchange coefficient *h* of the cold plate) was adjusted in simulations for the reference PCB sample, the difference with the measurements is only 3.7 % (not 0 % given the accuracy of the measurements). For PCB variants with graphite the difference can reach 20-35 %. This difference means that not all effects are properly modelled (the characteristics of the graphite may differ from their specified values, interfaces are not ideal in reality, some graphite layers may be misaligned, etc.).

Despite the difference between experimental and simulated values, the impact of embedding graphite is obvious. Up to 38 % reduction in R_{thJA} is achieved experimentally (up to 51 % predicted by FEM thermal simulations). Embedding two graphite sheets reduced the R_{thJA} by 34-38 % when comparing PCB variants with graphite to the reference sample D22R (2.54 K/W, 2.63 K/W, 2.72 K/W and 4.11 K/W, respectively).

As shown in the previous chapter, increasing micro vias density (layout Ga or Gb) reduces R_{thJA} by about 2.5 % according to simulations. However, this difference is too small to be validated experimentally because of the limited measurements accuracy. This is why, as shown in the table, the R_{thJA} values of the PCB variants with graphite are not correlated with the density of distributed micro vias: D22Ga exhibits a higher R_{thJA} than D22Gb (2.63 K/W, 2.54 K/W, respectively) although it has higher density of distributed micro vias. However, both layouts Ga and Gb a lower R_{thJA} than the layout without distributed micro vias (Gc).

As predicted by simulations, the effect of graphite on heat spreading can be observed experimentally by comparing the two PCB variants D22Ga with D11Ga (i.e. comparing two sizes of graphite heat spreader, 20×20 mm² and 10×10 mm², respectively). The smaller heat spreader (D11Ga) has a significant higher R_{thJA} 26.2 % than the larger heat spreader (D22Ga) (2.63 K/W, 3.32 K/W, respectively). However, the 10×10 mm² sample (D11Ga) already shows a dramatic heat spreading effect compared to a reference sample of the same size (D11R) even with its relatively modest area. A reduction of 24.7% in R_{thJA} is achieved experimentally (42.1 % in simulations). From this result, it can be concluded that even a 10×10 mm² graphite heat spreader can show a sufficient heat spreading effect for some applications.

5.4.2 R_{thJC} estimations

The dual thermal interface method (TDIM, described in JEDEC51-14 standard [115]) is used to obtain the junction-to-case thermal resistance (R_{thJC}) of the samples. As indicated in 3.4.2.4, the accuracy of TDIM is reported to be within ± 20 % [116]. Adding to the accuracy of R_{thJA}, the estimation of R_{thJC} can have ± 26 % accuracy. This low accuracy makes it difficult to

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distinguish between the R_{thJC} values of different samples especially for low thermal resistance packages.

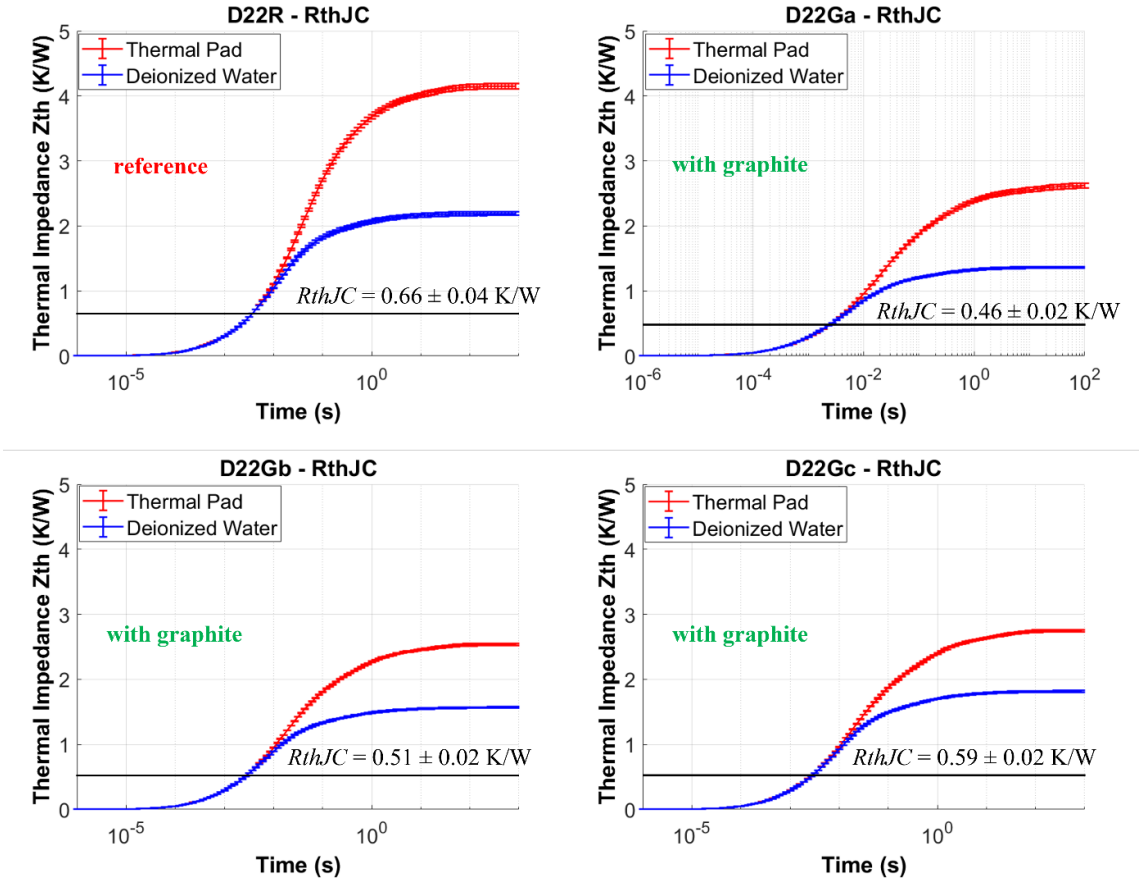

Figure 5.16: Thermal impedance curves produced using different TIMs and the calculated separation point indicating the value of R_{thJC} of 20×20 mm² samples.

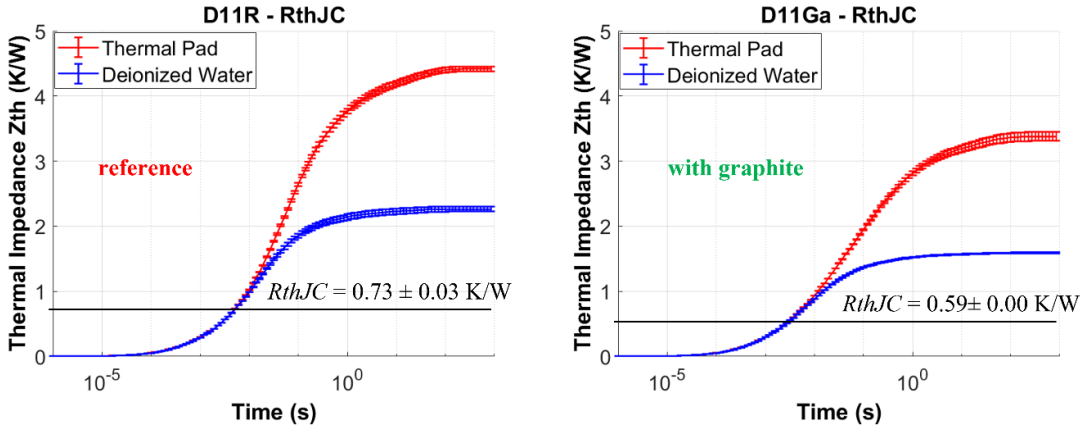

Figure 5.17: Thermal impedance curves produced using different TIMs and the calculated separation point indicating the value of R_{thJC} of 10×10 mm² samples.

R_{thJC} values are estimated for all PCB variants by performing five tests with both TIMs. This results in a 5×5 matrix of R_{thJC} values (i.e. 25 separation points between each of 5 Z_{th} curves

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obtained with one of the TIMs and each pf the 5 Z_{th} curves obtained with the other TIM), using the same approach as presented in [1]. The average value is then taken as the R_{thJC} of the PCB sample. Standard deviation is also calculated to assess reproducibility (Tables 5.2 – 5.7).

Figure 5.16 and Figure 5.17 show the thermal impedance curves produced using different TIMs and the calculated separation point indicating the value of R_{thJC}. The error bars indicate the standard deviation at each point with respect to the five measurements performed.

Table 5.2: R_{thJC} estimation of D22R.

R_{thJC} (K/W) **Reference (D22R)**		**Sil-Pad®1500ST**				
		1	***2***	***3***	***4***	***5***
Deionized Water	***1***	0.6015	0.6504	0.6504	0.6504	0.6504
	2	0.6495	0.6495	0.7119	0.7119	0.6495
	3	0.6572	0.6572	0.7199	0.7199	0.7199
	4	0.5989	0.5989	0.6477	0.6477	0.6477
	5	0.6014	0.6503	0.6503	0.6503	0.6503
Average R_{thJC}	***0.66***					
STD	***0.04***					

Table 5.3: R_{thJC} estimation of D22Ga.

R_{thJC} (K/W) **Graphite (D22Ga)**		**Sil-Pad®1500ST**				
		1	***2***	***3***	***4***	***5***
Deionized Water	***1***	0.4172	0.4172	0.4172	0.4172	0.4616
	2	0.4676	0.4676	0.4676	0.4676	0.4676
	3	0.4691	0.4691	0.4691	0.4691	0.4691
	4	0.4656	0.4209	0.4656	0.4209	0.4656
	5	0.4693	0.4693	0.4693	0.4693	0.4693
Average R_{thJC}	***0.46***					
STD	***0.02***					

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Table 5.4: R_{thJC} estimation of D22Gb.

R_{thJC} (K/W) Graphite (D22Gb)		Sil-Pad®1500ST				
		1	*2*	*3*	*4*	*5*
Deionized Water	*1*	0.5087	0.5087	0.5087	0.5087	0.5087
	2	0.4683	0.5089	0.5089	0.5089	0.5089
	3	0.5105	0.5105	0.5105	0.5562	0.5562
	4	0.5102	0.5102	0.5102	0.5102	0.5102
	5	0.5109	0.5109	0.5109	0.5109	0.5109
Average R_{thJC}	***0.51***					
STD	***0.02***					

Table 5.5: R_{thJC} estimation of D22Gc.

R_{thJC} (K/W) Graphite (D22Gc)		Sil-Pad®1500ST				
		1	*2*	*3*	*4*	*5*
Deionized Water	*1*	0.5557	0.5979	0.5979	0.5979	0.5979
	2	0.5582	0.6004	0.6004	0.6004	0.6004
	3	0.5558	0.598	0.598	0.598	0.598
	4	0.5569	0.5991	0.5991	0.5991	0.5991
	5	0.5559	0.5559	0.5979	0.5559	0.5559
Average R_{thJC}	***0.59***					
STD	***0.02***					

Table 5.6: R_{thJC} estimation of D11R.

R_{thJC} (K/W) Reference (D11R)		Sil-Pad®1500ST				
		1	*2*	*3*	*4*	*5*
Deionized Water	*1*	0.7242	0.7242	0.7242	0.7242	0.7242
	2	0.7877	0.727	0.7877	0.727	0.727
	3	0.7258	0.7258	0.7258	0.7258	0.7258
	4	0.7251	0.7251	0.7251	0.6661	0.6661
	5	0.7268	0.7268	0.7268	0.7268	0.7268
Average R_{thJC}	***0.73***					
STD	***0.03***					

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Table 5.7: R_{thJC} estimation of D11Ga.

R_{thJC} (K/W) Graphite (D11Ga)		Sil-Pad®1500ST				
		1	***2***	***3***	***4***	***5***
Deionized Water	***1***	0.5906	0.5906	0.5906	0.5906	0.5906
	2	0.5924	0.5924	0.5924	0.5924	0.5924
	3	0.5919	0.5919	0.5919	0.5919	0.5919
	4	0.5922	0.5922	0.5922	0.5922	0.5922
	5	0.5931	0.5931	0.5931	0.5931	0.5931
Average R_{thJC}	***0.59***					
STD	***0.00***					

Table 5.8 compares the experimental and simulated R_{thJC} values for the all single-diode PCB variants. Experiments show a reduction of 10-30 % in R_{thJC} for the PCB variants with graphite compared to the reference sample, while simulations show a 25 % reduction in R_{thJC} by embedding graphite. Regarding the 10×10 mm² samples, the reduction achieved in R_{thJC} is 19 % experimentally for D11Ga with respect to the reference sample D11R, while simulations predict 11.7 % reduction in R_{thJC}. A difference of up to 31 % can be observed between experimental measurements and FEM thermal simulations which suggest a deviation in the fabricated PCB samples from the simulation model. Due to TDIM accuracy, the difference between the experiment and the simulation of R_{thJC} value for each PCB variant is not consistent compared to that of R_{thJA} value.

Table 5.8: Experimental R_{thJC} values for all single-diode PCB samples compared to FEM simulations.

PCB Sample	***R_{thJC}(K/W)***			**Reduction in R_{thJC} %**	
	Experiment	***FEM***	**Difference %**	***Experiment***	***FEM***
D22R	0.66 ± 0.04	0.6	10	REF	REF
D22Ga	0.46 ± 0.02	0.465	1.1	– 30.3 %	– 22.5 %
D22Gb	0.51 ± 0.02	0.45	13.3	– 22.7 %	– 25 %
D22Gc	0.59 ± 0.02	0.45	31.1	– 10.6 %	– 25 %
D11R	0.73 ± 0.03	0.6	21.7	REF	REF
D11Ga	0.59 ± 0.00	0.53	11.3	– 19.2 %	– 11.7 %

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Because of the accuracy limitations of the TDIM discussed before, it is not possible to draw a conclusion from the experimental data regarding the different vias layouts. R_{thJC} calculation using TDIM is sensitive to many parameters, such as package geometry, material specifications, TIMs, and the cold plate. Besides, thermal resistance definition between two surfaces assumes that both surfaces are isothermal which is not the reality here since case temperature is not uniform nor is T_j. For these reasons, obtaining reproductible values of R_{thJC} using TDIM can be challenging and requires much effort and trials.

It is worth noting that the effect of the graphite heat spreader cannot be captured by the R_{thJC} value alone: the reduction in R_{thJC} between D22Ga and D22R is 0.2 K/W only (experimental values). However, when considering R_{thJA} (i.e. the complete heat path, from junction to case to ambient, which is the water inlet of the cold plate), the reduction is much larger (from 4.11 K/W down to 2.63 K/W in Table 5.8, or a 1.47 K/W difference). This highlights that the spreading effect offered by the graphite also allows to use the cold plate and TIM layer much more efficiently.

5.4.3 Comparison with a TO-247-3 package

The objective of this section is to provide a comparison point between the samples presented so far with a more conventional power packaging technology. The same MOSFET chips, packaged by their manufacturer in a TO-247-3 package are characterized thermally using the same protocol as previously described. In this package, the SiC die is sintered directly on a thick (2 mm) copper lead frame. The amount of copper and the direct sintering of the die in TO-247-3 package improve its heat spreading function compared to a PCB package, at the expense of a bulkier package.

Figure 5.18 shows the difference between MOSFET TO-247-3 package and a classical PCB package. Figure 5.19 shows the TO-247-3 package on the thermal test setup.

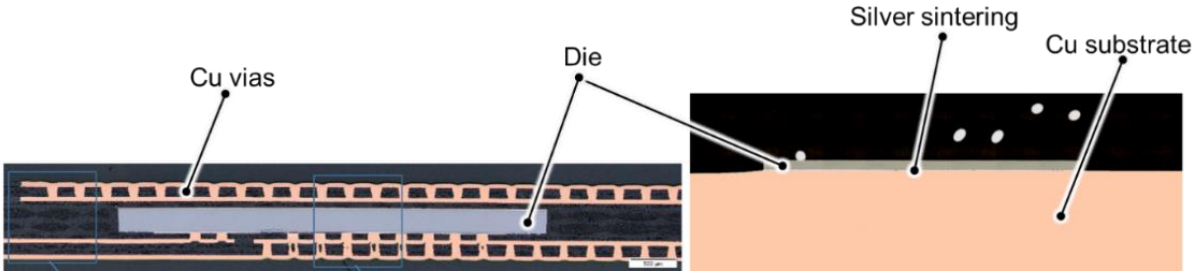

Figure 5.18: Typical PCB stack with embedded die and 4 layers of via interconnections (left) in comparison with direct silver sintering die in a TO-247-3 package (right [126]).

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Figure 5.19: TO-247-3 package on the thermal test setup.

Thermal impedance tests are performed on MOSFET samples M22R (reference), M22Ga (with graphite), and ta commercial TO-247-3 package with the same MOSFET die. R_{thJA} and R_{thJC} values are obtained and compared. Figure 5.20 shows the thermal impedance curves of the MOSFET samples indicating the R_{thJA} values while Figure 5.21 and Figure 5.22 show the calculated R_{thJC} using TDIM.

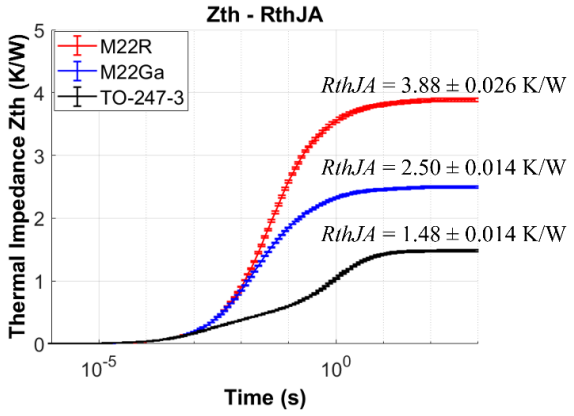

Figure 5.20: Thermal impedance curves of MOSFET PCB samples compared to TO-247-3 MOSFET package showing R_{thJA} values.

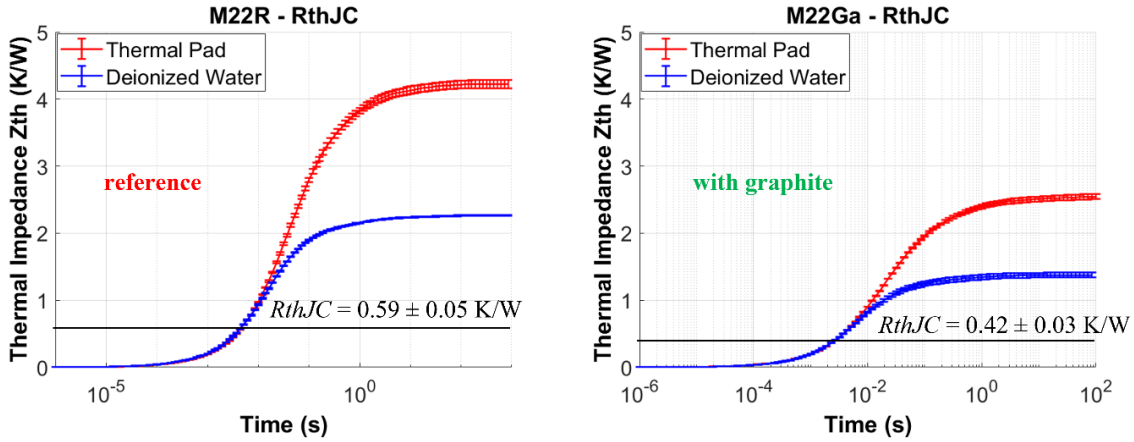

Figure 5.21: Thermal impedance curves produced using different TIMs and the calculated separation point indicating the value of R_{thJC} of MOSFET PCB samples.

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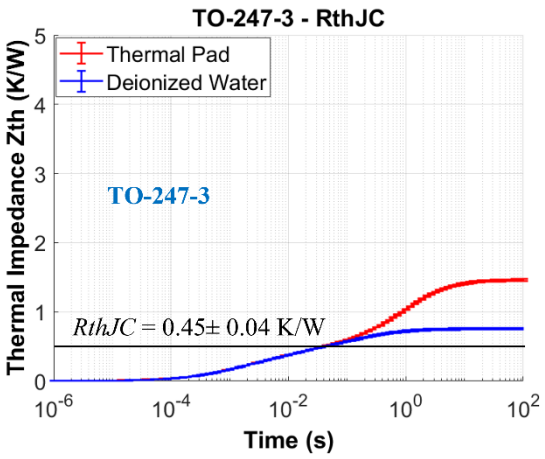

Figure 5.22: Thermal impedance curves produced using different TIMs and the calculated separation point indicating the value of R_{thJC} of MOSFET TO-247-3 package.

Table 5.9: R_{thJC} estimation of M22R.

R_{thJC} (K/W) Reference (M22R)		Sil-Pad®1500ST				
		1	***2***	***3***	***4***	***5***
Deionized Water	***1***	0.5921	0.5308	0.5308	0.5921	0.5921
	2	0.6662	0.6028	0.6028	0.6028	0.6662
	3	0.5904	0.4713	0.5295	0.5295	0.5904
	4	0.6635	0.5997	0.5997	0.5997	0.6635
	5	0.6633	0.5386	0.5386	0.6002	0.6633
Average R_{thJC}	0.59					
STD	0.05					

Table 5.10: R_{thJC} estimation of M22Ga.

R_{thJC} (K/W) With graphite (M22Ga)		Sil-Pad®1500ST				
		1	***2***	***3***	***4***	***5***
Deionized Water	***1***	0.4399	0.4399	0.4399	0.481	0.4399
	2	0.3925	0.3925	0.3925	0.4373	0.4373
	3	0.3873	0.3873	0.3873	0.4321	0.4321
	4	0.3918	0.3918	0.3918	0.4363	0.3918
	5	0.3908	0.3908	0.4359	0.4359	0.4359
Average R_{thJC}	0.42					
STD	0.03					

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Table 5.11: R_{thJC} estimation of TO-247-3 package.

R_{thJC} (K/W) TO-247-3		Sil-Pad®1500ST				
		1	***2***	***3***	***4***	***5***
Deionized Water	***1***	0.467	0.418	0.439	0.467	0.404
	2	0.485	0.457	0.471	0.485	0.485
	3	0.431	0.431	0.445	0.438	0.466
	4	0.486	0.443	0.464	0.309	0.486
	5	0.438	0.418	0.431	0.438	0.404
Average R_{thJC}	0.44					
STD	0.04					

Table 5.12 shows the experimental R_{thJA} and R_{thJC} values for single-MOSFET PCB samples compared to TO-247-3 MOSFET package (note that results in Table 5.1 and Table 5.8 correspond to diode samples, not MOSFETs). As shown for the diode PCB samples, the MOSFET M22Ga graphite sample offers a 36 % reduction in R_{thJA} compared to the M22R reference sample, and a 29 % reduction in R_{thJC}. When comparing with Table 5.1 and Table 5.8. One can also observe that the R_{thJA} of M22R and M22Ga is about 5 % lower than that of D22R and D22Ga. This is consistent with the difference in die size between the MOSFET and the diode.

The R_{thJA} of M22Ga and M22R are 69 % and 162 % higher than that of the TO-247-3, respectively. This large difference is much smaller when considering R_{thJC}, for which TO-247-3 and M22Ga show no significant difference (0.44±0.04 K/W and 0.42±0.03 K/W, respectively). This is because of the spreading effect that is not considered in the definition of R_{thJC}, which assumes one-directional heat flux between two isothermal surfaces. This, together with the modest increase in R_{thJA} when reducing the spreading area from 20×20 mm² to 10×10 mm² (D22Ga and D11Ga in table Table 5.1) seems to indicate that the graphite heat spreader is not efficient enough to fully utilize the 20×20 mm² area. For such large surface, the thick copper layers of the TO-247-3 package offers better heat spreading performance, at the expense of a much thicker package (5 mm for the TO-247-3, 0.8 mm for the PCB samples).

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Table 5.12: Experimental R_{thJA} and R_{thJC} values for single-MOSFET PCB samples compared to TO-247-3 MOSFET package.

PCB Sample	***R_{thJA}(K/W)*** ***Measurements***	***R_{thJC}(K/W)*** ***Measurements***	***Difference % in R_{thJA} w.r.t. TO-247-3***
M22R	3.88 ± 0.026	0.59 ± 0.05	+162 %
M22Ga	2.50 ± 0.014	0.42 ± 0.03	+ 69 %
TO-247-3	1.48 ± 0.014	0.44 ± 0.04	REF

5.4.4 Double-diode PCB variants and thermal coupling

In this section, the experimental measurements are performed on the double-diodes PCB samples by measuring the thermal impedances of the two diodes and obtaining the effect of embedding graphite on the percentage of thermal coupling.

A comparison is made between PCB sample with embedded graphite and the reference PCB sample without graphite. Figure 5.23 shows an example of the fabricated double-diodes PCB sample on the thermal impedance measurements test fixture.

Figure 5.24 shows the thermal impedance measurements of samples 2D23R (reference) and 2D23Gc (with graphite). The measurement of the thermal impedance is taken for each diode when the power is applied to only one diode (ON) as presented in the figure. Thermal impedance curves are compared to those obtained by transient FEM simulations.

The thermal coupling percentage can be defined by the following equations:

$$Thermal\ coupling\ \% = 100 \times \frac{R_{thJA-D2-OFF}}{R_{thJA-D1-ON}}$$

Where $R_{thJA\text{-}D1\text{-}ON}$ is the R_{thJA} of the first diode while dissipating heat (ON) and $R_{thJA\text{-}D2\text{-}OFF}$ is the R_{thJA} of the second diode with no heat dissipation (OFF).

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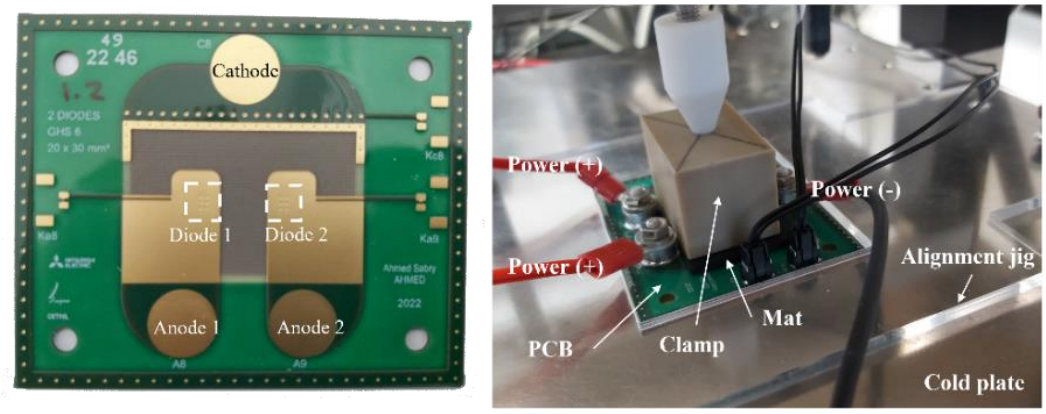

Figure 5.23: The fabricated double-diode PCB and the thermal impedance experimental setup.

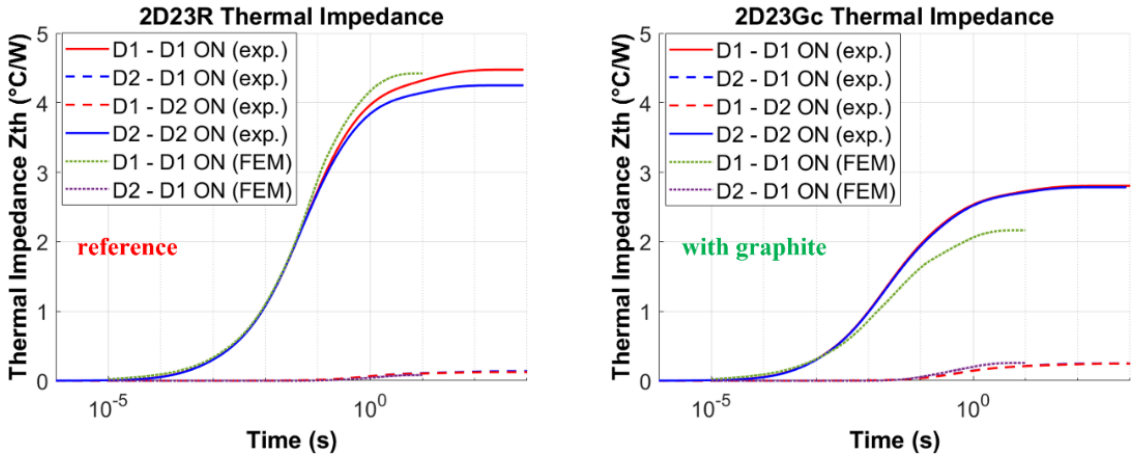

Figure 5.24: Thermal impedance curves comparison. “Exp”: experimental results; “FEM”: finite elements (Ansys Mechanical) simulation results. D1/D2 correspond to diodes 1 and 2 in Figure 5.23; “DX – DX ON” correspond to “self” thermal impedances, while “DX – DY ON” correspond to coupling impedances. Due to the symmetry in the FEM model, only the case when diode 1 is ON is considered, since the other case is identical.

Table 5.13: Thermal coupling percentage by experiment and FEM simulations.

Method	**PCB variant**	**D1-ON & D2-OFF**		**D1-OFF & D2-ON**		**Thermal coupling %**	
		$R_{thJA\text{-}D1}$ (K/W)	$R_{thJA\text{-}D2}$ (K/W)	$R_{thJA\text{-}D2}$ (K/W)	$R_{thJA\text{-}D1}$ (K/W)	**D1-ON**	**D2-ON**
Exp.	2D23R	4.48	0.137	4.25	0.125	3.06 %	2.94 %
	2D23Gc	2.8	0.248	2.79	0.245	8.86 %	8.78 %
FEM	2D23R	4.42	0.082	4.42	0.082	1.85 %	1.85 %
	2D23Gc	2.16	0.256	2.16	0.256	11.85 %	11.85 %

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R_{thJA} values are obtained at the steady state of the thermal impedance curves. This steady state is reached rapidly in simulation (2-3 s vs. 100s in experiments) because the cold plate model is a simple heat exchange coefficient, with no thermal mass, while in reality the cold plate is a large and thick piece (1 cm) of copper. Table 5.13 shows the values of R_{thJA} of the two diodes when applying the power to only one diode. The percentages of the thermal coupling in 2D23R and 2D23Gc are compared, showing an increase in thermal coupling by 5.8 % (from 2.94 % in 2D23R to 8.87 % in 2D23Gc) due to graphite heat spreading effect.

The percentage of thermal coupling due to graphite increases by 5.8 percentage points in measurements compared to 10 percentage points in simulations. This difference can be caused by the same issues as discussed before (deviation in manufacturing, interface effects...). It can also be due to the accuracy of the R_{thJA} measurements, because a diode in the OFF-state only heats up by a few degrees (as discussed in chapter 3, measurement accuracy depends on T_j increase, the lower the T_j the worse the accuracy). This leads to an exaggeration of the temperature difference of the OFF-state diode, leading to an exaggerated $R_{thJA\text{-}Dx\text{-}OFF}$ which overestimates the value of the thermal coupling percentage.

5.5 Conclusion

This chapter has presented the experimental validation of our embedded graphite heat spreader. Diode and MOSFET PCB packages with embedded graphite were successfully fabricated and compared to reference samples without graphite. An 86 % manufacturing yield for the embedded semiconductor devices has been measured, a reasonable value for a prototype run. Reflow tests show that a micro-vias must be distributed over the spreader area to provide mechanical clamping of the graphite layers, and prevent their delamination.

Thermal impedance measurements and simulations were performed to obtain R_{thJA} and R_{thJC} values of the samples. For R_{thJC}, the JEDEC51-14 method was implemented experimentally (as it was in simulation, see chapter 4). The impact of embedding a graphite heat spreader in the PCB is measured. Up to 38 % reduction in R_{thJA} and 30 % reduction in R_{thJC} are observed experimentally.

The R_{thJA} of traditionally-packaged chips (TO-247-3) remains lower than that of PCB-embedded devices with a graphite heat spreader, indicating a more efficient spreading effect for a thick copper lead frame than for thin graphite layers. However, the graphite heat spreader constitutes an interesting trade-off, offering a clear improvement over standard PCBs without any increase in board thickness or the steps of the manufacturing process.

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Additionally, dual diodes PCB samples were thermally measured to obtain the thermal coupling effect of graphite in multi-chip PCB package. Thermal coupling percentage has increased from 2.94 % in the reference PCB sample to 8.78 % by embedding graphite in the PCB.

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6 Heat extraction

This chapter starts by an estimation of the effective heat transfer coefficient needed to reach the targeted power loss density (1000 W/cm² at chip level). After that, a water jet impingement cooler (JIC) is presented as the heat extraction solution. The JIC consists of two parts: the pin-fin heat sink and the water manifold. This chapter explains the design and fabrication of the pin-fin heat sink and its lamination with the PCBs. In addition, the design and the fabrication of the water manifold of the JIC are illustrated. Finally, CHT simulations and thermo-hydraulic measurements results of R_{thJA} and ΔP for a range of water volume flow rates are compared and discussed.

6.1 The targeted effective heat transfer coefficient

As presented in previous chapters, the graphite heat spreading solution can dissipate a power loss density up to 500 W/cm² without exceeding 175°C junction temperature T_j (the limit for both FR4 and SiC chips) using a conventional cold plate with an effective heat transfer coefficient (HTC) of 6000 W/(m².K) (equivalent value which consider both the cold plate and the TIM).

By referring to the literature survey in Chapter 2 section 2.2.2.2, liquid jet impingement technique integrated with efficient surface enlargement of the heat exchange surface, such as pin-fins, is found to be capable of cooling high power loss density close to 1000 W/cm². In order to estimate the effective HTC requirements of a water jet impingement cooler that would result in a T_j of 175°C or less at power loss density of 1000 W/cm² (104.16 W), thermal simulations are performed (as illustrated in section 3.3.3.3.1 and section 4.2.6) by varying the HTC boundary condition from 5000 to 50000 W/(m².K) (which is the expected limit of the water jet impingement cooling based on the literature survey in chapter 2) . Note that in addition to the PCB stack, the model considered here also includes a 60 µm-thick high-performance prepreg layer (Rogers 92ML, 2.5 W/(m.K)), which is used both as a TIM and for electrical isolation, as the backside of the PCB samples is electrically active.

Figure 6.1 shows the R_{thJA} and T_j of the reference PCB variant without graphite (M22R) and the variant M22Gc with graphite. As shown in the Figure 6.1, the T_j of the PCB variant with graphite M22Gc does not reach the 175°C or less. Even at 50000 W/(m².K) effective HTC, it reaches 192°C. This suggests that achieving a T_j of 175°C or less is not feasible at a power loss density of 1000 W/cm² with this configuration of the PCB and the available isolation layer.

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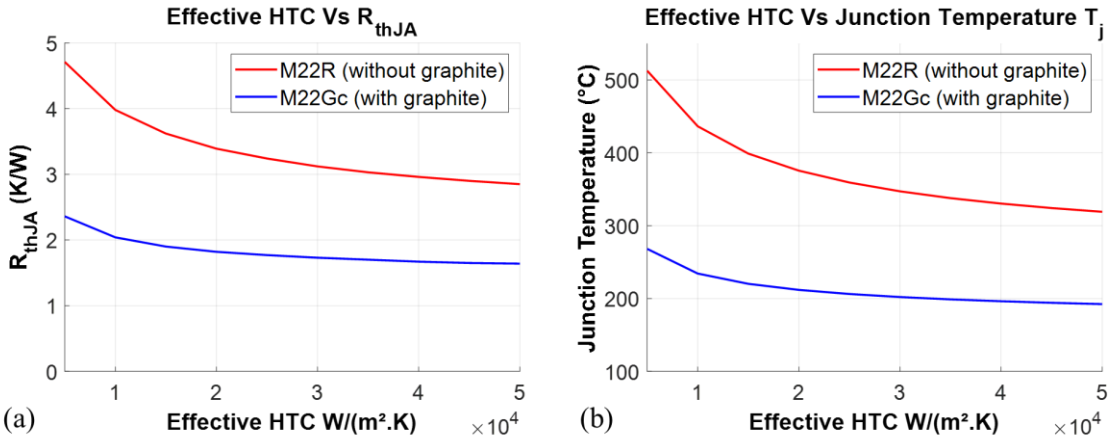

Figure 6.1: The R_{thJA} and T_j variation with the effective HTC of the cooling system.

The R_{thJA} of the PCB variant with graphite M22Gc at 50000 W/(m².K) is 1.64 K/W. When increasing the power loss density, the T_j is increased. By linear interpolation, the T_j reaches the limit of 175°C at power loss density of 895.7 W/cm² (93.3 W) at HTC equal to 50000 W/(m².K).

From previous analysis, it can be seen that reaching a power loss density of 1000 W/cm² is not feasible. However reaching ~900 W/cm² can be achievable by cooling the PCB variant with graphite by a 50000 W/(m².K) effective HTC cooler. This value of HTC is reachable by water jet impingement cooling techniques.

6.2 The concept of water jet impingement cooler (JIC)

The objective of the JIC here is to maximize the effective heat transfer coefficient while keeping the pumping power at a minimum. The heat sink of the JIC must be compatible with the PCB manufacturing process and packaging technology which imposes constraints on its fabrication method and, therefore, its geometry.

Figure 6.2 shows the concept of the water JIC. It consists of the water manifold, and copper pin-fin heat sink. The water manifold is fabricated by the means of additive manufacturing. Since it has no requirement for thermal conductivity, the water manifold can be made out of a polymer, and 3D printing is a good solution for prototyping. The copper pin-fin heat sink is fabricated by chemically etching a plate of copper in order to form the pin-fins (chemical etching process is used in PCB fabrication to form copper tracks for electrical connections). After that, it is laminated to the PCB package using an electrically isolating prepreg layer (lamination is an essential process in the fabrication of PCBs). This makes it possible to

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fabricate the PCB with its pin-fin heat sink as one part by using the standard PCB manufacturing process (the heat sink simply being a thick copper layer in the PCB stack). The PCB can then be simply assembled to the water manifold using screws and O-ring seal to prevent water leakage.

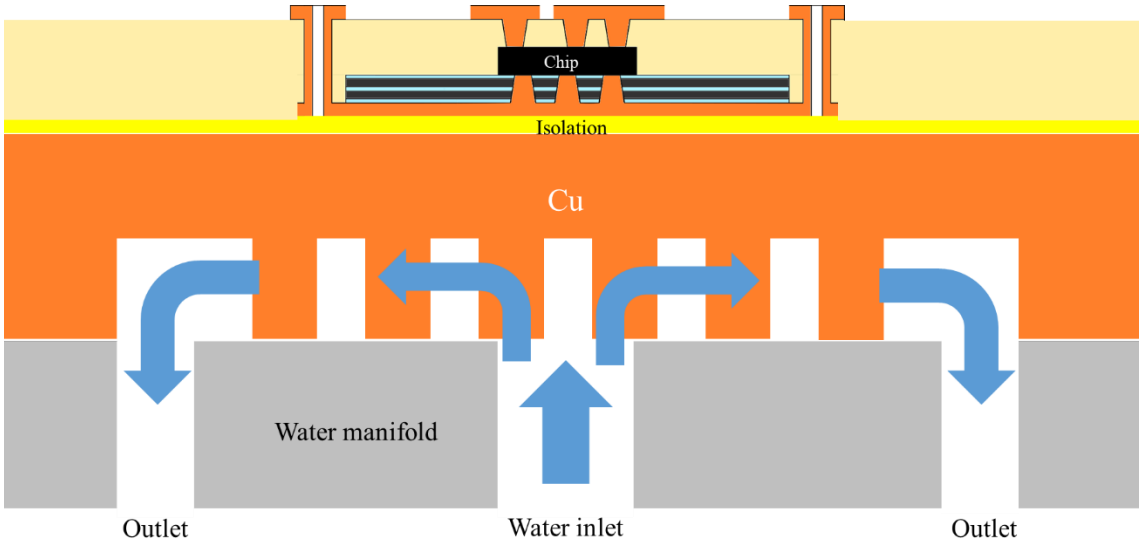

Figure 6.2: The concept of the water JIC.

6.2.1 Pin-fin heat sink fabrication by chemical etching

Square copper plates of 1.5 mm thickness and 46×46 mm² (the size of PCB samples) are cut out of a larger sheet. The pattern of the pin-fins is first designed and printed on a transparent plastic mask. The copper plate is coated with a photoresist film (Dupont Riston), which is a light-sensitive material, and exposed to UV light through the mask. After that, the sample is dipped into a developer (MIF 726) which dissolves only the areas of the photoresist film that were not exposed to light. After developing, the remaining photoresist film has the desired pattern. The copper plate is then chemically etched by exposing it to a spray of a chemical etcher (ferric chloride in a Bernier Electronic PR2030S etcher) that attacks the bare areas of the copper which are not covered by the photoresist film.

6.2.1.1 First etching trial

The objective of this trial is to evaluate the capability of reaching a depth of etching of 1000 µm and the effect on the pin-fin diameter. Indeed, copper etching occurs in all directions, resulting in the pins becoming thinner as etching progresses deeper. That is why it is important to compensate for the diameter reduction by increasing the fins diameter on the mask. This first etching trial is aimed at assessing the relationship between diameter reduction and etching depth.

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Masks for four patterns are prepared: two patterns with circular shaped pin-fins having an initial diameter of 1.5 mm and 2 mm (Figure 6.3a and Figure 6.4a); two patterns with an airfoil shape of NACA0024 having a chord (length of the airfoil) of 2 mm and 4 mm. This symmetric airfoil shape has its maximum thickness equal to 24 % of the chord located at 40 % of the cord (Figure 6.3b and Figure 6.4b). Three etching depths are considered: 300 µm, 600 µm, and 1000 µm. These samples are prepared in 3DPHI platform in Toulouse.

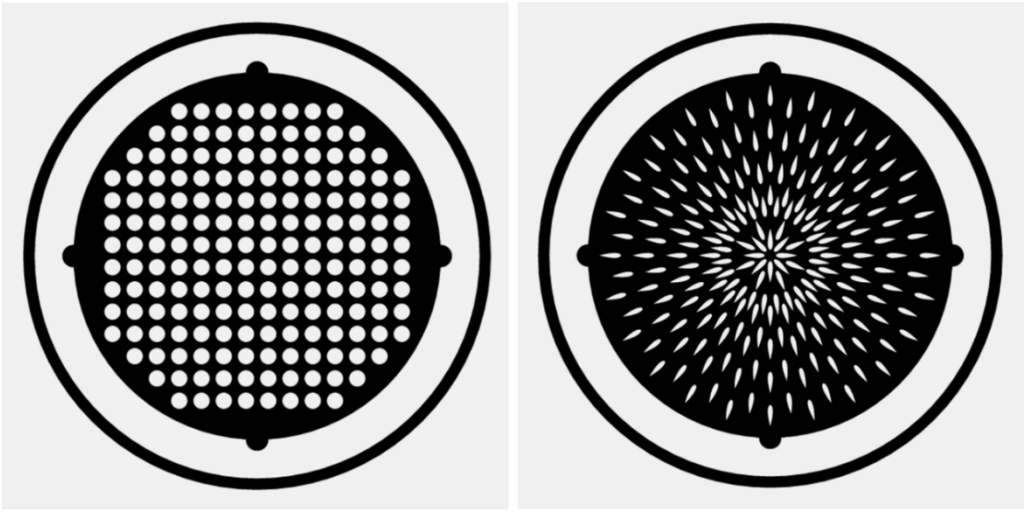

Figure 6.3: Pin-fins patterns for etching: (a) circular pin-fins with 1.5 mm initial diameter. (b) NACA0024 airfoil shaped pin-fins with 2 mm initial chord.

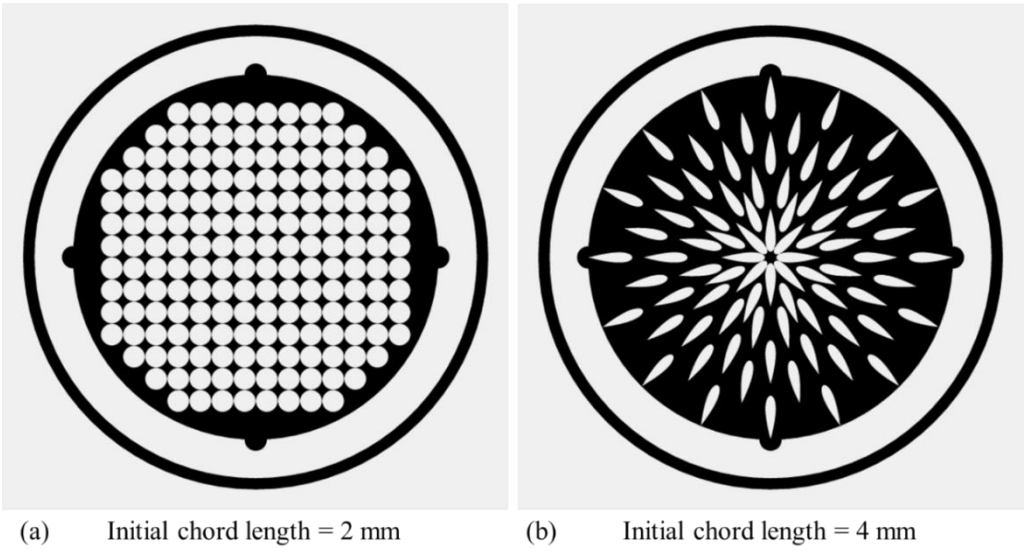

Figure 6.4: Pin-fins patterns for etching: (a) circular pin-fins with 2 mm initial diameter. (b) NACA0024 airfoil shaped pin-fins with 4 mm initial chord.

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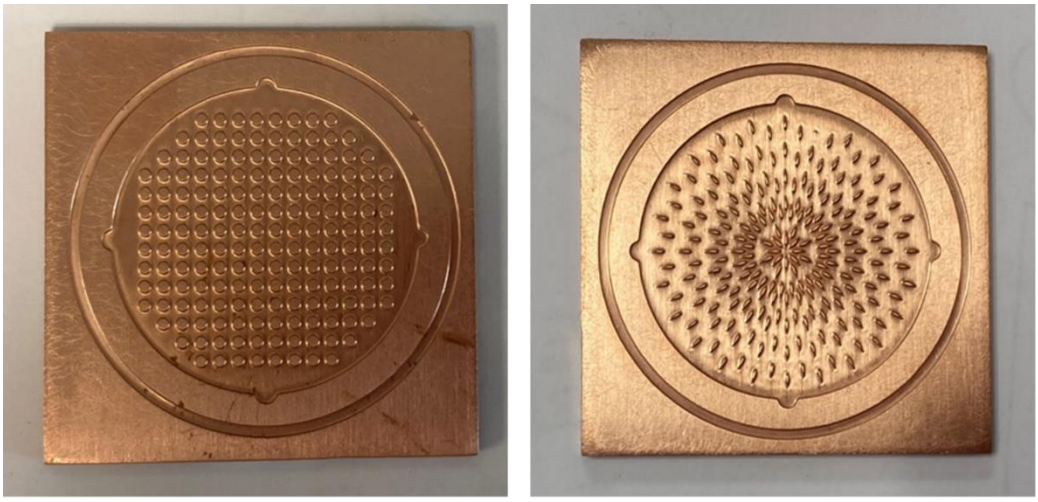
Figure 6.5 shows the 1.5 mm pin-fins and NACA0024 samples after the chemical etching. Figure 6.6 shows a microscopic picture of the circular pin-fins after etching of 300 µm indicating that the resulting etching depth measured is ~290 µm. While the diameter of the circular pin-fin is found to be ~ 1 mm. For the NACA0024 pin-fins, the chord length is measured at ~1 mm after etching ~300 µm compared to 2 mm initial chord length (Figure 6.7). The thickness of the airfoil is reduced from 480 µm to ~240 µm after etching keeping the same percentage of 24% from the chord length. This means that the size of the NACA024 airfoil pin-fins will reduce to its half when reaching ~300 µm etching depth.



(a) Circular – etching depth = ~300 µm (b) NACA0024 – etching depth = ~300 µm

Figure 6.5: Copper plates after chemical etching of ~300 µm: (a) circular pin-fins pattern. (b) NACA0024 airfoil shaped pin-fins pattern.

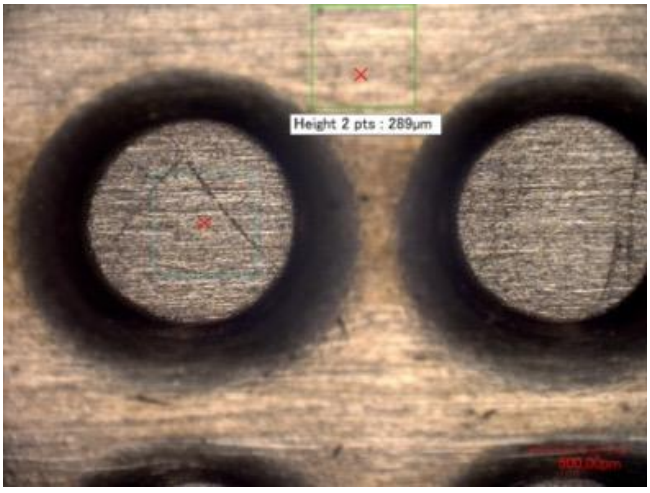


Figure 6.6: A microscopic picture of the measured etching depth of the ~300 µm objective.

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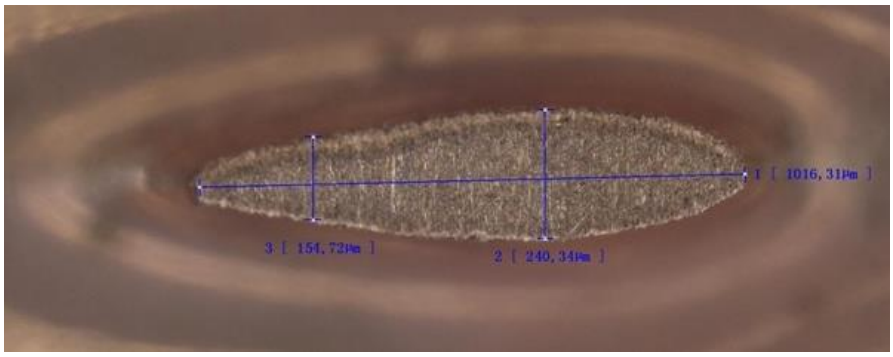
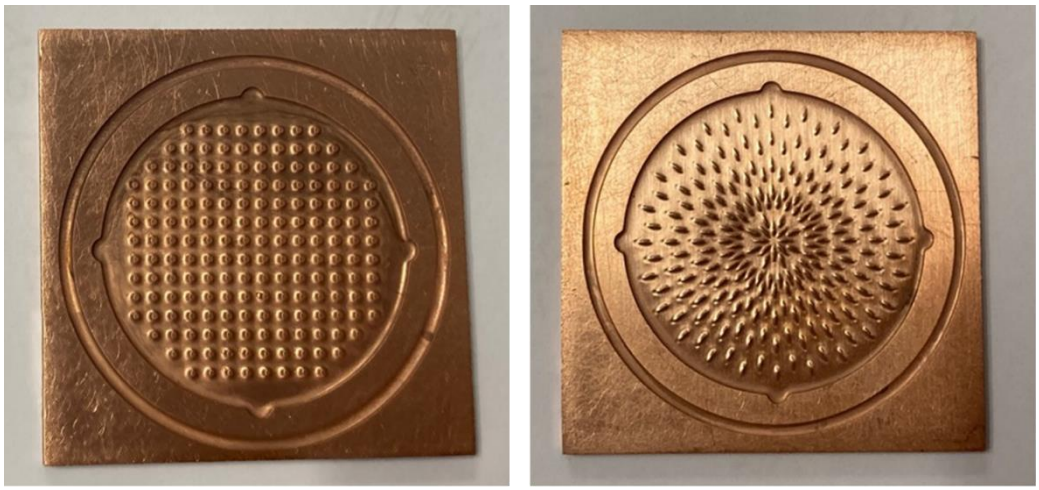


Figure 6.7: A microscopic picture of the measured chord and the thickness of NACA0024 airfoil shaped pin-fins after etching ~300 µm.

Using the same patterns shown in Figure 6.3, two copper plates are chemically etched in order to reach 600 µm as shown in Figure 6.8. For the circular pin-fin the measured diameter is ~650 µm after reaching an etching depth of ~560 µm as shown in Figure 6.9a. For the NACA0024 airfoil shaped pin-fin, the top surface is totally etched as shown in Figure 6.9b.



(a) Circular – etching depth = ~600 µm (b) NACA0024 – etching depth = ~600 µm

Figure 6.8: Copper plates after chemical etching of ~600 µm: (a) circular pin-fins pattern. (b) NACA0024 airfoil shaped pin-fins pattern.

From these results, reaching a 1000 µm etching depth will totally etch the surface of the circular pin-fin of 1.5 mm initial diameter and the airfoil with 2 mm chord length. The larger circular pin-fin pattern with an initial diameter of 2 mm and NACA0024 airfoil shaped pin fin with an initial chord length of 4 mm are considered for 1000 µm etching depth objective as shown in Figure 6.4. Figure 6.10 shows the two copper plates samples after the chemical etching.

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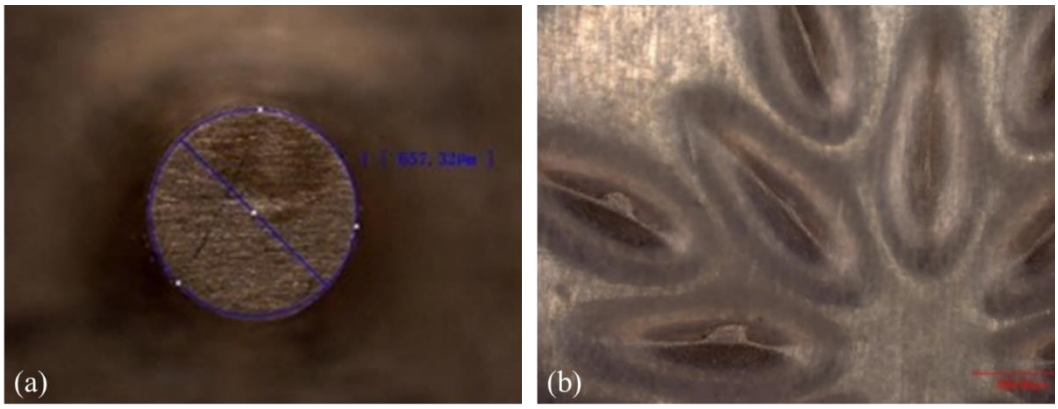

Figure 6.9: (a) a microscopic picture of the measured diameter of the circular pin-fin after etching ~600 µm. (b) a microscopic picture of NACA0024 airfoil shaped pin-fins after etching ~600 µm.

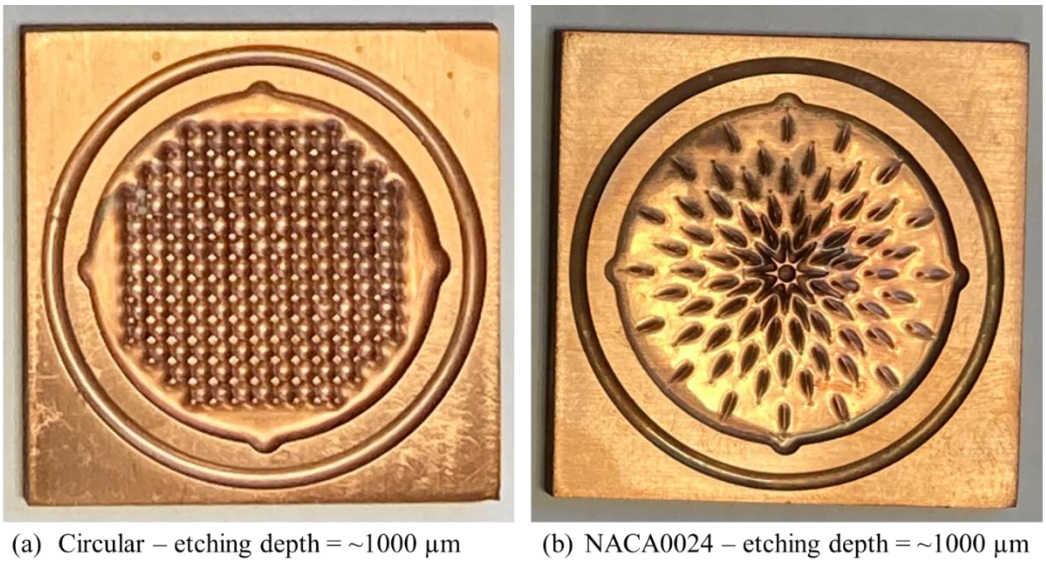

Figure 6.10: Copper plates after chemical etching of ~1000 µm: (a) circular pin-fins pattern. (b) NACA0024 airfoil shaped pin-fins pattern.

In Figure 6.10a, it can be visually noticed that there is an inhomogeneity in the resulting diameter of the circular pin-fins near the edges. Figure 6.11a shows a microscopic picture of the circular pin-fins. The measured resulting diameter after etching is ~500-700 µm. For the airfoil pin-fins, the top surface is totally etched. However, when etching the same airfoil to a ~600 depth, the resulted chord length measured is ~ 1.4 mm compared to 4 mm initially before etching (Figure 6.11b).

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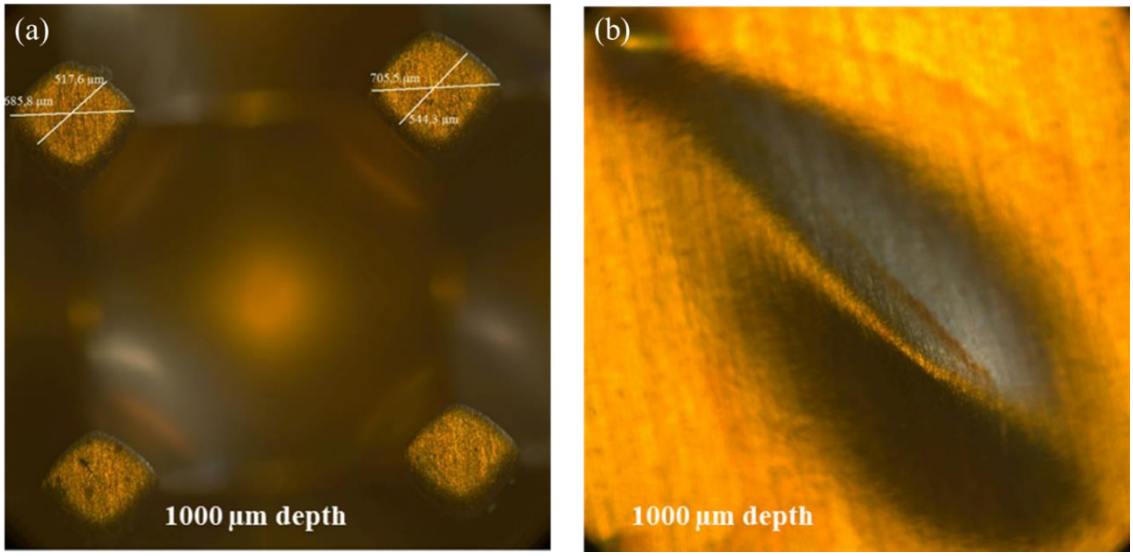

Figure 6.11: (a) a microscopic picture of the measured diameter of the circular pin-fin after etching ~1000 µm. (b) a microscopic picture of NACA0024 airfoil shaped pin-fins after etching ~1000 µm.

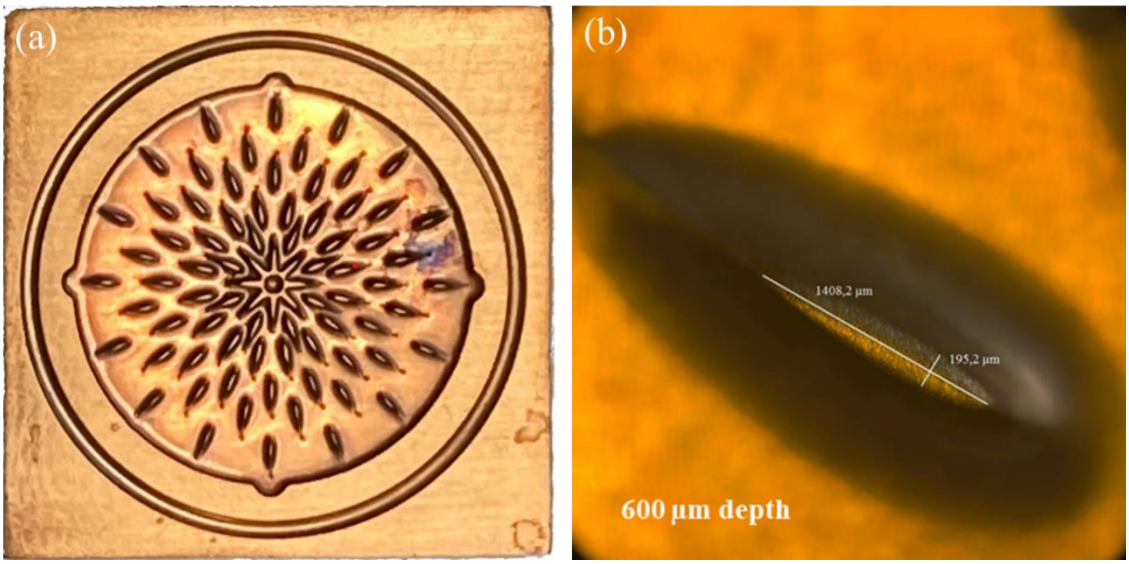

Figure 6.12: (a) a copper plate of NACA0024 airfoil shaped pin-fins pattern after chemical etching of ~600 µm (b) a microscopic picture of NACA0024 airfoil shaped pin-fins after etching ~600 µm.

From the data presented in Table 6.1, the compensation of the lateral etching as a function of the vertical etching depth is estimated. For circular pin-fins, ~500 µm reduction of the pin-fin initial diameter for each ~300 µm etching depth. For NACA0024 airfoil pin-fins, ~1 mm of the chord length is reduced for each ~300 etching depth.

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Table 6.1: First etching trial results.

Shape	Initial pin-fin diameter/chord (mm)	Etching depth objective (µm)	Pin-fin diameter after etching (mm)	Measured etching depth (µm)
Circular	1.5	300	~1	~290
	1.5	600	~0.65	~560
	2	1000	~0.5 – 0.7	~1000
Airfoil NACA0024	2	300	~1	~300
	2	600	-	~600
	4	600	~1.4	~600
	4	1000	-	~1000

In the conclusion of this first trial of etching, the 1000 µm etching depth can be reached with circular pin-fins of large initial diameter (>2 mm) and larger/thicker airfoil with. However, approaching this depth of etching can result in inhomogeneity in circular pin-fin diameter after etching. This can be due to the falling of the photoresist film during etching as a result of the lateral etching of the pin-fins.

6.2.1.2 Second etching trial (final samples)

By considering the measured reduction in the pin-fins shape due to the etching depth achieved, a second batch of samples is prepared by compensating for the expected reduction in the initial shape of the pin-fins pattern. Figure 6.13 shows the three chosen patterns: circular pin-fins with 1.9 mm initial diameter, circular pin-fins with 1.4 initial diameter, and NACA0050 shaped pin-fins with 4 mm initial chord. The spacing between pin-fins edges is 100 µm.

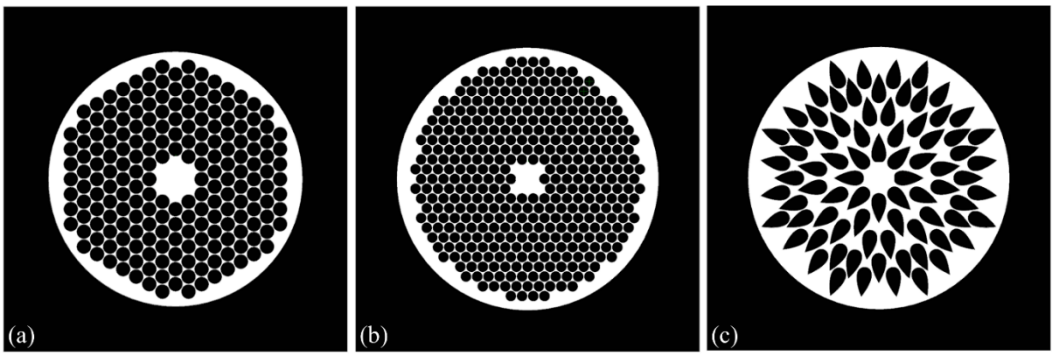

Figure 6.13: Pin-fins patterns for etching: (a) circular pin-fins with 1.9 mm initial diameter. (b) circular pin-fins with 1.4 mm initial diameter (c) NACA0050 airfoil shaped pin-fins with 4 mm initial chord.

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The objective is to reach an etching depth of 1000 µm. However, the etching depth is first chosen at ~500 µm in order to produce a homogenous etching throughout the whole copper plate.

The rate of etching depends on the concentration and the freshness of the etchant. Just before this second trial the old etcher was replaced by a fresh one which resulted in faster etching but also changed the ratio between lateral and vertical etching compared with the first trial.

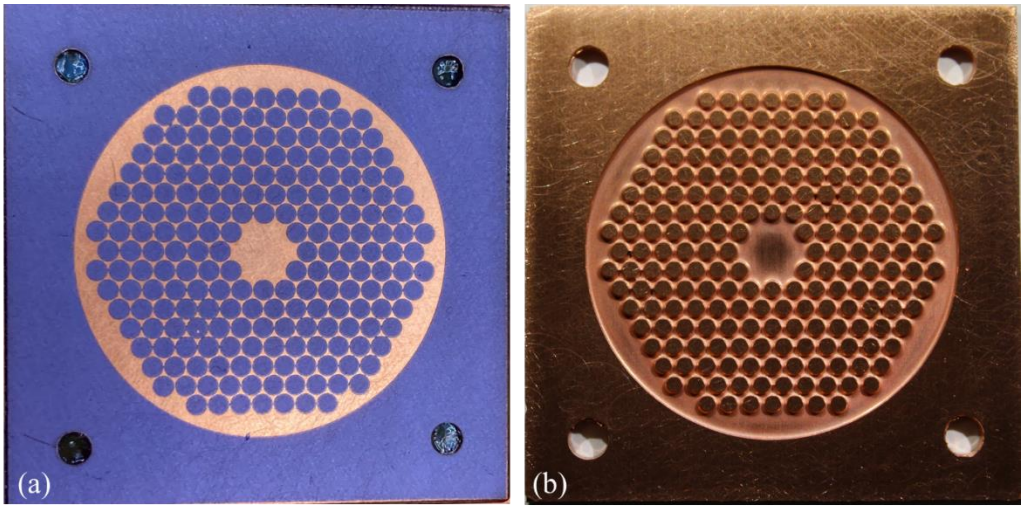

Figure 6.14: Circular pin-fins with 1.9 mm initial diameter: (a) copper plate sample with the developed photo resist film before etching. (b) copper plate sample after etching ~500 µm.

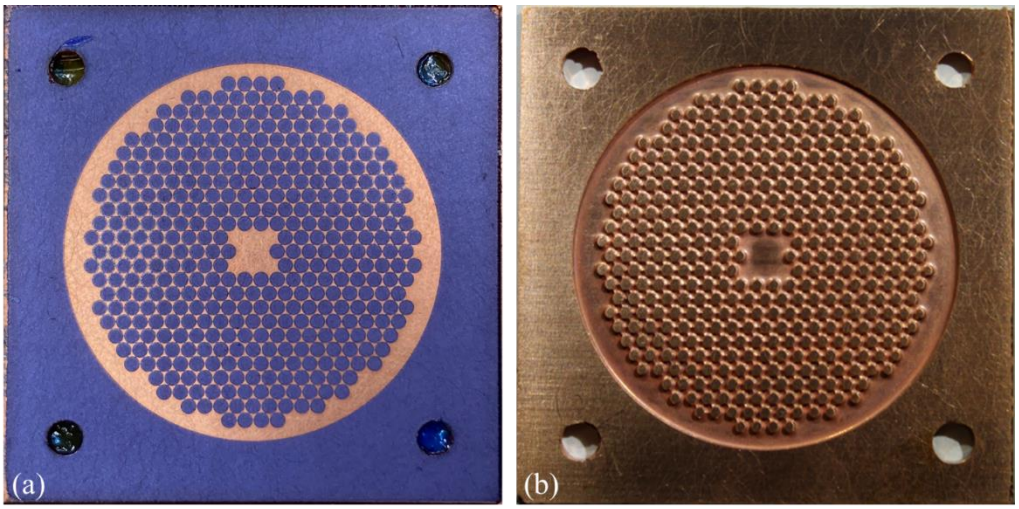

Figure 6.15: Circular pin-fins with 1.4 mm initial diameter: (a) copper plate sample with the developed photo resist film before etching. (b) copper plate sample after etching ~500 µm.

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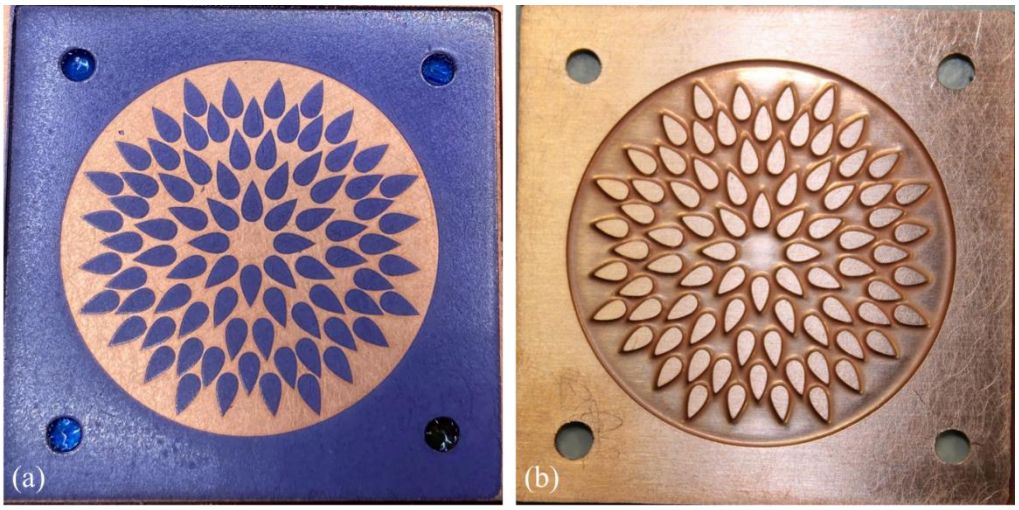

Figure 6.16: NACA0050 airfoil shaped pin-fins with 4 mm initial chord: (a) copper plate sample with the developed photo resist film before etching. (b) copper plate sample after etching ~500 µm.

Figure 6.14a, Figure 6.15a, and Figure 6.16a show the copper plate covered by the photoresist film before etching while Figure 6.14b, Figure 6.15b, and Figure 6.16b shows the copper plate heat sink after the chemical etching process with an etching depth of ~500 µm. The form of the circular pin-fins resulted from chemical etching is shown in Figure 6.17, which takes the form of a conical shape. This form is considered for the CAD modeling of the pin-fins in simulations.

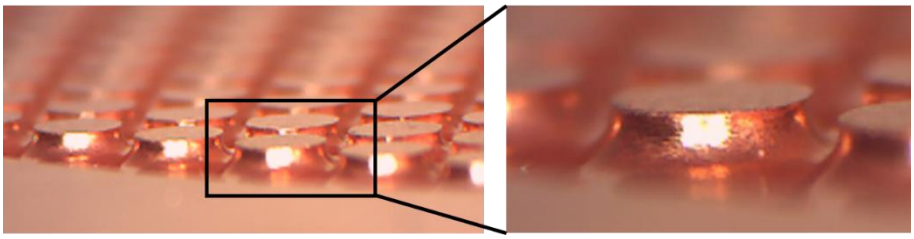

Figure 6.17: The form of the circular pin-fins resulted from chemical etching.

Figure 6.18 shows microscopic pictures of the circular pin-fins with 1.9 mm initial diameter indicating the measured diameter of the pin-fins resulted from the chemical etching process. 300 – 400 µm is reduced from the initial diameter during etching. The circular pin-fins with 1.4 mm initial diameter are showing the same amount of reduction in the initial diameter (Figure 6.20). The etching depth is measured at 400 – 600 µm as shown in Figure 6.19 and Figure 6.21. For NACA0050 airfoil shaped pin-fins, the measured thickness is reduced by ~300 µm while the chord is reduced by ~500 µm due to the sharp angle at the airfoil tale (Figure 6.22 and Figure 6.23). Table 6.2 summarizes the etching results of the second trial. Note that these measurements are also helpful for modeling these patterns of pin-fins for the simulations.

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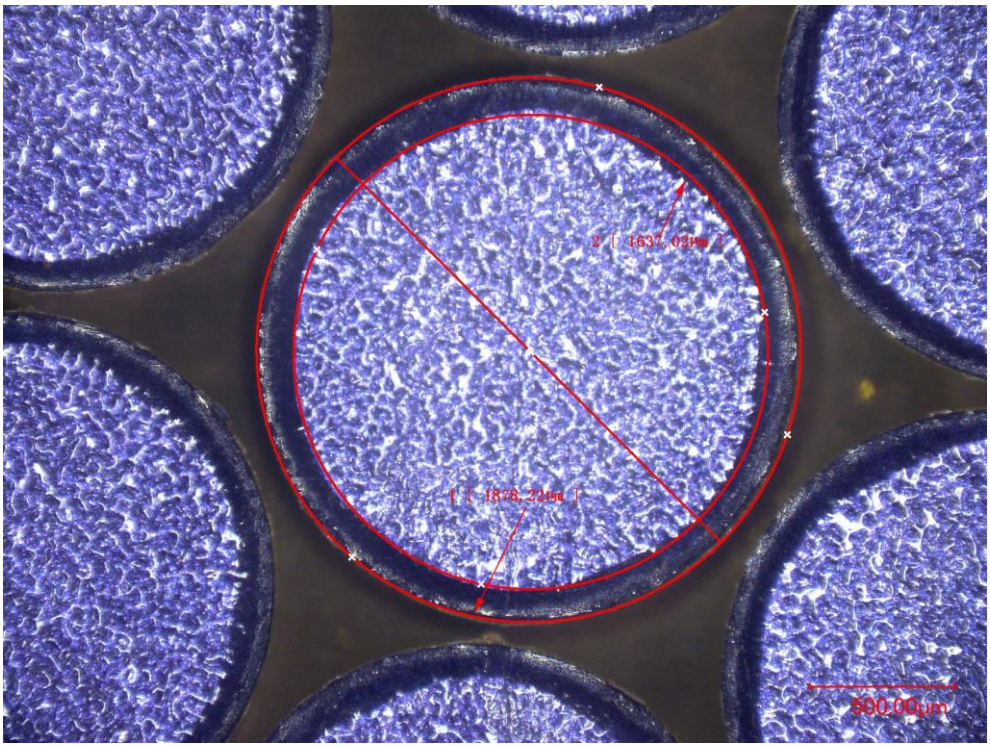

Figure 6.18: The measured diameter after etching of a circular pin-fin with an initial diameter of 1.9 mm for the ~500 µm objective. Around 300 - 400 µm reduction in the diameter.

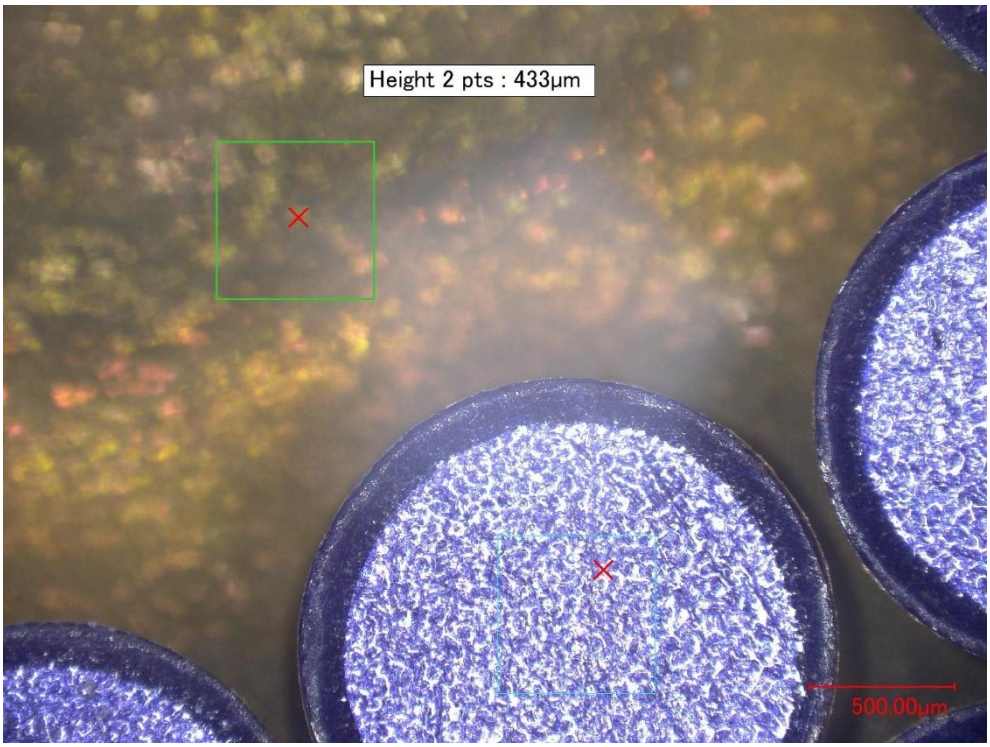

Figure 6.19: The measured etching depth of a circular pin-fin pattern with an initial diameter of 1.9 mm for the ~500 µm objective.

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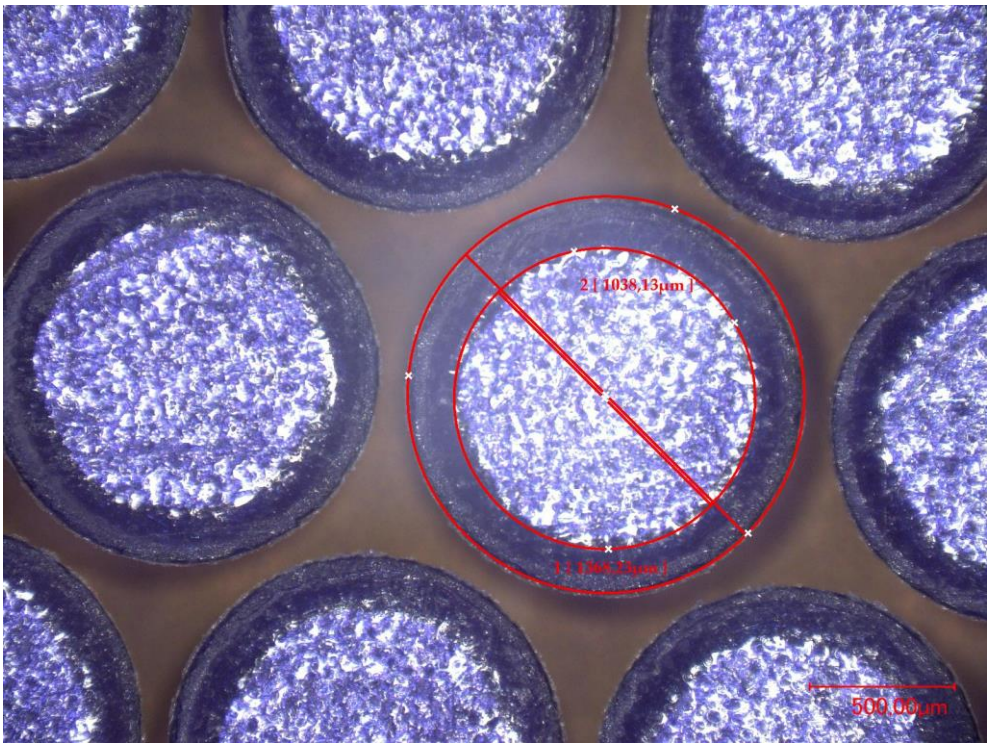

Figure 6.20: The measured diameter after etching of a circular pin-fin with an initial diameter of 1.4 mm for the ~500 µm objective. Around 300 - 400 µm reduction in the diameter.

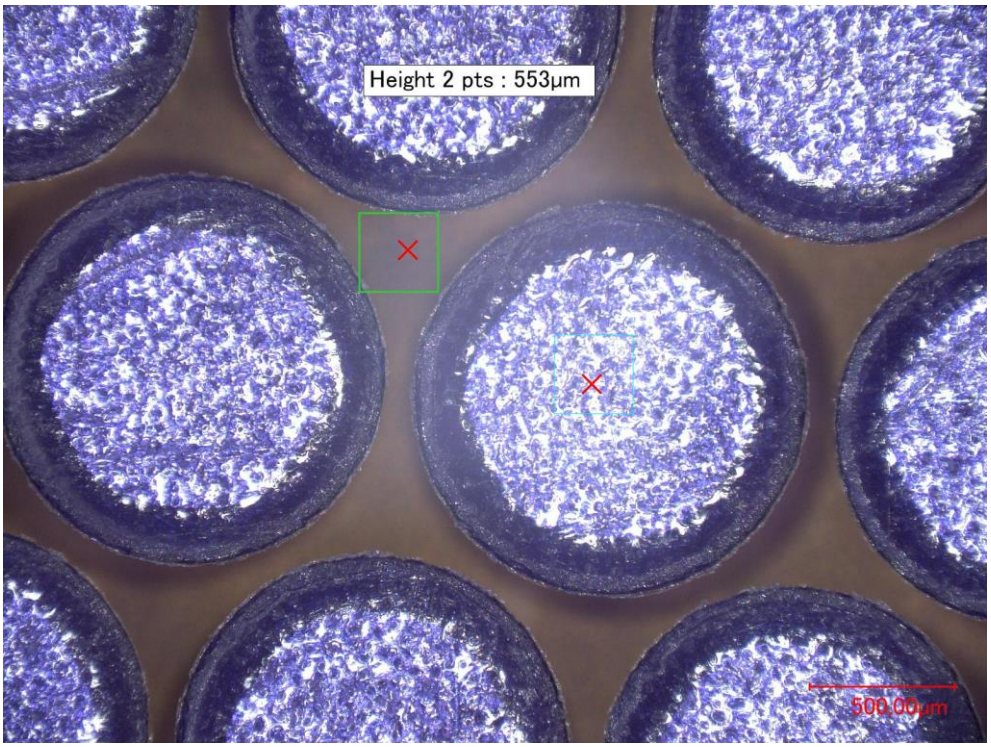

Figure 6.21: The measured etching depth of a circular pin-fin pattern with an initial diameter of 1.4 mm for the ~500 µm objective.

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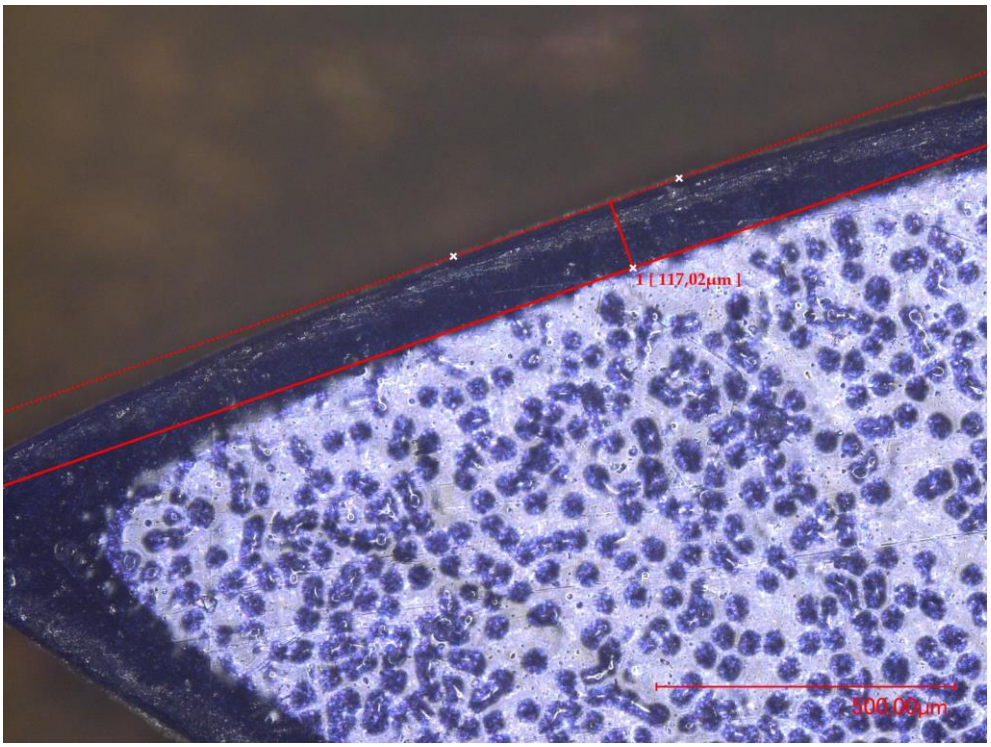

Figure 6.22: The measured reduction in NACA0050 pin-fin thickness after etching with an initial chord of 4 mm for the ~500 µm objective. Around ~300 µm reduction in the total thickness.

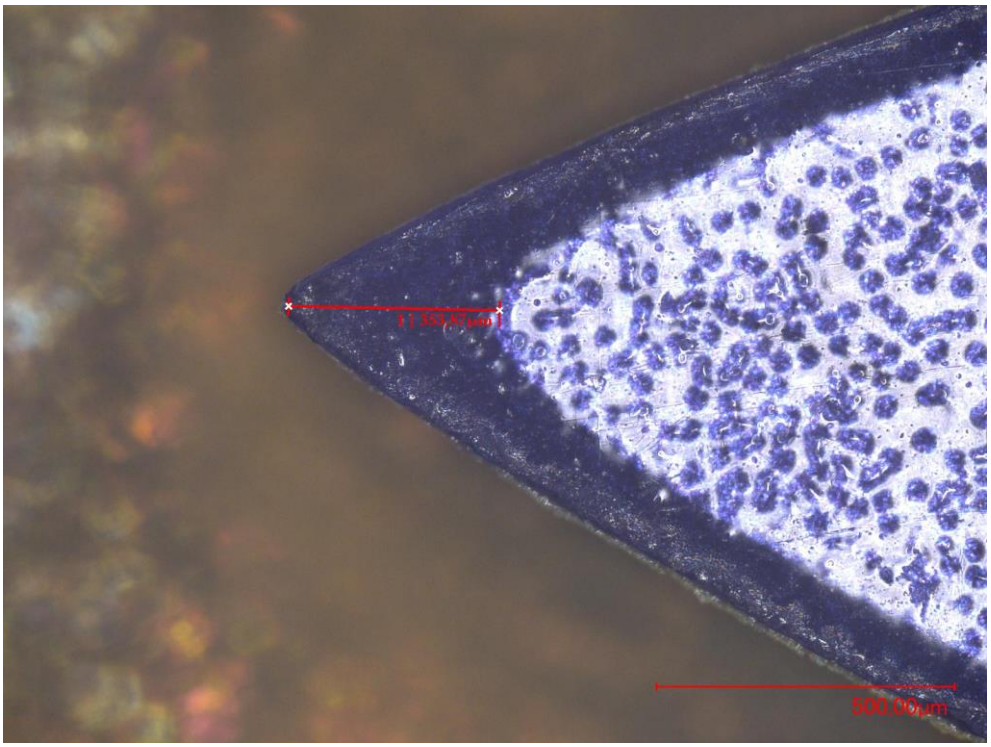

Figure 6.23: The measured reduction in NACA0050 pin-fin chord after etching with an initial chord of 4 mm for the ~500 µm objective. Around ~500 µm reduction in the total chord.

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The objective is to reach an etching depth of 1 mm (1000 µm). However, when trying to achieve etching beyond the 700 µm, the photosensitive film starts falling off the pin-fins which can result in etching the whole pin-fins away. In addition, the final etching depth when measuring at several locations is different.

Table 6.2: Second etching trial results.

Shape	Initial pin-fin diameter/chord (mm)	Etching depth objective (µm)	Pin-fin diameter/chord after etching (mm)	Measured etching depth (µm)
Circular	1.9	500	~1.6 – 1.5	~430
Circular	1.4	500	~1.1 – 1	~550
NACA0050	4	500	~3.5	~500

In the conclusion of etching, the 500 µm etching depth is successfully achieved. From the data presented in Table 6.2, the compensation of the lateral etching as a function of the vertical etching depth is estimated. For circular pin-fins, ~300-400 µm reduction of the pin-fin initial diameter for each ~500 µm etching depth. For NACA0050 airfoil pin-fins, ~0.5 mm of the chord length is reduced for each ~500 etching depth.

6.2.2 PCB lamination with the pin-fin heat sink

Lamination is an essential process in PCB manufacturing where the stack of several layers of copper and prepreg (epoxy) are pressed under high pressure and temperature. Here, this lamination process is used to attach the PCB samples to the copper plate using an epoxy-based prepreg (Rogers 92ML) as shown in Figure 6.24. This prepreg layer is 60 µm-thick after lamination and it has a thermal conductivity of 2.5 W/(m.K) which is about 8 times higher than the standard FR4 used in the fabrication of the PCB (0.3 W/(m.K)). It also provides the electrical isolation needed to isolate the PCB from the cooling water.

To perform the lamination with a uniformly distributed pressure, a conformable release sheet (Pacothane plus) is used on the top and the bottom of the stack as shown in figure. In addition, two aluminum plates are used to contain the stack and to ensure the proper alignment of the laminated plates and layers. The steps of the stack-up are shown in Figure 6.25.

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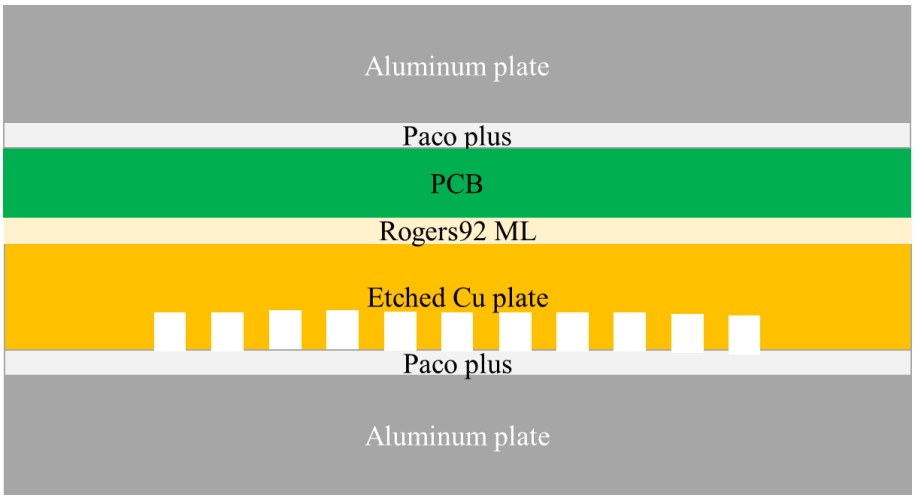

Figure 6.24: A schematic of the stack-up for the lamination process.

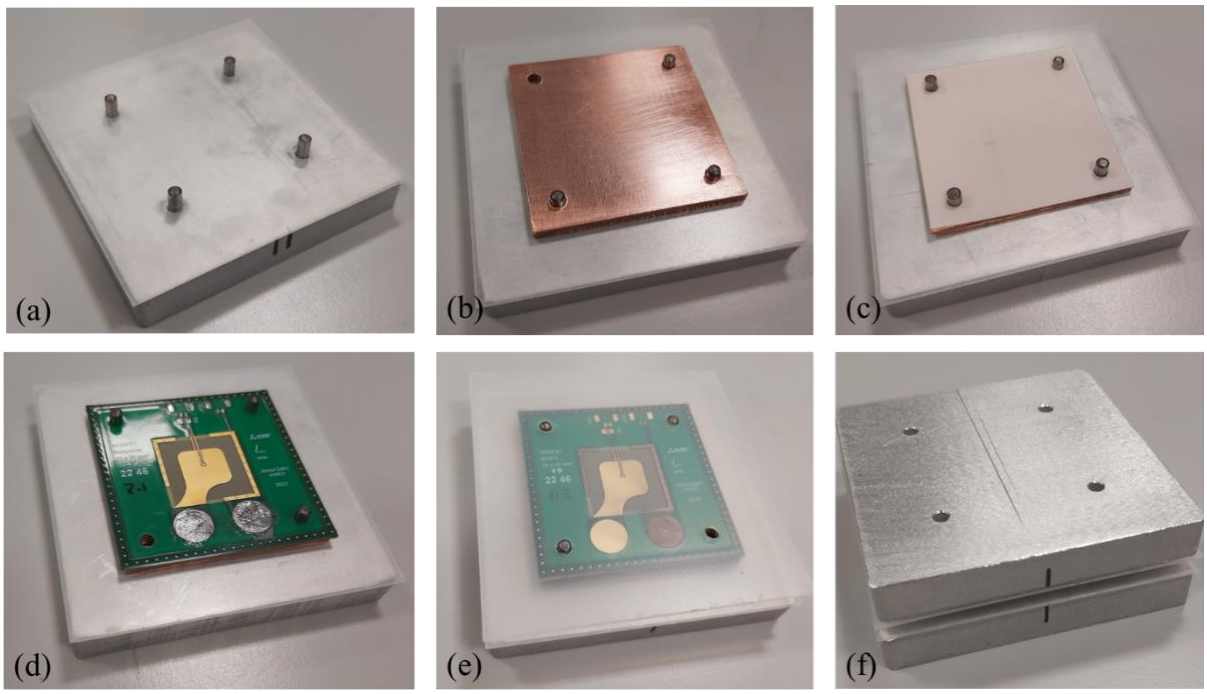

Figure 6.25: Stack-up steps: (a) placing the bottom conformable release sheet on the bottom aluminum plate. (b) placing the etched copper plate. (c) placing the prepreg layer. (d) placing the PCB. (e) placing the top conformable release sheet. (f) placing the top aluminum plate to contain the stack-up.

The stack-up is then placed in a press (Figure 6.26) which control the pressure and the temperature throughout a pre-programmed pressure and temperature profile. (which is based on the processing guidelines for Rogers 92ML prepreg. At the heating phase, the temperature is increased with a rate of 3°C/min up to 185°C. the temperature stays at 185°C for 90 minutes before starting the cooling down phase. During the heating phase, a pressure of 27.58 bar (400 PSI) is applied when the temperature reaches 100°C and maintained until the end of the cooling down. This pressure corresponds to 0.6 ton given the surface area of the PCB, the prepreg, and

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the copper plate (46×46 mm²). However, the minimum setting on the pressing machine is 1 ton. Hence, 1 ton is applied (45.97 bar). Figure 6.27 shows the pressure and temperature profiles of the lamination process.

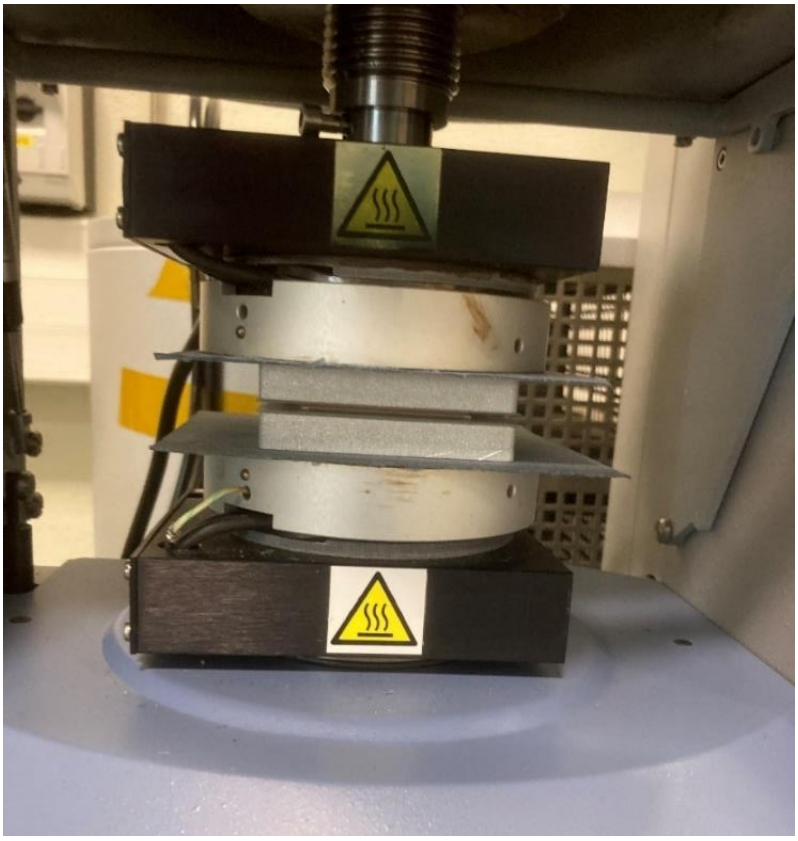

Figure 6.26: The stack-up placed in the press.

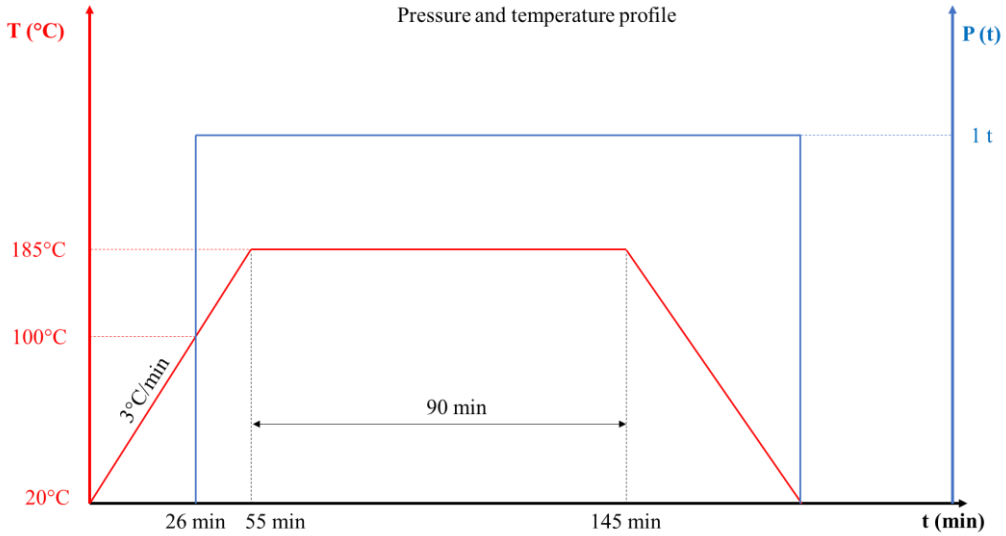

Figure 6.27: Pressure and temperature profiles of the lamination process.

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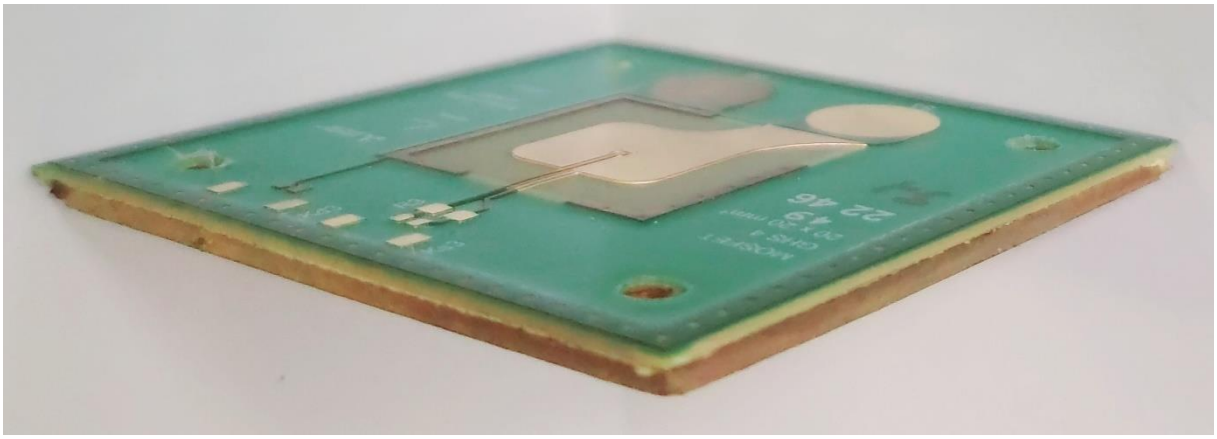

Figure 6.28: The PCB sample laminated with etched copper pin-fin heat sink.

After the lamination process, the PCB and the etched copper plate become one part with an isolation interlayer as shown in Figure 6.28. Note that in its principle, the etching of the copper plate and its lamination can be performed during the fabrication of the PCB itself, as it consists in the same processes. Therefore, we produce a PCB with its heat sink all in one part to be assembled with a water manifold of the jet impingement cooling system.

It should be noted that during the lamination process, the PCB variants with embedded graphite heat spreaders without distributed micro vias all over the spreading area (M22Gb & M22Gc) have suffered from swelling. On the other hand, the PCB variants with graphite and distributed micro vias (M22Ga) have successfully been laminated. This proves the necessity of the distribution of micro vias all over the spreading area to prevent defoliation of the graphite, as explained previously in chapter 5 section 5.3.2.

Note that the etched copper plate with NACA0050 airfoil shaped pin-fins has been laminated with the M22Gb PCB variant which exhibits swelling issues, and therefore cannot be used for measurement. Consequently, the thermal measurements below only consider the circular pin-fins pattern with an initial diameter of 1.4 mm (Figure 6.15).

6.2.3 JIC water manifold

The water manifold manages the circulation of the cooling water from the inlet to the exit allowing the heat exchange between the water and the surface of the etched copper pin-fins heat sink. The water manifold also prevents water leakage during operation. This section presents the modelling, design, and fabrication of the JIC water manifold, to be assembled with the PCB/Cu pin-fins heat sink.

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6.2.3.1 Modelling

The objective here is to design a compact JIC water manifold that ensures the impingement of the water jet to the heat exchange surface with a low pressure drop and high thermal performance. Figure 6.29 and Figure 6.30show the CAD model of the designed JIC water manifold.

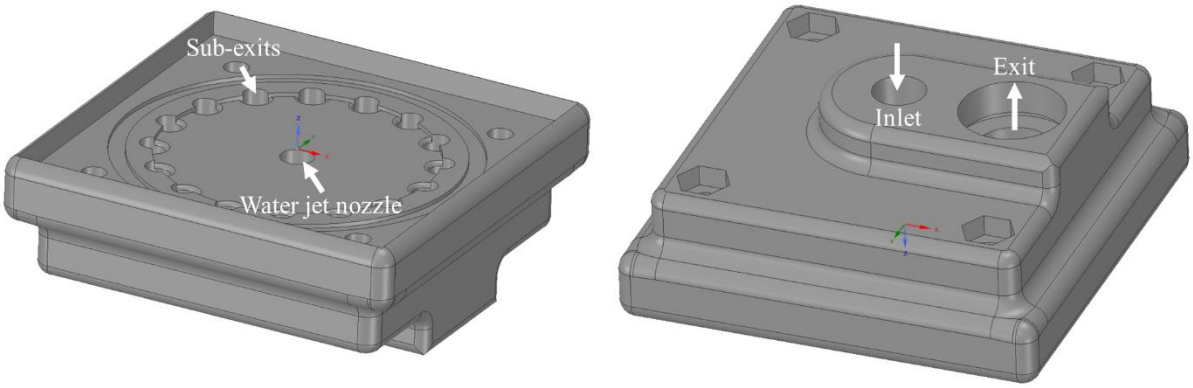

Figure 6.29: The JIC water manifold CAD model.

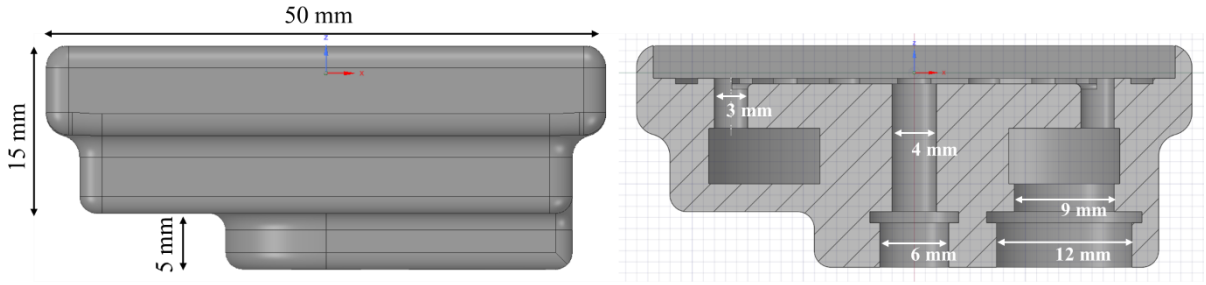

Figure 6.30: A cross-section of the JIC water manifold CAD model.

The manifold size is 50×50×15 mm^3 with an extension of 5 mm in height to contain the water tubes for the inlet and the exit. The water enters through one inlet leading to the jet nozzle with constant 4 mm diameter. The water then diffuses radially and exits through 16 radially distributed sub-exits (3 mm of diameter for each sub-exit). These sub-exits lead to a cavity where the water is collected to exit the manifold through an exit with a diameter of 9 mm. This design is based on a parametric study presented in the next subsection. A principal groove is made for an O-ring, to ensure proper sealing between the manifold and the heatsink. The JIC water manifold is assembled to the PCB/Cu pin-fins heat sink by four M3 screws.

6.2.3.2 Parametric study

In this study, the effective HTC and the water pressure drop of the combination of the copper pin-fins heat sink and the water manifold are calculated by CHT simulations. In this CHT simulation, the height of the pin-fins is varied from 0 mm (no pin-fins) to 1 mm (as the objective

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was) passing by the 0.5 mm which is the successfully etched one. The pin-fin is circular with a 1 mm diameter. The inlet diameter of the manifold is varied between 2 mm, 4 mm, and 6 mm. The number of sub-exits is varied between 4, 8, and 16. This is to study the impact of these two parameters on the pressure drop and the effective HTC.

Figure 6.31 shows the CHT simulation CAD model with the boundary conditions. One can see the solid domains (water manifold and copper pin-fins heat sink) and the fluid domain (water). The heat (100 W) is assigned on a surface of 20×20 mm² which is the spreading area of the PCB. A natural convection boundary condition (constant heat transfer coefficient of 10 W/(m².K)) is assigned on the outer surfaces of the manifold. A uniform water velocity is assigned at the inlet of the manifold and a uniform atmospheric pressure at the exit.

For these simulations, the k-ε turbulence model is used, since it is faster than the SST model that is used in the rest of the simulations in this chapter (SST is more accurate but slower). Due to the symmetry of the manifold, only half of the model is considered for the CHT simulation to reduce computational time (Figure 6.31b).

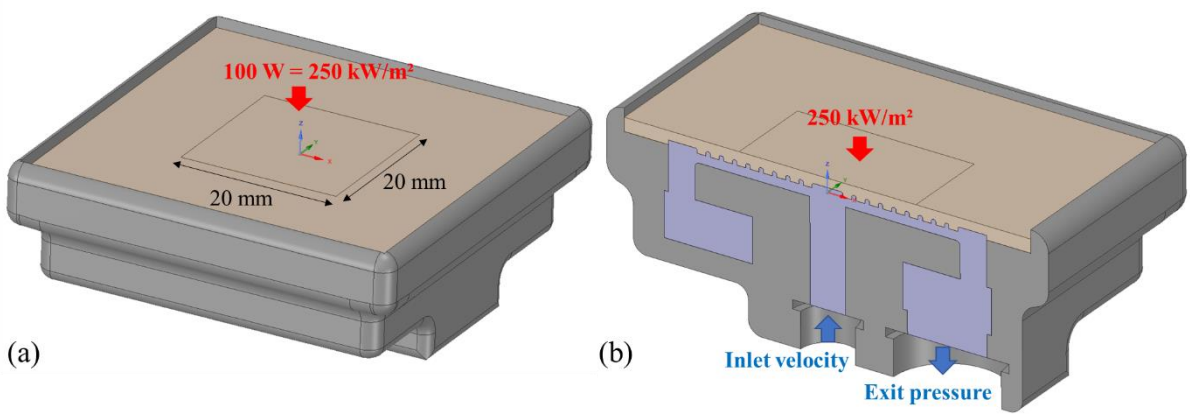

Figure 6.31: The CHT simulation CAD model. (a) Full model. (b) Half model.

Table 6.3 shows the effective HTC and the pressure drop at various parameters at a volumetric flow rate of 1.5 L/min (inlet velocity = ~2 m/s at 4 mm inlet diameter). The effective HTC is calculated between the average temperature of the heating surface of 20×20 mm² and the water inlet temperature of 22°C. the pressure drop is calculated from the difference between the total pressure at the inlet and the atmospheric pressure at the outlet. At 1.5 L/min, 4 mm inlet diameter, 16 sub-exits, and pin-fins height of 0.5 mm, Figure 6.32 shows the temperature contour while Figure 6.33 shows the streamlines of velocity circulating through the water manifold.

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Table 6.3: The HTC and the pressure drop at various parameters.

Inlet diameter (mm)	No. of sub-exits	Pin-fins height (mm)	Turbulence model	Effective HTC (W/(m².K))	ΔP (kPa)
2	16	0.5	KE	34406.8	36.96
4	**16**	**0.5**	**KE**	**24220.1**	**3.38**
6	16	0.5	KE	20743.4	1.21
4	**8**	0.5	KE	24347.5	3.51
4	**4**	0.5	KE	24813.9	3.89
4	16	**0 (No fins)**	KE	19004.2	2.53
4	16	**1**	KE	30102.3	3.11
4	**16**	**0.5**	**SST**	**35186.5**	**3.56**

As shown in Table 6.3, the pressure drop increases significantly when setting the inlet diameter at 2 mm (about 11 times larger than for an inlet diameter of 4 mm). However, at 2 mm, the water jet hits the surface at higher velocity, which leads to an increase in the effective HTC (30 % more than for a 4 mm inlet diameter). At 6 mm inlet diameter, the pressure drop is 2.8 times lower, but with 15 % lower effective HTC. The 4 mm inlet diameter is chosen for the best compromise. Regarding the number of sub-exits, no significant impact on the effective HTC is observed. However, the pressure drop decreases by increasing the number of sub-exits. The number of sub-exits is chosen to be 16.

For the height of the pin-fins, increasing the height increases the total heat exchange surface, which leads to an increase in the effective HTC. Increasing the height of the pin-fins to 1 mm can increase the effective HTC by 20 % compared to 0.5 mm. On the contrary, having no pin-fins at all yields a 20% lower HTC. A pin-fin heigh of 0.5 mm is chosen since it is the etching depth that can be reached safely as mentioned previously in section 6.2.1.2.

Since the SST turbulence model is more accurate, a comparison is made by using it for one simulation. As shown in the table, the k-ε model underestimates the effective HTC by around 32 % compared to the SST model. The difference in pressure drop is only 5 % between the two turbulence models. For the rest of the CHT simulations in this chapter, the SST turbulence model is used.

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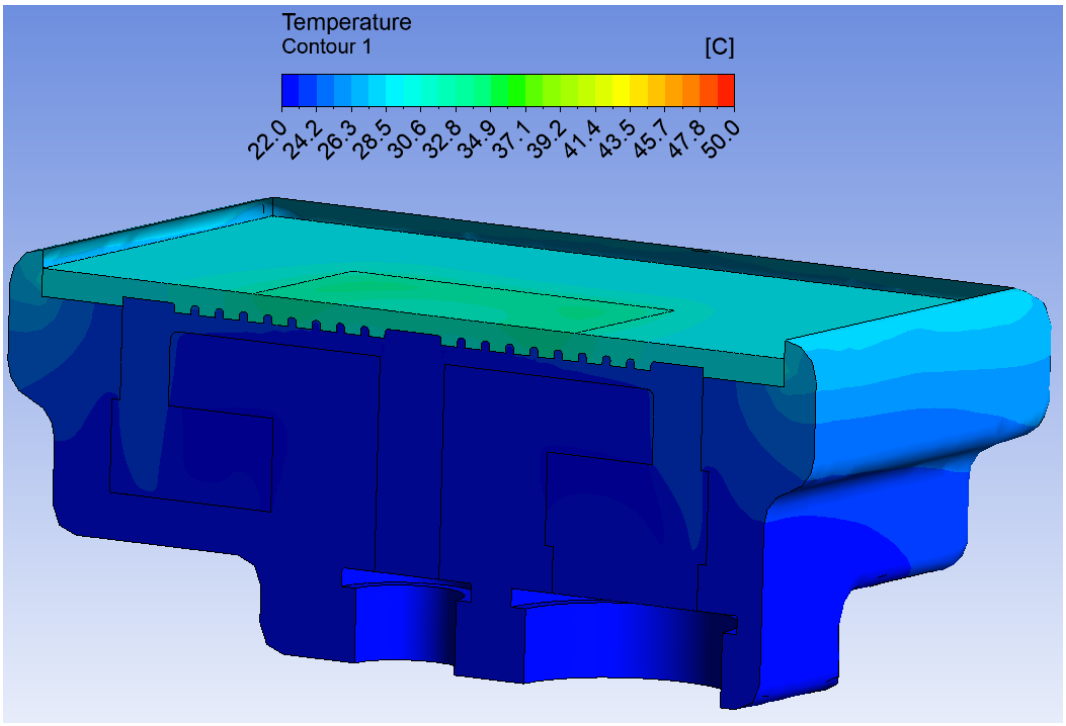

Figure 6.32: The temperature contour at 1.5 L/min, 4 mm inlet, 16 sub-exits, and pin-fins height of 0.5 mm.

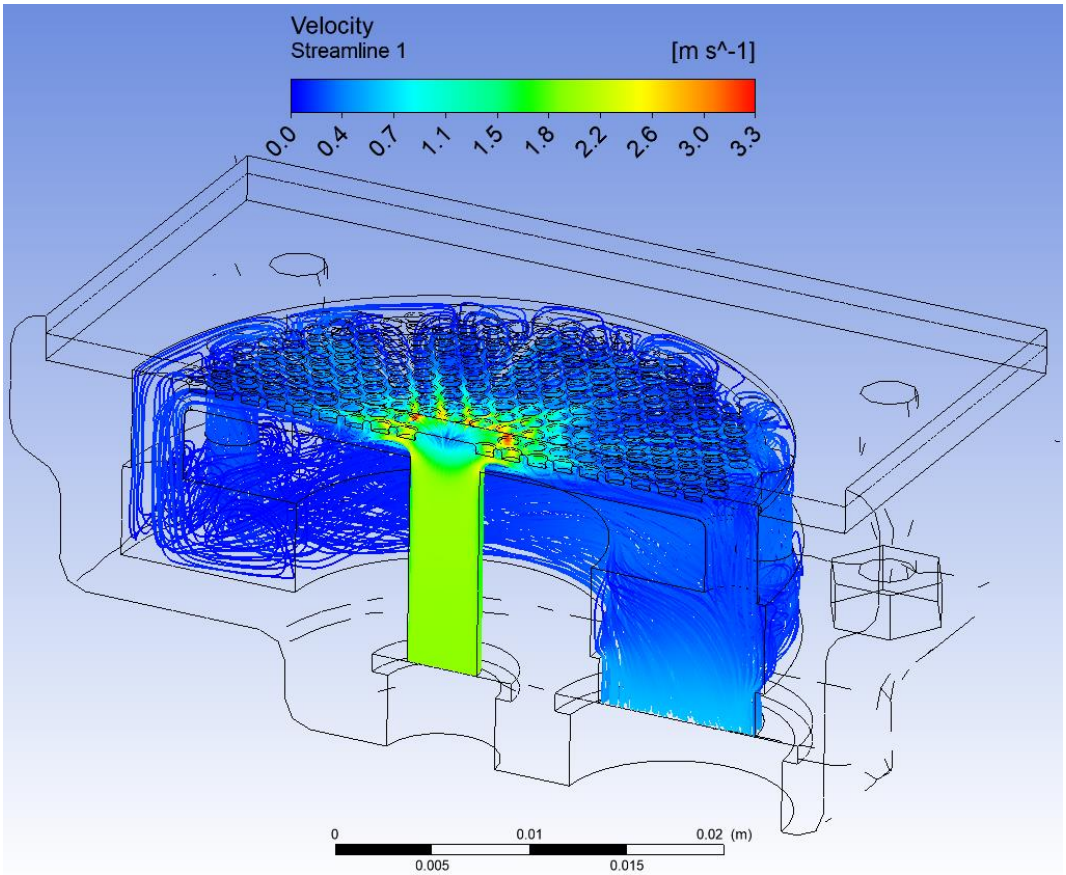

Figure 6.33: The velocity streamlines at 1.5 L/min, 4 mm inlet, 16 sub-exits, and pin-fins height of 0.5 mm.

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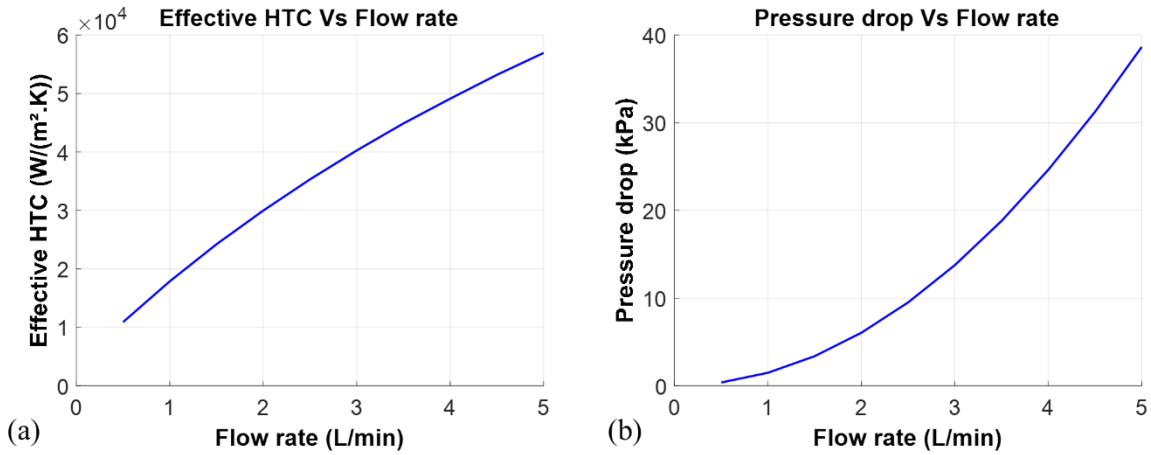

Figure 6.34: (a) the effective HTC versus flow rate. (b) the pressure drop versus flow rate. At, 4 mm inlet, 16 sub-exits, and pin-fins height of 0.5 mm

Figure 6.34 shows the effective HTC and pressure drop of the JIC as a function of the water volumetric flow rates in the range from 0.5 L/min up to 5 L/min. The higher the flow rate, the higher the achieved effective HTC and the pressure drop.

6.2.3.3 Fabrication by additive manufacturing

The JIC water manifold is fabricated using 3D printing by selective laser sintering (SLS) which is an additive manufacturing technique. This fabrication technique uses a laser beam as a heat source in order to sinter some powdered material to form a 3D object. The locations at which the laser is aimed at is defined by the 3D CAD model. Figure 6.35 shows the JIC water manifold after fabrication by the SLS technique, using powdered Nylon (PA12).

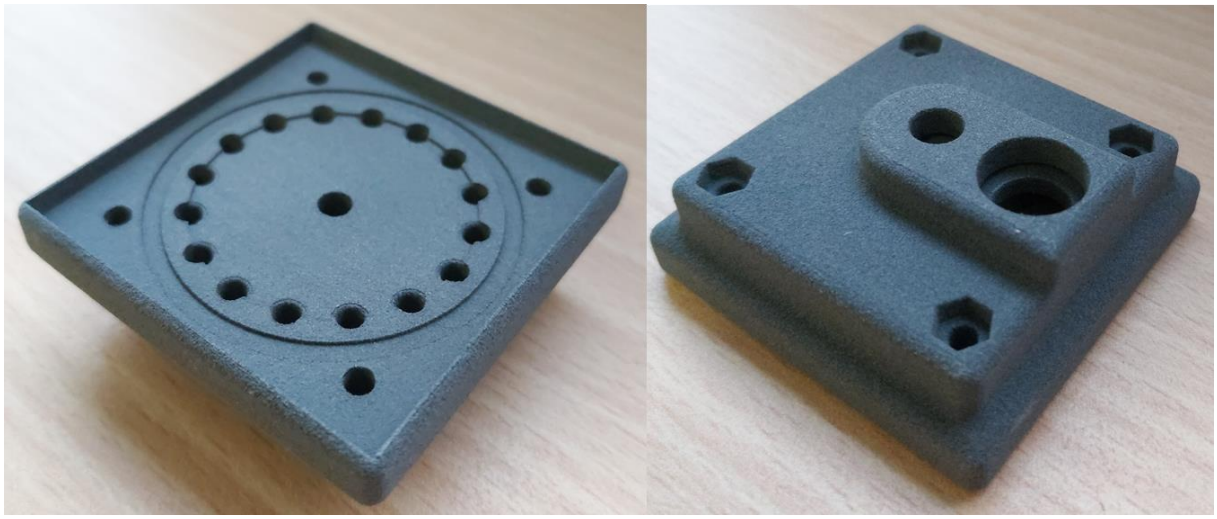

Figure 6.35: JIC manifold fabricated by using the SLS method.

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6.3 Assembly of PCB/copper pin-fins/water manifold

In this section, the copper pin-fins heat sink laminated with the PCB variants (with and without graphite), and assembled all together with the JIC water manifold, is simulated and validated by experimental measurements. The thermo-hydraulic performance is assessed by obtaining the R_{thJA} and the pressure drop for a range of water volumetric flow rates.

6.3.1 CHT simulations

6.3.1.1 Modelling

Figure 6.36 shows the CAD model of the half of the model prepared for the CHT simulations. Compared with the structure presented in Figure 6.31, the power dissipation is no longer considered to be uniformly distributed over the spreader area: here, the heat is generated internally in a volume within the SiC chip as explained in section 3.3.3 in order to avoid making any assumption about the direction of the heat flux. However, for these simulations using ANSYS CFX solver, a hot spot with unrealistic temperature value appears on that volume if its thickness is kept at 20 µm as before in the simulations using ANSYS Mechanical. As a workaround, in the simulations presented below, the power dissipation is considered to occur within the entire volume of the SiC chip rather than in its top 20 µm. A total heat of 25 W is generated internally for the full model.

For the boundary conditions, a natural convection constant (10 W/(m².K)) is assigned on the outer surfaces of the manifold and the PCB top surfaces. Uniform water velocity is assigned at the inlet of the manifold and an atmospheric pressure is assigned at the exit. The SST turbulence model is used for these simulations. The R_{thJA} is calculated based on the difference between the maximum temperature of the SiC chip and the inlet temperature of the water (22°C).

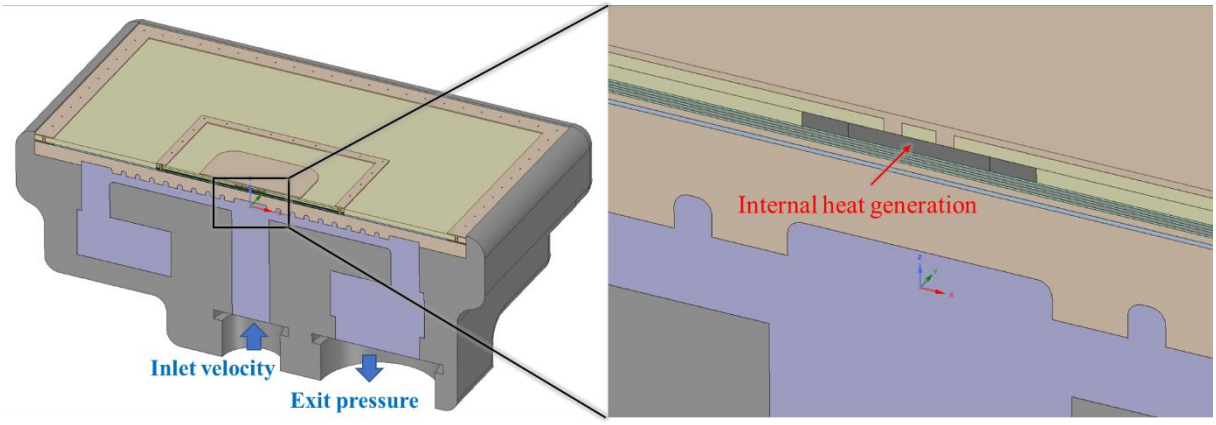

Figure 6.36: The CHT simulation CAD model.

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6.3.1.2 Thermal performance

For the CHT simulation, the PCB variant with graphite used is M22Gc which has no distributed micro vias over the spreading area. The reason for using M22Gc instead of M22Ga (with distributed micro vias over the spreading area), used in the experiment, is to reduce the computational time since both M22Ga and M22Gc showed only a difference of 5 % in R_{thJA} as presented previously in chapter 4 section 4.2.7.1.

Figure 6.37a shows the R_{thJA} of the PCB variant without graphite (M22R) and the PCB variant with graphite (M22Gc) as a function of the water volumetric flow rate varying from 0.5 L/min up to 2.5 L/min (2.5 L/min is the upper limit for the pump used in our experiments). The reduction in R_{thJA} achieved by embedding graphite is about 40 % at 2.5 L/min (from 2.83 K/W down to 1.7 K/W). With 1.7 K/W R_{thJA}, the PCB package with graphite can reach a power loss density of 864 W/cm² (90 W) without exceeding the junction temperature limit of 175°C. Increasing the flow rate from 0.5 L/min to 2.5 L/min reduces the R_{thJA} by only 4.7 % for the M22R PCB variant without graphite. For the M22Gc PCB variant with graphite, the effect of increasing the water flow rate is slightly higher (the reduction is 6.2 %). This is despite the corresponding effective HTC range of ~16000 – 43000 W/(m².K), calculated at Rogers92ML/Cu heatsink interface, for the water flow rate range (0.5 – 2.5 L/min). By referring also to Figure 6.1, this suggests that at this scale of effective HTC, the convection heat transfer is not the main contribution to the R_{thJA}. Figure 6.37b shows the increase in the pressure drop when increasing the water flow rate from 0.5 L/min up to 2.5 L/min. The maximum pressure drop estimated by simulation is 9.87 kPa at 2.5 L/min.

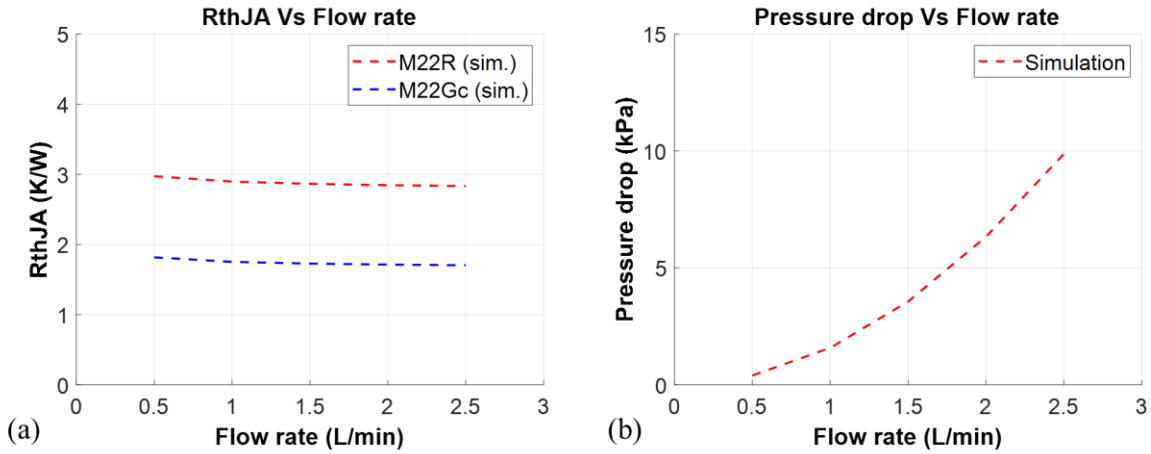

Figure 6.37: CHT simulations (a) the R_{thJA} versus flow rate. (b) the pressure drop versus flow rate.

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Figure 6.38 and Figure 6.39 show the temperature fields of the JIC with the M22R PCB variant without graphite while Figure 6.40 and Figure 6.41 show the temperature fields of the JIC with the M22Gc PCB variant with graphite. The velocity streamlines are shown in Figure 6.42.

Since the height of the pin-fins is only 0.5 mm, the impact of the shape or even not having pin-fins is not very significant. CHT simulations are performed without pin-fins (just a copper plate with a flat surface). At 2.5 L/min, the R_{thJA} is higher by only 3.2 % when removing the circular pin-fins (from 1.705 K/W to 1.762 K/W) for PCB variants with graphite. For the PCB variant without graphite, the difference is even smaller, as R_{thJA} only increases by 1.8 % when removing the pin-fins (from 2.833 K/W to 2.884 K/W). The reduction in pressure drop is more significant, at 8.5 %. This suggests that at this scale of pin-fins, the shape or the presence of pin-fins is not very significant.

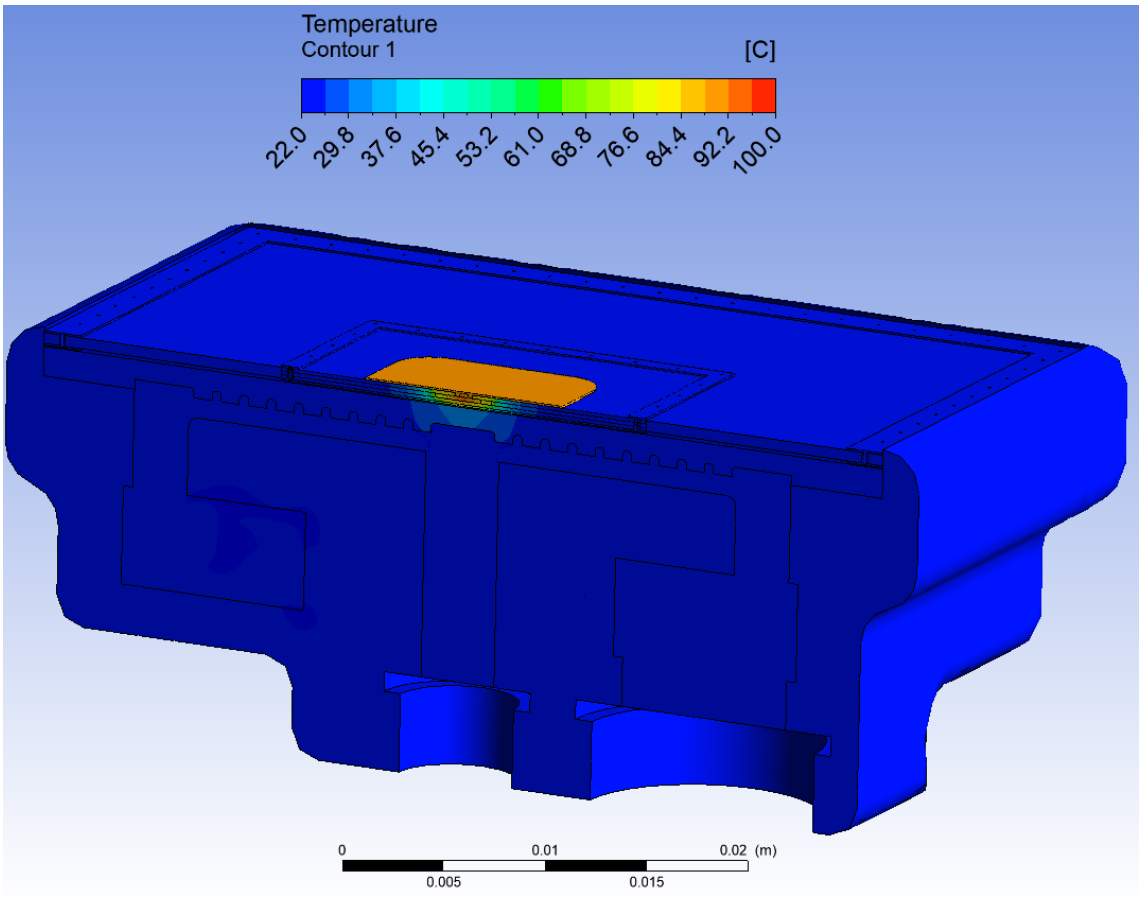

Figure 6.38: Temperature contour of the JIC with the M22R PCB cross-section without graphite for a 25 W dissipation at the chip level.

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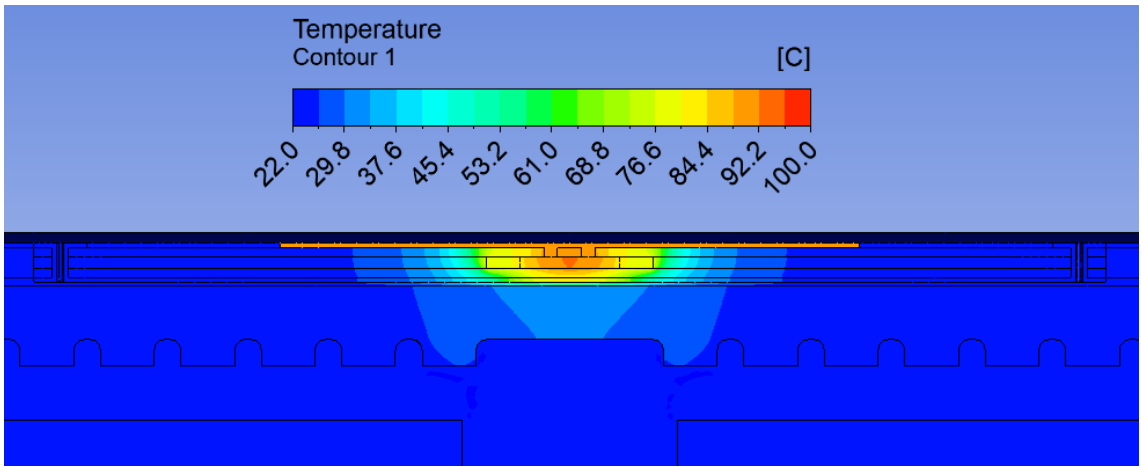

Figure 6.39: Temperature contour of the JIC with the M22R PCB cross-section without graphite for a 25 W dissipation at the chip level.

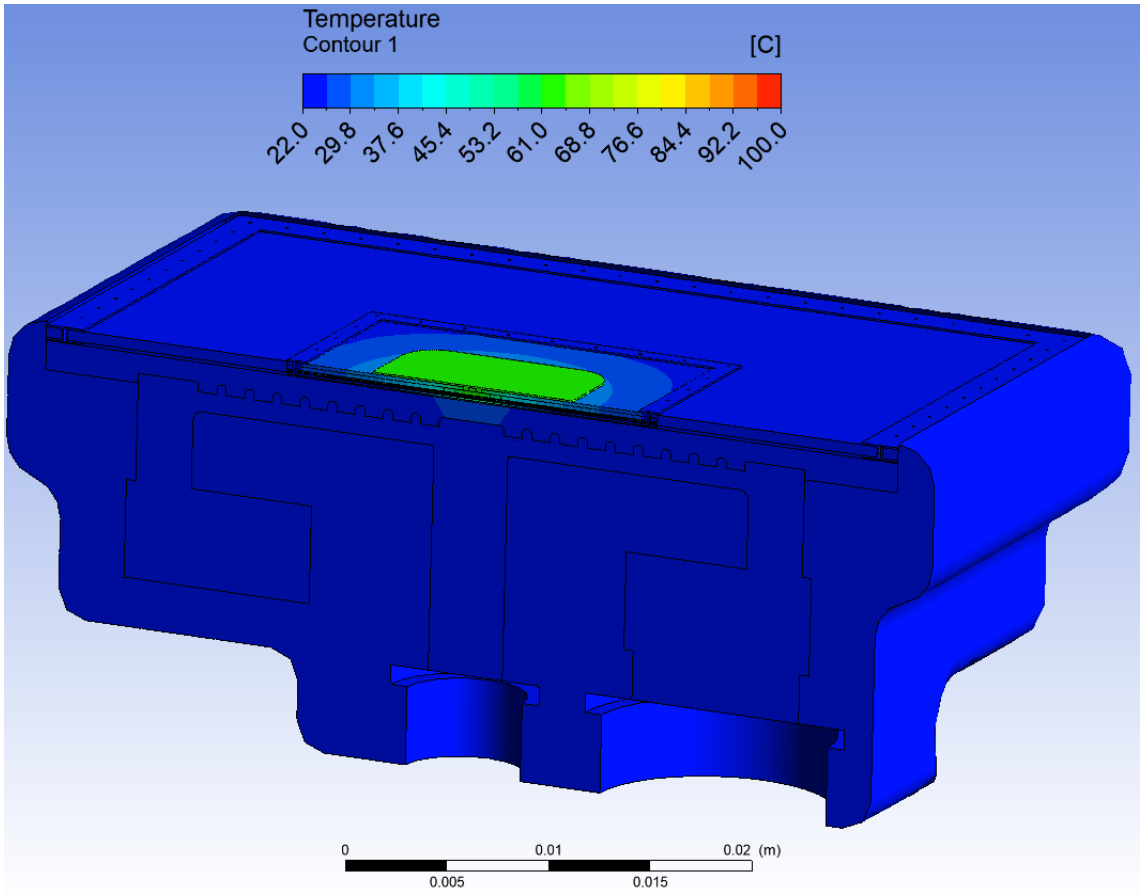

Figure 6.40: Temperature contour of the JIC with the M22Gc PCB cross-section with graphite for a 25 W dissipation at the chip level.

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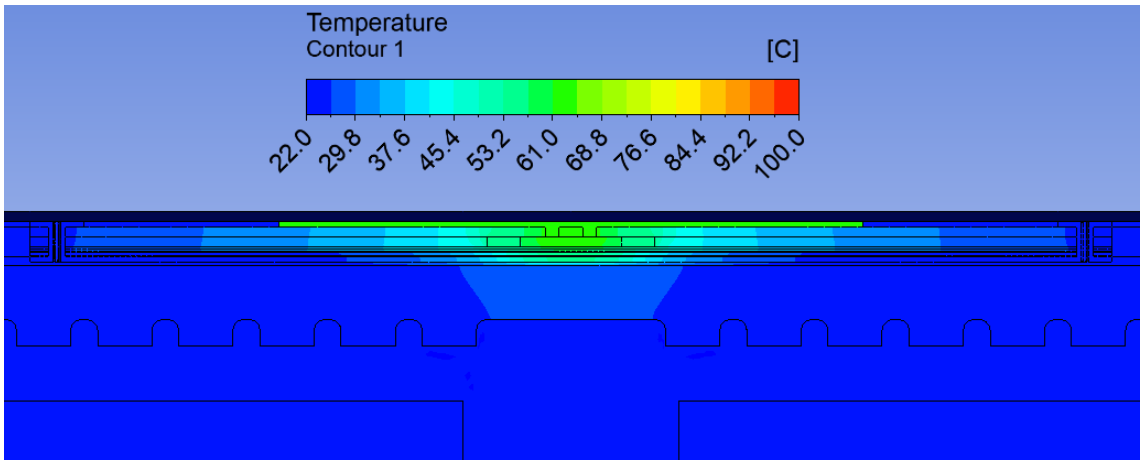

Figure 6.41: Temperature contour of the JIC with the M22Gc PCB cross-section with graphite for a 25 W dissipation at the chip level.

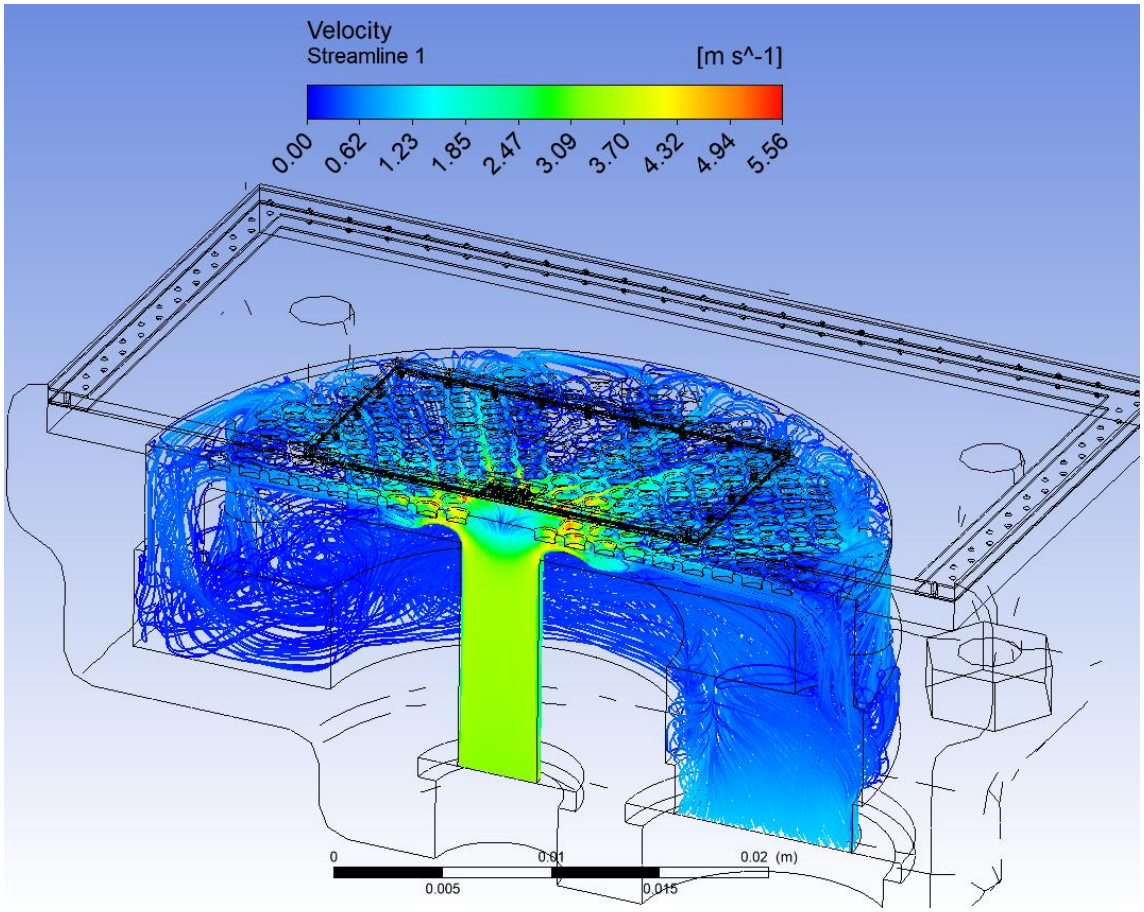

Figure 6.42: velocity streamlines through the water JIC.

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In order to assess the effect of the thermal conductivity of the 60 µm isolation prepreg layer between the PCB package and the copper heat sink, the maximum achieved effective HTC of the JIC (43000 W/(m.K)) is assigned as a boundary condition (representing the JIC), and the R_{thJA} is calculated for a range of thermal conductivities from 0.3 W/(m.K) to 30 W/(m.K). Figure 6.43 shows the simulated R_{thJA} values as a function of the thermal conductivity of the isolation layer.

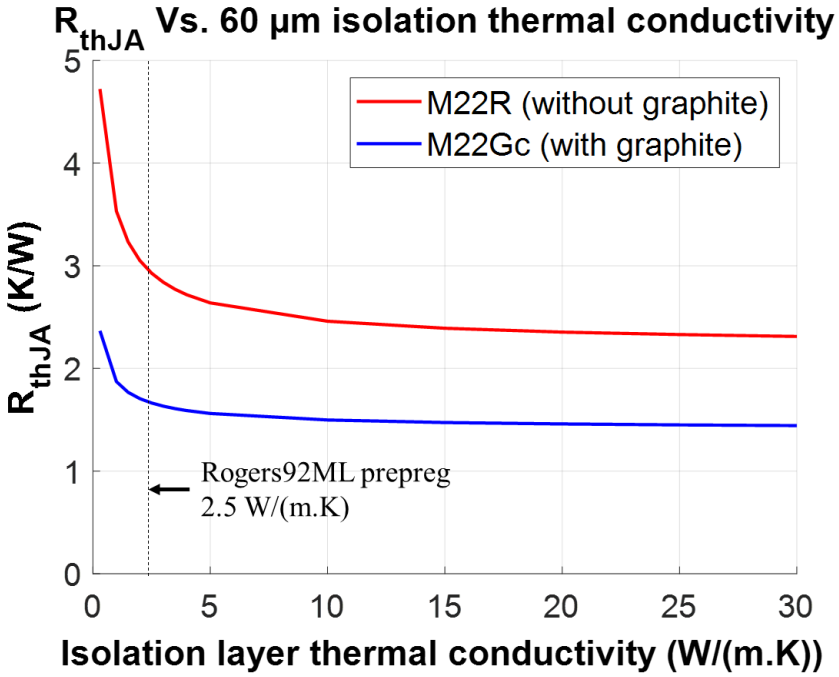

Figure 6.43: The expected R_{thJA} values by simulation as a function of the thermal conductivity of the 60 µm isolation layer.

Increasing the isolation layer thermal conductivity by 10 times (from 2.5 W/(m.K) to 25 W/(m.K)) results in only 13 % reduction in R_{thJA}, which allows to reach 993 W/cm² (very close to the target of 1000 W/cm²) without exceeding 175°C junction temperature.

6.4 Thermohydraulic measurements

Thermohydraulic measurements are performed using the methodology and the experimental setup explained in chapter 3 section 3.4.3 in order to measure the total R_{thJA} and the pressure drop of the water JIC. The water inlet and outlet tubes are glued to the water JIC manifold as shown in Figure 6.44b and connected to the experimental setup. The PCB laminated with the etched copper pin-fins heat sink is assembled to the water JIC manifold using four screws as shown in Figure 6.44a. Figure 6.45 shows the assembly of the PCB/Cu pin-fins/JIC manifold mounted and connected to the thermohydraulic experimental setup.

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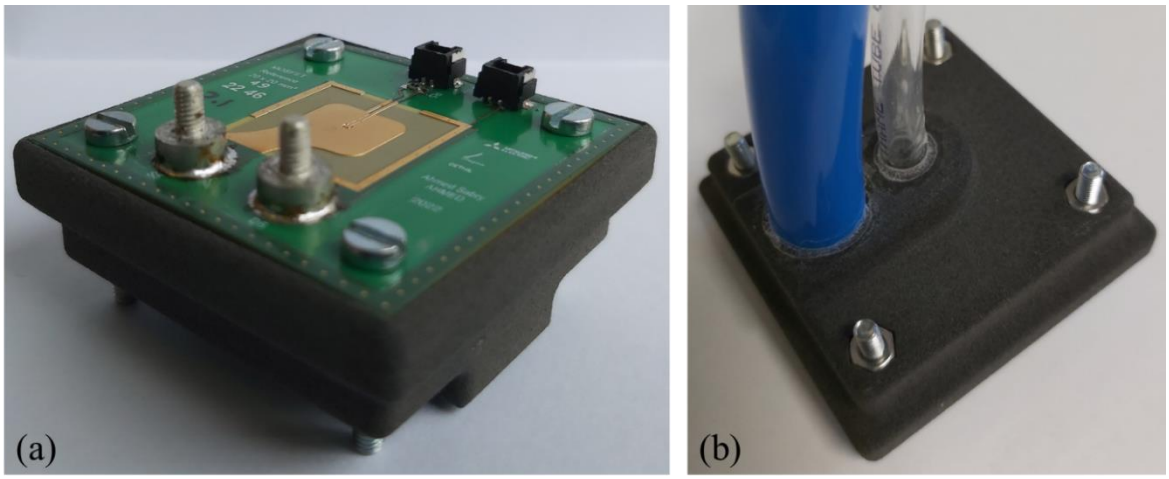

Figure 6.44: (a) Assembly of PCB/Cu pin-fins/JIC manifold. (b) Inlet and outlet tubes glued to the manifold.

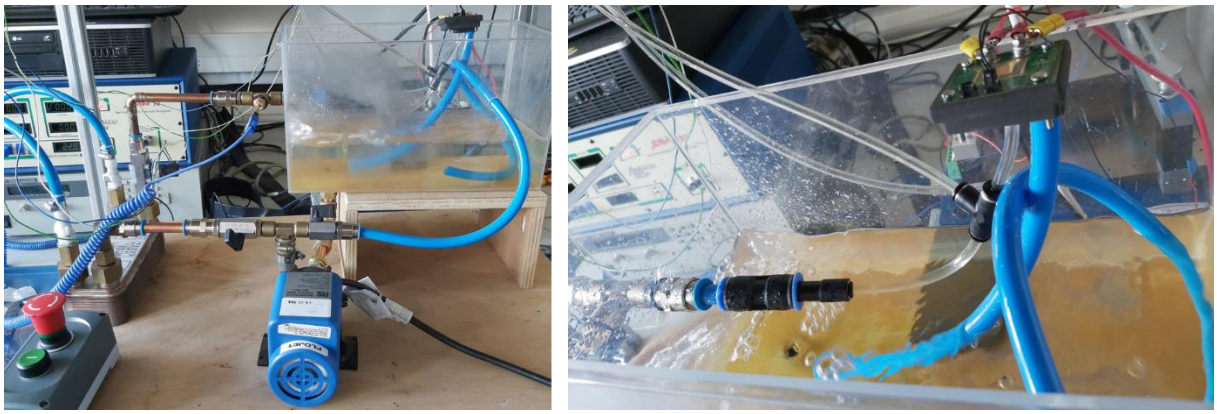

Figure 6.45: Thermohydraulic experimental setup.

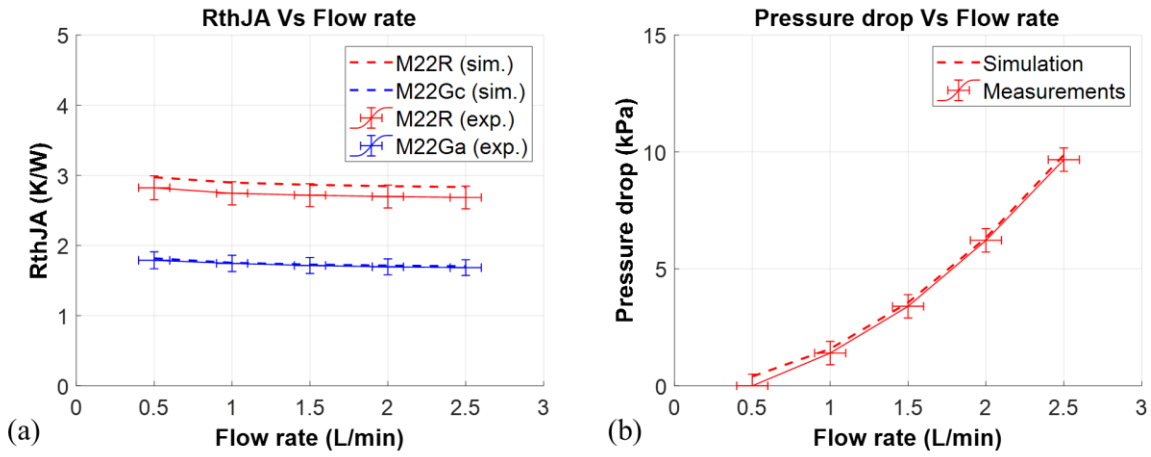

Figure 6.46: Thermo-hydraulic measurements and simulation with (a) R_{thJA} versus flow rate. (b) pressure drop versus flow rate.

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Figure 6.46a shows the R_{thJA} plotted as a function of the water volumetric flow rate of the JIC in the range from 0.5 L/min to 2.5 L/min. These measured values are compared to simulation results as well as the measured pressure drop of the JIC water (Figure 6.46b).

6.5 Results and discussion

As shown in Figure 6.46a, R_{thJA} decreases slightly with the increasing water flow rate. The reduction is only 5 % for the M22R PCB variant without graphite (from 2.823 K/W down to 2.684 K/W) and about 6 % for the M22Ga PCB variant with graphite (from 1.789 K/W down to 1.685 K/W). The simulated R_{thJA} values are in excellent agreement with the experiments and within the margin of error of the experiments, at +5 % (compared with the measurements) for M22R and +1 % for M22Ga.

The thermohydraulic measurements show that the R_{thJA} of M22Ga is lower by 37 % compared to M22R (from 2.684 K/W to 1.685 K/W at 2.5 L/min). This agrees closely with the 35.5 % measured in Chapter 5 (section 5.4.3) when mounting the PCB on the water cold plate presented in Chapter 3 section 3.4.1.3. This indicates that the graphite heat spreader alone is responsible for 35-37 % reduction in R_{thJA}. Moreover, the laminated JIC is responsible for 31-33 % reduction in R_{thJA} compared to the conventional water cold plate used before (from 3.88 K/W to 2.684 K/W for the M22R PCB without graphite, and from 2.5 K/W to 1.685 K/W for the M22Ga PCB with embedded graphite).

The measured pressure drop increases by increasing the water flow rate as shown in Figure 6.46b. It reaches 9.67 kPa at 2.5 L/min (0.403 W pumping power) compared to around 0.4 kPa at 0.5 L/min (0.0033 W pumping power). The CHT simulations (using the SST turbulence model) predicted the pressure drop with only 2 % difference (compared to the 9.87 kPa by simulations). The difference increases at a lower flow rate since the measurements accuracy is ± 0.5 kPa.

The objective of the water JIC solution was to reach 1000 W/cm² (i.e. 104.16 W for the embedded MOSFET chip size), without exceeding the maximum junction temperature T_j limit of 175°C. Theoretically speaking and giving the measured R_{thJA} value of 1.685 K/W at 2.5 L/min when injecting 25 W, the expected power that can be reached without exceeding the 175°C limit is 90 W (864 W/cm²). However, it is observed that injecting higher power in M22Ga results in higher R_{thJA}, as shown in Figure 6.47. The same is not observed with M22R. This indicates that the performance of graphite heat spreaders can be affected by the increase

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of the temperature. This degradation in performance can be due to a temperature-dependency of the thermal conductivity of the pyrolytic graphite sheets.

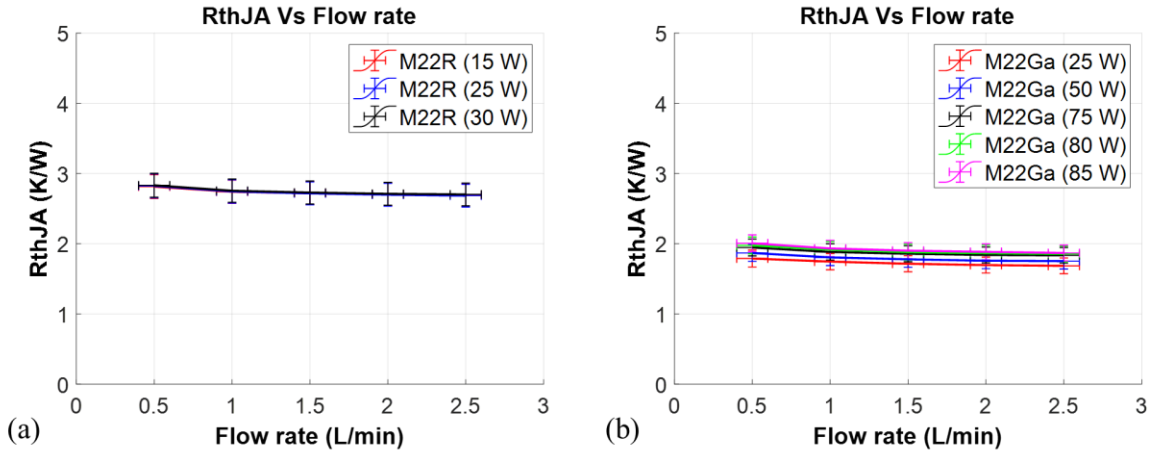

Figure 6.47: (a) R_{thJA} Vs. flow rate of M22R PCB variant at different injected powers. (b) R_{thJA} Vs. flow rate of M22Ga PCB variant with graphite at different injected powers.

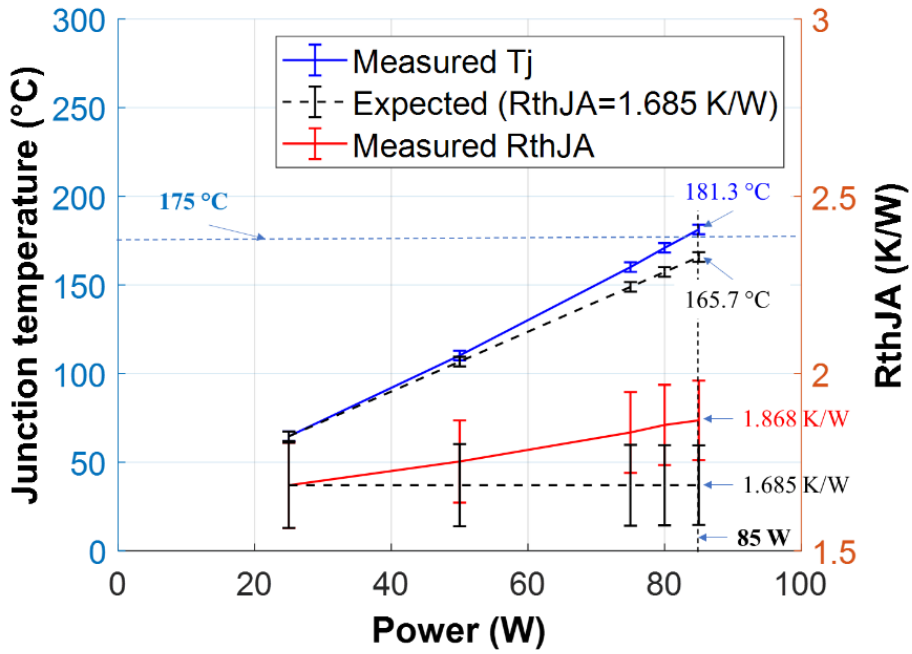

Figure 6.48: The variation of R_{thJA} with the injected power (right) of the M22Ga PXB with graphite at 2.5 L/min and the corresponding variation in T_j (left).

Figure 6.48 shows the effect of increasing the injected power on the maximum T_j and the R_{thJA} of the PCB with graphite. The maximum power injected in the measurement is 85 W which resulted in 181.3°C maximum T_j compared to 165.7°C expected. The M22Ga PCB with graphite reaches the limit of 175°C at 82 W which corresponds to 787 W/cm² power loss density.

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6.6 Conclusion

This chapter presents a numerical and experimental analysis of the heat extraction solution based on water jet impingement cooling. This cooling solution is composed of a chemically etched copper base plate laminated to a fabricated PCB, which includes the embedded MOSFET and graphite heat spreaders. The copper plate is etched to create 0.5 mm height pin-fins in order to maximize the heat exchange surface with the cooling water. This combination of the PCB/etched copper pin-fins is assembled to a compact water manifold of the fabricated by the SLS technique.

Forming the pin-fins on the copper plate using chemical etching is an attractive solution, since it is a process that is already used in PCB manufacturing. However, it is found that it puts limits on the height of the pin-fins since etching more than 0.5 mm (etching depth) can cause inhomogeneity with respect to the shape of the pin-fins and the overall etching depth. The photoresist film can fall off the pin-fins surfaces for larger etching depths. Forming taller structures would require a careful control of the etching process, as the results depend on the concentration and the freshness of the etcher (as well as on the robustness of the photosensitive layer). For the present cooling solution, based on CHT simulations, such short pin-fins (0.5 mm) offers 20 % improvement in effective HTC comparing to not having pin-fins. However this results in a modest reduction in R_{thJA} by only 3.2 % compared to not having pin-fins. The copper heat sink can be attached (before or after etching of the pin fins), by laminating it to the PCB stack during its fabrication process, much like any other copper layer.

The presented water jet impingement cooler reduces the R_{thJA} experimentally by 33 % (reaching 1.685 K/W at 2.5 L/min, or 17.6 K.mm²/W) compared to a conventional cold plate. The effective HTC of the JIC is around 43 kW/(m².K) at a 9.7 kPa pressure drop. this performance allows reaching 865 W/cm² power loss density without exceeding the 175°C junction temperature limit. However, it is observed that the graphite heat spreader performance is degraded with the increase of T_j caused by the increase in the injected power, which leads to reaching the limit of 175°C at just 787 W/cm² power loss density.

Furthermore, increasing the thermal conductivity of the isolation layer by 10 times (from 2.5 W/(m.K) to 25 W/(m.K)) results in only 13 % reduction in R_{thJA}. Therefore, the power loss density can theoretically be increased to 993 W/cm² (very close to the target of 1000 W/cm²) without exceeding 175°C junction temperature.

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7 General conclusions and perspectives

It is important to develop thermal management and packaging solutions to reduce the thermal resistance of power electronics devices, because of the increased power loss density levels achieved as the semiconductor chips shrink. A lot of progress has been achieved in electrical performance, cost and size of the chips. However, packaging and thermal management technology have not reached the same level of development, which makes it difficult to use the most advanced chip technologies available to their full potential. In this thesis, thermal management solutions compatible with PCB embedding technology were investigated.

The thermal management solutions allowing for heat spreading and heat extraction were reviewed in order to find the most suitable technique for PCB packaging and embedding technology. Two thermal management solutions were examined in this work. The first involves embedding a pyrolytic graphite heat spreaders within the PCB package. The second employs a water jet impingement heat exchanger to collect heat from the surface of the PCB. Both solutions were designed to handle a power loss density of 500 – 1000 W/cm² at the chip level and are compatible with PCB embedding technology and manufacturing processes.

The section below presents a summary of the thesis work as well as the main contributions (in bold).

7.1 Summary and contributions

- **A parametric study based on an analytical heat transfer model was performed to determine the heat spreading requirements** to dissipate 500 W/cm² power loss density from a 3.3×3.3mm^2 chip, considering a moderately efficient heat exchanger (cold plate).

- For heat spreading, **a PCB structure was designed with embedded two layers of PGS.**

    - Embedding a sandwiched structure of graphite/adhesive in PCB packages near the chip, in a way that is compatible with the existing PCB fabrication process.

    - Micro-vias were laser-drilled through graphite/adhesive stack and plated with copper by electrodeposition, which are necessary for thermo-mechanical aspects.

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- **Diode and MOSFET PCB packages with embedded graphite were successfully fabricated.**
    - Electrical characterization tests obtained a **manufacturing yield of 86 % for the embedded semiconductor devices**, which is a reasonable value for a prototype run.
    - Reflow tests showed that micro-vias must be distributed over the spreader area to provide mechanical clamping of the graphite layers, and prevent their delamination.
- Thermal impedance simulations and measurements were performed to obtain R_{thJA} and R_{thJC} values of the PCB variants. **For R_{thJC}, the TDIM method (according to JEDEC51-14 standard), used for measurements, was implemented also in simulations.**
    - **Up to 51 % reduction in R_{thJA} and 25 % reduction in R_{thJC} were observed by FEM thermal simulations** compared to **38 % reduction in R_{thJA} and 30 % reduction in R_{thJC} by measurements.**
    - R_{thJA} values gives better indication on the thermal performance of the package comparing to R_{thJC} values, which can misestimate the spreading effect in the package.
    - By comparing to a traditional packaging technology, the R_{thJA} values of TO-247-3 packaged chip remains lower than that of PCB-embedded devices with a graphite heat spreader, indicating a more efficient spreading effect for a thick copper lead frame than for thin graphite layers. However, the graphite heat spreader constitutes an interesting trade-off, as they do not cause any significant increase in board thickness, whereas the copper heat spreader in a TO247-3 is about 2 mm-thick.
- **Additional PCB variants with dual diodes were designed and fabricated** to assess the impact of graphite one the thermal coupling behavior.
    - **The thermal coupling percentage was increased (from 1.85 % to 11.85 %) due to the graphite layers** by simulations while **measurements showed it has increased from 2.94 % in the reference PCB sample to**

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8.78 % by embedding graphite in the PCB. This may help balance the temperature of chips, for example in the case of parallel connection.

- For heat extraction, liquid jet impingement combined with efficient enlargement of the heat exchange surface, pin-fins, was chosen for heat extraction thermal management solution, since it shows high thermal performance and provides a uniform surface temperature.

- **The heat extraction solution based on water jet impingement cooling (JIC) was designed and fabricated**.

    - It is composed of a chemically etched copper base plate laminated to the fabricated PCB, which includes embedded MOSFET and graphite heat spreaders. **The copper plate was chemically etched to create 0.5 mm height pin-fins in order to maximize the heat exchange surface with the cooling water.**

    - This combination of the PCB/etched copper pin-fins was assembled with **a compact water manifold of the JIC which is fabricated by SLS technique (additive manufacturing).**

    - Forming the pin-fins on the copper plate using chemical etching is an attractive solution, since it is a process that is already used in PCB manufacturing. However, it is found that it puts limits on the height of the pin-fins: etching more than 0.5 mm (etching depth) can cause inhomogeneity with respect to the shape of the pin-fins and the overall etching depth because the photoresist film used to pattern the copper can fall off the pin-fins surfaces during the process.

    - Forming taller structures would require a careful control of the etching process, as the results depend on the concentration and the freshness of the etcher (as well as on the robustness of the photosensitive layer).

    - Based on CHT simulations, such short pin-fins offers 20 % increase in effective HTC, but a modest reduction in R_{thJA} (3.2 %).

    - The copper heat sink can be attached (before or after etching of the pin fins), by laminating it to the PCB stack during its fabrication process, much like any other copper layer.

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- **Thermohydraulic measurements and CHT simulations were performed** to determine the thermohydraulic performance of the JIC.
    - The presented water JIC **reduces the R_{thJA} experimentally by 33 % (reaching 1.685 K/W at 2.5 L/min, or 17.6 K.mm²/W) compared to a conventional cold plate.** The effective HTC of the JIC is calculated by simulations and it is found to be around **43 kW/(m².K) at a 9.7 kPa pressure drop.**
    - This performance **allows reaching 865 W/cm² power loss density without exceeding the 175°C junction temperature limit**. However, it is observed that the graphite heat spreader performance is affected by temperature, which leads to **reaching the limit of 175°C at just 787 W/cm² power loss density.**
    - Increasing the isolation layer thermal conductivity by 10 times (from 2.5 W/(m.K) to 25 W/(m.K)) results in only 13 % reduction in R_{thJA}, which allows theoretically to reach 993 W/cm² (very close to the target of 1000 W/cm²) without exceeding 175°C junction temperature.

The proposed cooling solutions allow to extract more than 800 W/cm² with a compact structure compatible with the PCB embedding and fabrication process.

7.2 Perspectives

Graphite has been found to be a very promising heat spreader for this application, as it is compatible with PCB process, is relatively inexpensive, and offer a clear improvement in thermal performance However, it was found that its mechanical properties are limited, and may cause early delamination of the PCB structure. While the distribution of vias over the graphite surface seem to provide an efficient reinforcement, a more complete investigation is needed to validate the long-term reliability of the proposed structure (thermal cycling, moisture absorption, etc). Also, various graphite and adhesive types can be studied in order to choose the most suitable ones in terms of CTE matching which can decrease the thermo-mechanical stresses in the PCB package.

Further development can be made to the isolation prepreg layer used to laminate the PCB to the copper base plate by using more thermal conductive prepreg. This can allow to operate at higher power loss density.

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Appendices

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Appendix A: analytical model for the estimation of the equivalent thermal conductivity

Micro-via regions and thin multi-layers in the PCB can be challenging in FEM simulations since these small features require a large number of elements, resulting in high computational power and time. To overcome this issue, especially during the preliminary design phase, micro vias and the graphite/adhesive stack are simplified by a network of thermal resistances, allowing the equivalent thermal conductivity in the vertical and lateral direction (keq_z and keq_{xy} respectively) to be obtained. This analytical model is derived mathematically and then coded using MATLAB.

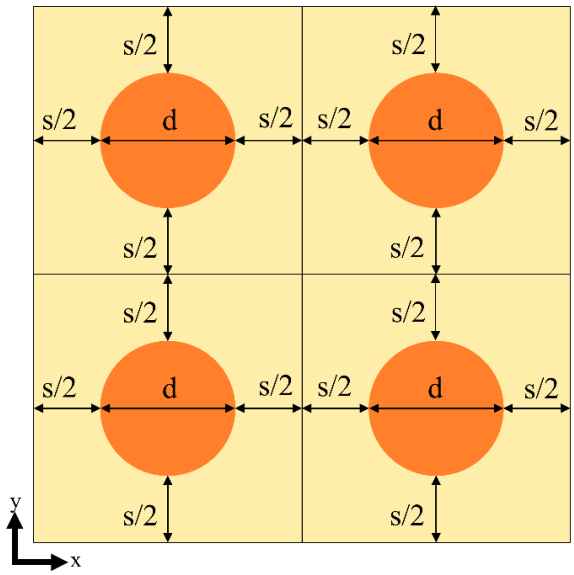

Figure A.1: Top view of a region of copper vias through a substrate material.

Figure A.1 shows a region of copper vias through a substrate material. The amount of copper depends on the diameter of vias (d) and the spacing between the edges of vias (s). The region of vias is divided into several blocks where each block contains a single via.

As shown in Figure A.2, the via block can be simplified as a network of of vertical and lateral thermal resistances. By applying in-series and in-parallel rules of resistance network, the equivalent vertical thermal resistance ($Rtheq_z$) and the equivalent lateral thermal resistance of the via block ($Rtheq_{xy}$) is determined. Therefore, the keq_z and keq_{xy} can be obtained consequently.

The cylindrical via can be filled completely with copper or partially (hollow) with a copper thickness of (f) as presented in Figure A.3. The equations to obtain the equivalent thermal conductivity are derived for each case.

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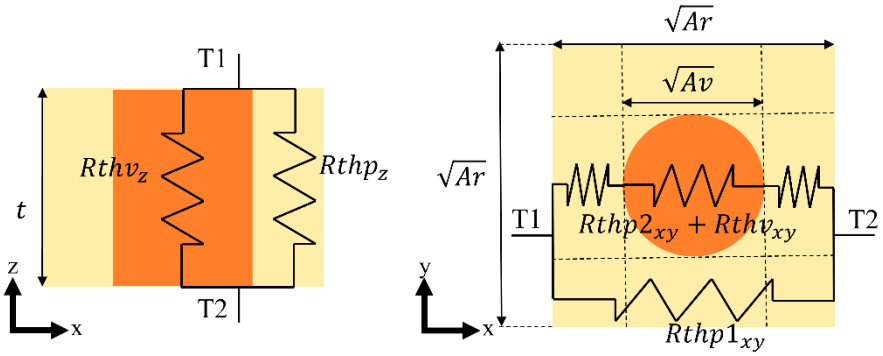

Figure A.2: The equivalent thermal resistance network of a single via in all directions.

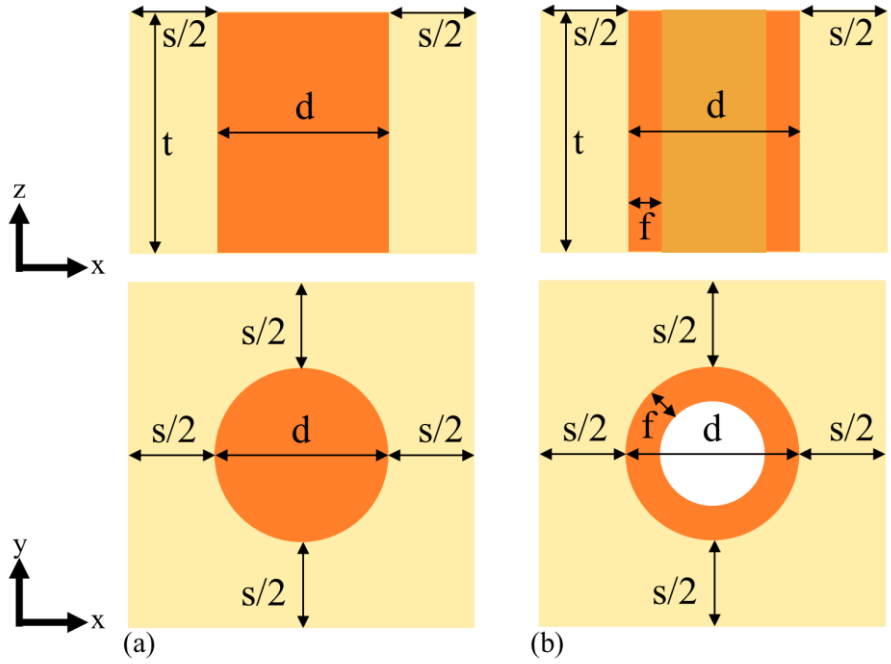

Figure A.3: (a) fully filled cylindrical via. (b) hollow cylindrical via.

For the case of a completely filled cylindrical copper via, the keq_z is determined as follows:

$$\frac{1}{Rtheq_z} = \frac{1}{Rthv_z} + \frac{1}{Rthp_z}$$

$$\frac{1}{\frac{t}{Ar\ keq_z}} = \frac{1}{\frac{t}{Av\ kv}} + \frac{1}{\frac{t}{Ar\ kp_z}}$$

$$Ar\ keq_z = kv\ Av + kp_z\ Ar - kp_z\ Av$$

$$\boldsymbol{keq_z = kv\ \frac{Av}{Ar} + kp_z\left(1 - \frac{Av}{Ar}\right)}$$

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where $Av = \frac{\pi}{4}d^2,\ Ar = (s+d)^2$, kv is the via thermal conductivity, and kp is the substrate thermal conductivity.

The same concept of thermal resistance network is applied to obtain the lateral equivalent thermal conductivity of a via block. For the case of a completely filled cylindrical copper via, the keq_{xy} is determined as follows:

$$\frac{1}{Rtheq_{xy}} = \frac{1}{Rthp1_{xy}} + \frac{1}{Rthp2_{xy} + Rthv_{xy}}$$

$$\frac{1}{\frac{\sqrt{Ar}}{t\sqrt{Ar}\,keq_{xy}}} = \frac{1}{\frac{\sqrt{Ar}}{t\left(\sqrt{Ar}-\sqrt{Av}\right)kp_{xy}}} + \frac{1}{\frac{(\sqrt{Ar}-\sqrt{Av})}{t\sqrt{Av}\ kp_{xy}} + \frac{\sqrt{Av}}{t\sqrt{Av}\ kv}}$$

$$\boldsymbol{keq_{xy} = kp_{xy}\left(1-\frac{\sqrt{Av}}{\sqrt{Ar}}\right) + \frac{1}{\frac{\left(1-\frac{\sqrt{Av}}{\sqrt{Ar}}\right)}{kp_{xy}} + \frac{\frac{\sqrt{Av}}{\sqrt{Ar}}}{kv}}}$$

In our proposed PCB stack with embedded graphite, the micro vias are drilled through graphite/adhesive stack which is a replacement of the substrate layer of a vertical thermal conductivity of kp_z and a lateral thermal conductivity of kp_{xy}.

In order to obtain the equivalent vertical thermal conductivity of a stack of multiple layers of graphite and adhesive materials, the equivalent vertical thermal resistance is obtained by applying in-series rule of the resistances network as follows:

$$Rtheq_z = Na\ Rtha_z + Ng\ Rthg_z = \frac{t}{A\ keq_z} = Na\ \frac{ta}{A\ ka_z} + Ng\ \frac{tg}{A\ kg_z}$$

$$t = Na\ ta + Ng\ tg$$

$$\boldsymbol{keq_z = \frac{t}{\frac{Na\ ta}{ka_z} + \frac{Ng\ tg}{kg_z}}}$$

Where *Ng* is the number of graphite layers, *Na* is the number of adhesive layers, *tg* is the graphite layer thickness, *ta* is the adhesive layer thickness, and *t* is the total thickness of the stack.

By applying the same concept, the equivalent lateral thermal resistance is obtained by applying in-parallel rule of the resistances network as follows:

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$$\frac{1}{Rtheq_{xy}} = \frac{Na}{Rtha_{xy}} + \frac{Ng}{Rthg_{xy}} = \frac{1}{\frac{\sqrt{A}}{t\sqrt{A}\,keq_{xy}}} = \frac{Na}{\frac{\sqrt{A}}{ta\sqrt{A}\,ka_{xy}}} + \frac{Ng}{\frac{\sqrt{A}}{tg\sqrt{A}\,kg_{xy}}}$$

$$\boldsymbol{keq_{xy}} = \frac{\boldsymbol{Na\ ta\ ka_{xy} + Ng\ tg\ kg_{xy}}}{\boldsymbol{t}}$$

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Appendix B: MATLAB code to estimate the equivalent thermal conductivity

Equivalent thermal conductivity of a layer with vias

```
clc
clear all
close all

d1= 0.00024;
d2 = 0.00024;
s=0.000005:0.000005:0.001;
ss=1000000.*s;
t = 0.000175;
kxy=0.3;
kz=0.3;
kvia = 400;
z=0:100:t;
for i=1:200
fun=@(z)(1-sqrt((((((d2-d1)./t).*z+d1).^2)./((4./pi).*(((((d2-
d1)./t).*z+d1)+s(i)).^2))))).*kxy+(sqrt((((((d2-
d1)./t).*z+d1).^2)./((4./pi).*(((((d2-d1)./t).*z+d1)+s(i)).^2)))).(((1-
sqrt((((((d2-d1)./t).*z+d1).^2)./((4./pi).*(((((d2-
d1)./t).*z+d1)+s(i)).^2))))./kxy)+(sqrt((((((d2-
d1)./t).*z+d1).^2)./((4./pi).*(((((d2-d1)./t).*z+d1)+s(i)).^2)))./kvia)));
kxy_eq(i) = (1./t).*integral(fun,0,t);
end
for i=1:200
    A=(d1+s(i))^2;
    kz_eq(i)=kz+(kvia-kz)*((pi/4)/A)*(d1*d2+(1/3)*((d2-d1)^2));
end

figure;
hold on
grid on
plot(ss,kxy_eq,'LineWidth',1.5,'color','b');
xlabel('Vias spacing between edges (µm)');
ylabel('keq_x_y (W/(m.K))');
set(gca,'FontSize',15);
title('keq_x_y Vs. vias density');

figure;
hold on
grid on
plot(ss,kz_eq,'LineWidth',1.5,'color','b');
xlabel('Vias spacing between edges (µm)');
ylabel('keq_z (W/(m.K))');
set(gca,'FontSize',15)
title('keq_z Vs. vias density');
```

Equivalent thermal conductivity of multiple layers

```
clc
clear all

t=[25,50,25,50,25];
kxy=[0.22,1300,0.22,1300,0.22];
kz=[0.22,15,0.22,15,0.22];
```


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```
n_layers=5;

 t_tot=sum(t);
for i=1:n_layers

   kxy_eq(i)=t(i)*kxy(i)/t_tot;
   Az(i)=(t(i)/kz(i));

end
Kxyeq=sum(kxy_eq)
Kzeq=t_tot/sum(Az)
```


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Appendix C: MATLAB code of the analytical model

SLA:

```
clc
clear all

A1 = 0.01*0.01;
A2 = 0.05*0.05;
h=10000;
d=0.0012;
Q=200;

a=sqrt(A1/pi);
b=sqrt(A2/pi);

k=400;

ep=a/b;
taw=d/b;
lamda=pi+(1/(sqrt(pi)*ep));
for i=1:length(k)

Bi=h*b/k(i);
theta=(tanh(lamda*taw)+(lamda/Bi))/(1+((lamda/Bi)*tanh(lamda*taw)));

epsi_max=((ep*taw)/sqrt(pi))+((1/sqrt(pi))*(1-ep)*theta);
epsi_av=((ep*taw)/sqrt(pi))+(0.5*((1-ep)^1.5)*theta);

R_max(i) = epsi_max/(sqrt(pi)*k(i)*a);
R_av(i) = epsi_av/(sqrt(pi)*k(i)*a);

R_conv(i) = 1/(h*A2);

dT_max(i) = Q*(R_max(i)+R_conv(i));
dT_av(i) = Q*(R_av(i)+R_conv(i));
R_tot_max(i)=dT_max(i)/Q;
R_tot_av(i)=dT_av(i)/Q;

Rth_L(i)=R_conv(i)+(log(A2/A1)/(4*pi*k(i)*d))-(0.577/(2*pi*k(i)*d));
end
figure
hold on
grid on
plot (k,R_tot_max,'color','black');
plot (k,R_tot_av,'color','yellow');
plot (k,R_max,'color','red');
plot (k,R_conv,'color','blue');
plot (k,Rth_L,'color','green');
```

Muzychka:

```
clear all new
clc
tic
% % %  Define number of layers
nb_layer=2;
% % % Define number of heat source
nb_source=1;
```


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```
% % % Baseplate Size in m
X=[0.05];
Y=[0.05];
% % % Power losses on each heat source [1,2.....] in W
P=[200];
% % % Z geo coordinate [1,2.....]
z=[0.0002,0.001];
thickness=[1,0.0002;2,0.001];
% % % Die size [1,2.....] in m
L_die_Y=[0.01];
L_die_X=[0.01];
% % % Center of the die [1,2.....] in mm
xc=[X(1)/2];
yc=[Y(1)/2];
% % % Source plane conductance
hs=[10000];
% % % Ambient temperature in °C
T_amb=22;
% % % Thermal conductivity in each layer
% kk=[100 200 400 700 1000 1500 2000];
kk=400;
for rr=1:length(kk)
    kkk=kk(rr);
kx=[1,400;2,400];
ky=[1,400;2,400];
kz=[1,400;2,400];
segma=sqrt(ky(1,2)./kx(1,2));
Y=Y./segma;
yc=yc./segma;
L_die_Y=L_die_Y./segma;
for j=1:nb_layer
    meo(j)=(kx(1,2)*ky(j,2))/(ky(1,2)*kx(j,2));
end
for j=1:nb_layer
k(j,2)=sqrt(kx(j,2).*kz(j,2));
end
% % % Thickness in mm for each layer
% thickness=[1,0.0005;2,0.001;3,0.0005];

for j=1:nb_layer
t(j,2)=thickness(j,2)./sqrt(kz(j,2)./kx(j,2));
end
% % % Matrix initialisation
dd=50;% dd has to be even number
ddz=5;
T=zeros(1,nb_layer);
A0=zeros(1,nb_layer);
B0=zeros(1,nb_layer);
Temp=zeros(dd+1,dd+1,nb_layer);
Tempt=zeros(dd+1,dd+1,nb_layer);
Temps=zeros(dd+1,dd+1,ddz+1,nb_layer);
% % % Accuracy of the surface plotting net
x=0:(X/dd):X;
y=0:((Y*segma)/dd):(Y*segma);
% % % Zero Fourrier coefficents
        FF = 0;
        F=0;
        for j=1:nb_layer
            F=0;
```


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```
            for i=j:nb_layer
           FF= (t(i,2)./k(i,2));
           F= F+FF;
            end
            T(j)=F;
        end

 for i=1:nb_source
for j=1:nb_layer

        A0(j)=(P(i)./(X.*Y*segma)).*((1./hs)+T(j));
        B0(j)=(-1)*(P(i)./(X.*Y*segma.*k(j,2)));

end
% % %  Index of the Fourrier Expension
% Nx=floor((5*X)/L_die_X(i));
% Ny=floor((5*Y)/L_die_Y(i));
Nx=10;
Ny=10;
% % % Eigenvalues used to consider the boundary conditions (adiabatic edges +
convection)
for m=1:Nx
lambda(m)=((m).*pi)./(X);
end
for j=1:nb_layer
for n=1:Ny
delta(j,n)=(((n).*pi)./(Y))./sqrt(meo(j));
end

for m=1:Nx
    for n=1:Ny
        beta(j,m,n)=sqrt(((lambda(m))^2)+(((delta(j,n))^2)./meo(j)));
    end
end
end
% % % Phi, Spreading Function
for m=1:Nx
    for n=1:Ny
PhiL_max(m)=((((k(nb_layer,2).*lambda(m))./hs).*tanh(lambda(m).*t(nb_layer,2)))+1)
./((((k(nb_layer,2).*lambda(m))./hs)+(tanh(lambda(m).*t(nb_layer,2)))));
PhiD_max(n)=((((k(nb_layer,2).*delta(nb_layer,n))./hs).*tanh(delta(nb_layer,n).*t(
nb_layer,2)))+1)./((((k(nb_layer,2).*delta(nb_layer,n))./hs)+(tanh(delta(nb_layer,n
).*t(nb_layer,2)))));
PhiB_max(m,n)=((((k(nb_layer,2).*beta(nb_layer,m,n))./hs).*tanh(beta(nb_layer,m,n)
.*t(nb_layer,2)))+1)./((((k(nb_layer,2).*beta(nb_layer,m,n))./hs)+(tanh(beta(nb_lay
er,m,n).*t(nb_layer,2)))));
    end
end
for j=nb_layer:-1:1
    if(j==nb_layer)

PhiL(j,:)=PhiL_max;
PhiD(j,:)=PhiD_max;
PhiB(j,:,:)=PhiB_max;
    else

PhiBeta_t(:,:)=PhiB(j+1,:,:);
for m=1:Nx
    for n=1:Ny
```


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```
PhiL(j,m)=(((k(j,2)./(k(j+1,2))).*tanh(lambda(m).*t(j,2)))+(PhiL(j+1,m))./((k(j,2
)./(k(j+1,2)))+(PhiL(j+1,m).*tanh(lambda(m).*t(j,2))));

PhiD(j,n)=((((k(j,2).*delta(j,n))./(k(j+1,2).*delta(j+1,n))).*tanh(delta(j,n).*t(j
,2)))+(PhiD(j+1,n)))./(((k(j,2).*delta(j,n))./(k(j+1,2).*delta(j+1,n)))+(PhiD(j+1,
n).*tanh(delta(j,n).*t(j,2))));


PhiB(j,m,n)=((((k(j,2).*beta(j,m,n))./(k(j+1,2).*beta(j+1,m,n))).*tanh(beta(j,m,n)
.*t(j,2)))+(PhiBeta_t(m,n)))./(((k(j,2).*beta(j,m,n))./(k(j+1,2).*beta(j+1,m,n)))+
(PhiBeta_t(m,n).*tanh(beta(j,m,n).*t(j,2))));
    end
end
    end
end
% % % Fourrier coeffcients for order higher than one
AL=zeros(nb_layer,m);
AD=zeros(nb_layer,n);
AB=zeros(nb_layer,m,n);

for m=1:Nx
AL(1,m)=(4.*P(i).*cos(lambda(m).*xc(i)).*sin(0.5.*lambda(m).*L_die_X(i))./(X.*Y.*
segma.*L_die_X(i).*k(1,2).*lambda(m).*lambda(m).*PhiL(1,m));
end
for n=1:Ny
AD(1,n)=(4.*P(i).*segma.*cos(delta(1,n).*yc(i)).*sin(0.5.*delta(1,n).*L_die_Y(i)))
./(X.*Y.*L_die_Y(i).*(segma^2).*k(1,2).*delta(1,n).*delta(1,n).*PhiD(1,n));
end
PhiB_t(:,:)=PhiB(1,:,:);
for m=1:Nx
    for n=1:Ny
AB(1,m,n)=(16.*P(i).*segma.*cos(lambda(m).*xc(i)).*sin(0.5.*lambda(m).*L_die_X(i))
.*cos(delta(1,n).*yc(i)).*sin(0.5.*delta(1,n).*L_die_Y(i))./(X.*Y.*L_die_X(i).*L_
die_Y(i).*(segma^2).*k(1,2).*lambda(m).*delta(1,n).*beta(1,m,n).*PhiB_t(m,n));
    end
end
for j=2:nb_layer

        AB_t(:,:)=AB(j-1,:,:);
        PhiB_t(:,:)=PhiB(j-1,:,:);
for m=1:Nx
    for n=1:Ny
        AL(j,m)=AL(j-1,m).*(cosh(lambda(m).*t(j-1,2))-PhiL(j-
1,m).*sinh(lambda(m).*t(j-1,2)));
        AD(j,n)=AD(j-1,n).*(cosh(delta(j-1,n).*t(j-1,2))-PhiD(j-
1,n).*sinh(delta(j-1,n).*t(j-1,2)));

        AB(j,m,n)=AB_t(m,n).*(cosh(beta(j-1,m,n).*t(j-1,2))-
PhiB_t(m,n).*sinh(beta(j-1,m,n).*t(j-1,2)));
    end
end

end
% % % Calcul of the temperature distribution
for j=1:nb_layer
    zi=1;
   for zz=0:(z(j)/ddz):z(j)
```


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```
    for xi=1:length(x)

        for yi=1:length(y)
        T1=0;
        for m=1:Nx

S1=AL(j,m).*cos(lambda(m).*x(xi)).*(cosh(lambda(m).*(zz./sqrt(kz(j,2)./kx(j,2))))-
(PhiL(j,m).*sinh(lambda(m).*(zz./sqrt(kz(j,2)./kx(j,2))))));
            T1=T1+S1;
        end

        T2=0;
        for n=1:Ny

S2=AD(j,n).*cos(delta(1,n).*(y(yi)./segma)).*(cosh(delta(j,n).*(zz./sqrt(kz(j,2)./
kx(j,2))))-(PhiD(j,n).*(sinh(delta(j,n).*(zz./sqrt(kz(j,2)./kx(j,2)))))));
            T2=T2+S2;
        end

        T3=0;
        for m=1:Nx
            for n=1:Ny

S3=AB(j,m,n).*cos(lambda(m).*x(xi)).*cos(delta(1,n).*(y(yi)./segma)).*(cosh(beta(j
,m,n).*(zz./sqrt(kz(j,2)./kx(j,2))))-
(PhiB(j,m,n).*(sinh(beta(j,m,n).*(zz./sqrt(kz(j,2)./kx(j,2)))))));
                T3=T3+S3;
            end
        end


Temp(xi,yi,zi,j)=A0(j)+(B0(j)*(zz./sqrt(kz(j,2)./kx(j,2))))+T1+T2+T3;

        end

    end
    zi=zi+1;
   end

end
Temps(:,:,:,:)=Temps(:,:,:,:)+Temp(:,:,:,:);

TT1=0;
for m=1:Nx

SS1=(AL(1,m).*cos(lambda(m).*xc).*(sin(lambda(m).*0.5.*L_die_X))./(lambda(m).*L_d
ie_X);
            TT1=TT1+SS1;
        end

        TT2=0;
        for n=1:Ny

SS2=(segma.*AD(1,n).*cos(delta(1,n).*(yc./segma)).*(sin(0.5.*delta(1,n).*(L_die_Y.
/segma)))./(delta(1,n).*L_die_Y);
            TT2=TT2+SS2;
        end

        TT3=0;
```


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```
        for m=1:Nx
            for n=1:Ny

SS3=(segma.*AB(1,m,n).*cos(lambda(m).*xc).*cos(delta(1,n).*(yc./segma)).*(sin(0.5.
*delta(1,n).*(L_die_Y./segma))).*(sin(lambda(m).*0.5.*L_die_X))./(L_die_X.*lambda
(m).*L_die_Y.*delta(1,n));
                TT3=TT3+SS3;
            end
        end

Tc(i)=A0(1)+2*TT1+2*TT2+4*TT3+T_amb;
 end
Rt(rr)=(mean(Tc)-T_amb)/sum(P);
end
figure
plot(kk,Rt)
% % % Plotting cross section z axis
% % % Meshing reverse the z axis for each layer and coning in a single figure
save('saveTemps.mat','Temps');
for j=1:nb_layer

for i=((j-1)*(ddz)+1):(((j-1)*(ddz)+1)+ddz)
Tempst(:,:,i)= Temps(:,:,(i-ddz*(j-1)),j);
end
end
% % % Plotting top surface
xx=0:(X/dd):X;
yy=0:((Y*segma)/dd):(Y*segma);

figure
[XX,YY] = meshgrid(x,y);
TT=Tempst(:,:,1)+T_amb;
h=contour(XX,YY,transpose(TT),'ShowText','on','Fill','on','LineStyle','-
.','LineColor','black');
xlabel('x-axis')
ylabel('y-axis')


zzz(1)=0;
for j=1:nb_layer

for i=((j-1)*(ddz)+2):(((j-1)*(ddz)+1)+ddz)

zzz(i)= (zzz(i-1)-(z(j)/ddz));
end
end

% % % Plotting at half of the Y axis (death=dd/2)
figure

hold on

[XX,ZZ] = meshgrid(xx,zzz);

TTT=transpose(squeeze(Tempst(:,dd/2,:)))+T_amb;

h=contour(XX,ZZ,TTT,'ShowText','on','Fill','on','LineStyle','-
.','LineColor','black');
```


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```
gg=0;
for i=1:length(thickness)
    hold on
gg=-thickness(i,2)+gg;
plot(x,gg*ones(size(x)),'Color','black');
end
xlabel('x-axis')
ylabel('z-axis')
toc
```

Parametric study of heat spreading

```
clc
clear all
close all


RRt=load('saveRtot.mat');
Rtt=RRt.Rt;

m=min(Rtt);
mm=min(m);
mmm=min(mm);

Rttt=Rtt;

k=[100 200 400 700 1000 1500 2000];
tcu=[0.000035 0.0001 0.0002 0.0005 0.001];
ts=[0.0001 0.0002 0.0005 0.001 0.005];
As=[0.005 0.01 0.02 0.05 0.1];
h=[100 1000 10000 50000 100000];

for a=1:length(k)
    for b=1:length(tcu)
        for c=1:length(ts)
            for d=1:length(As)
                for e=1:length(h)

                    if (Rttt(a,b,c,d,e) > 3)
                        Rttt(a,b,c,d,e)=0;
                    end
                end
            end
        end
    end
end

figure;
hold on
grid on
Rth=squeeze(Rtt(3,3,3,3,:));
hh=100:10:100000;
RRth=pchip(h,Rth,hh);
semilogx(h,Rth,'LineWidth',2);
semilogx(h,Rth,'*','Color','k');
set(gca,'xscale','log');
xlabel('Convection heat transfer coefficient h
(W/(m².K))','FontSize',12,'FontWeight','bold');
ylabel('Thermal Resistance RthJA (K/W)','FontSize',12,'FontWeight','bold');
```


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```
title('RthJA Vs. Heat transfer coefficient','FontSize',12,'FontWeight','bold')
set(gca,'FontSize',12)

figure;
hold on
ttcu=0.035:10:0.35;
Rttcu=squeeze(Rtt(3,:,3,3,3));
plot(tcu*1000,Rttcu,'LineWidth',2)
plot(tcu*1000,Rttcu,'*','Color','k')
xlabel('Copper layer thickness tcu (mm)','FontSize',12,'FontWeight','bold');
ylabel('Thermal Resistance RthJA (K/W)','FontSize',12,'FontWeight','bold');
title('RthJA Vs. Copper layer thickness','FontSize',12,'FontWeight','bold');
set(gca,'FontSize',12)


figure;
hold on
kk=100:10:2000;
for i=1:length(As)
Rtk=squeeze(Rtt(:,3,3,i,3));
RRtk=pchip(k,Rtk,kk);
plot(kk,RRtk,'LineWidth',2)
plot(k,Rtk,'*','Color','k')
end
legend('As=5x5 mm²','','As=10x10 mm²','','As=20x20 mm²','','As=50x50
mm²','','As=100x100 mm²','','FontSize',12);
xlabel('Thermal Conductivity k (W/(m.K))','FontSize',12,'FontWeight','bold');
ylabel('Thermal Resistance RthJA (K/W)','FontSize',12,'FontWeight','bold');
title('RthJA Vs. Thermal Conductivity','FontSize',12,'FontWeight','bold');
set(gca,'FontSize',12)

figure;
hold on
kk=100:10:2000;
for i=1:length(ts)
Rtk=squeeze(Rtt(:,3,i,3,3));
RRtk=pchip(k,Rtk,kk);
plot(kk,RRtk,'LineWidth',2)
plot(k,Rtk,'*','Color','k')
end
legend('ts=0.1 mm','','ts=0.2 mm','','ts=0.5 mm','','ts=1 mm','','ts=5
mm','','FontSize',12);
xlabel('Thermal Conductivity k (W/(m.K))','FontSize',12,'FontWeight','bold');
ylabel('Thermal Resistance RthJA (K/W)','FontSize',12,'FontWeight','bold');
title('RthJA Vs. Thermal Conductivity','FontSize',12,'FontWeight','bold');
set(gca,'FontSize',12)

figure;
hold on
AAs=0.005:0.001:0.1;
for i=1:length(k)
RtAs=squeeze(Rtt(i,3,3,:,3));
RRtAs=pchip(As,RtAs,AAs);
plot(AAs*1000,RRtAs,'LineWidth',2)
plot(As*1000,RtAs,'*','Color','k')
end
legend('k=100 W/(m.K)','','k=200 W/(m.K)','','k=400 W/(m.K)','','k=700
W/(m.K)','','k=1000 W/(m.K)','','k=1500 W/(m.K)','','k=2000
W/(m.K)','','FontSize',12);
```


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```
xlabel('Heat spreader length \surdAs (mm)','FontSize',12,'FontWeight','bold');
ylabel('Thermal Resistance RthJA (K/W)','FontSize',12,'FontWeight','bold');
title('RthJA Vs. Heat spreader length \surdAs','FontSize',12,'FontWeight','bold');
set(gca,'FontSize',12)

figure;
hold on
AAs=0.005:0.001:0.1;
for i=1:length(ts)
RtAs=squeeze(Rtt(3,3,i,:,3));
RRtAs=pchip(As,RtAs,AAs);
plot(AAs*1000,RRtAs,'LineWidth',2)
plot(As*1000,RtAs,'*','Color','k')
end
legend('ts=0.1 mm','','ts=0.2 mm','','ts=0.5 mm','','ts=1 mm','','ts=5
mm','','FontSize',12);
xlabel('Heat spreader length \surdAs (mm)','FontSize',12,'FontWeight','bold');
ylabel('Thermal Resistance RthJA (K/W)','FontSize',12,'FontWeight','bold');
title('RthJA Vs. Heat spreader length \surdAs','FontSize',12,'FontWeight','bold');
set(gca,'FontSize',12)

figure;
hold on
tts=0.0001:0.0001:0.005;
for i=1:length(k)
Rtts=squeeze(Rtt(i,3,:,3,3));
RRtts=pchip(ts,Rtts,tts);
plot(tts*1000,RRtts,'LineWidth',2)
plot(ts*1000,Rtts,'*','Color','k')
end
legend('k=100 W/(m.K)','','k=200 W/(m.K)','','k=400 W/(m.K)','','k=700
W/(m.K)','','k=1000 W/(m.K)','','k=1500 W/(m.K)','','k=2000
W/(m.K)','','FontSize',12);
xlabel('Heat spreader thickness ts (mm)','FontSize',12,'FontWeight','bold');
ylabel('Thermal Resistance RthJA (K/W)','FontSize',12,'FontWeight','bold');
title('RthJA Vs. Heat spreader thickness','FontSize',12,'FontWeight','bold');
set(gca,'FontSize',12)

figure;
hold on
tts=0.0001:0.0001:0.005;
for i=1:length(As)
Rtts=squeeze(Rtt(3,3,:,i,3));
RRtts=pchip(ts,Rtts,tts);
plot(tts*1000,RRtts,'LineWidth',2)
plot(ts*1000,Rtts,'*','Color','k')
end
legend('As=5x5 mm²','','As=10x10 mm²','','As=20x20 mm²','','As=50x50
mm²','','As=100x100 mm²','','FontSize',12);
xlabel('Heat spreader thickness ts (mm)','FontSize',12,'FontWeight','bold');
ylabel('Thermal Resistance RthJA (°C/W)','FontSize',12,'FontWeight','bold');
title('RthJA Vs. Heat spreader thickness','FontSize',12,'FontWeight','bold');
set(gca,'FontSize',12)
```


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Appendix D: MATLAB coded for the TDIM

```
clc
clear all
close all
filename1=["1-2-D22R_11W_TIM_t1_HtgSim.txt",
           "1-2-D22R_11W_TIM_t2_HtgSim.txt",
           "1-2-D22R_11W_TIM_t3_HtgSim.txt",
           "1-2-D22R_11W_TIM_t4_HtgSim.txt",
           "1-2-D22R_11W_TIM_t5_HtgSim.txt"];

filename2=["1-2-D22R_20W_water3d_t1_HtgSim.txt",
           "1-2-D22R_20W_water3d_t2_HtgSim.txt",
           "1-2-D22R_20W_water3d_t3_HtgSim.txt",
           "1-2-D22R_20W_water3d_t4_HtgSim.txt",
           "1-2-D22R_20W_water3d_t5_HtgSim.txt"];

for n=1:5
    f2=filename2(n);
    for m=1:5
        f1=filename1(m);
A1=readtable(f1,"Delimiter","|");
t1=A1(2:(size(A1)-1),"T_sec_");
Z1=A1(2:(size(A1)-1),"Z__C_W_");
time1=table2array(t1);
Zth1=table2array(Z1);
ln_time1=log(time1);
dadz1=gradient(Zth1,ln_time1);

A2=readtable(f2,"Delimiter","|");
t2=A2(2:(size(A2)-1),"T_sec_");
Z2=A2(2:(size(A2)-1),"Z__C_W_");
time2=table2array(t2);
Zth2=table2array(Z2);
ln_time2=log(time2);
dadz2=gradient(Zth2,ln_time2);
Zth1max=Zth1(length(Zth1));
Zth2max=Zth2(length(Zth2));

for i=1:size(dadz2)
D_dadz(i)=dadz1(i)-dadz2(i);
delta(i)=D_dadz(i)/(Zth1max-Zth2max);
eps(i)=0.0045*(Zth2(i))+0.003;
end
D_eps_delta=eps-delta;

for i=1:length(D_eps_delta)
    if D_eps_delta(i)<0
as1=(delta(i)-delta(i-1))/(Zth2(i)-Zth2(i-1));
as2=(eps(i)-eps(i-1))/(Zth2(i)-Zth2(i-1));
bs1=delta(i)-as1*Zth2(i);
bs2=delta(i)-as2*Zth2(i);
Rth_JC(n,m)=(bs2-bs1)/(as1-as2);
break
    end

end

    end
```


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```
end
Rth_JC_av=mean2(Rth_JC);
Rth_std=std2(Rth_JC);

figure;
hold on
plot(time1,Zth1);
plot(time2,Zth2);
set(gca,'xscale','log')

figure;
hold on
plot(Zth1,dadz1);
plot(Zth2,dadz2);

figure;
hold on
plot(Zth2,delta);
plot(Zth2,eps);
```


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THESE DE L'INSA LYON, MEMBRE DE L'UNIVERSITE DE LYON

NOM : AHMED DATE de SOUTENANCE : 15/11/2024
Prénoms : Ahmed Sabry Eltaher

TITRE : Refroidissement haut-performance de composants de puissance enfouis dans un circuit imprimé

NATURE : Doctorat Numéro d'ordre : 2024ISAL0100

Ecole doctorale : MEGA (ED 162)

Spécialité : Thermique Energétiques

RESUME :
L'intégration de dispositifs semi-conducteurs de puissance dans un circuit imprimé (PCB) est une solution prometteuse pour réduire les éléments parasites des circuits, simplifier le packaging des dispositifs et réduire les coûts. Cependant, la réduction continue de la taille des puces semi-conductrices, combinée à la faible conductivité thermique des couches diélectriques des PCB nécessitent des solutions de gestion thermique plus efficaces.
Dans ce projet de recherche, deux solutions de gestion thermique sont étudiées. Tout d'abord, un dissipateur de chaleur en graphite avec une haute conductivité thermique (1300 W/(m.K) dans le plan, et 15 W/(m.K) hors plan) est intégré dans le PCB. Deuxièmement, une solution d'extraction de chaleur basée sur la technique de refroidissement par jet d'eau impactant est mise en œuvre pour collecter la chaleur à la surface du PCB. Pour la solution de dissipation de chaleur, les valeurs des résistances thermiques jonction-environnement et jonction-boîtier (RthJA et RthJC, respectivement), des variantes de PCB avec des diodes et des puces MOSFET intégrées, sont réduites jusqu'à 38 % pour RthJA et 30 % pour RthJC, d'après les mesures. Pour la solution d'extraction de chaleur, le refroidisseur à jet d'eau (JIC) présenté réduit expérimentalement RthJA de 33 % par rapport à une plaque froide conventionnelle. Le coefficient de transfert de chaleur effectif (HTC) du JIC est calculé par simulations et s'élève à environ 43 kW/(m².K) avec une chute de pression de 9,7 kPa. Cette performance permet d'atteindre une densité de puissance de 865 W/cm² sans dépasser la limite de température de jonction de 175°C. Augmenter la conductivité thermique de la couche isolante par un facteur de 10 permettra d'atteindre 993 W/cm² (très proche de l'objectif de 1000 W/cm²).

MOTS-CLÉS : FEM, CFD, simulations thermique, mécanique des fluides, transfert thermique, échangeurs de chaleur, dissipateurs de chaleur, refroidissement, graphite, mesure expérimentale, électronique de puissance, SiC MOSFET packaging, composants de puissance, et fabrication de circuit imprimé.

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